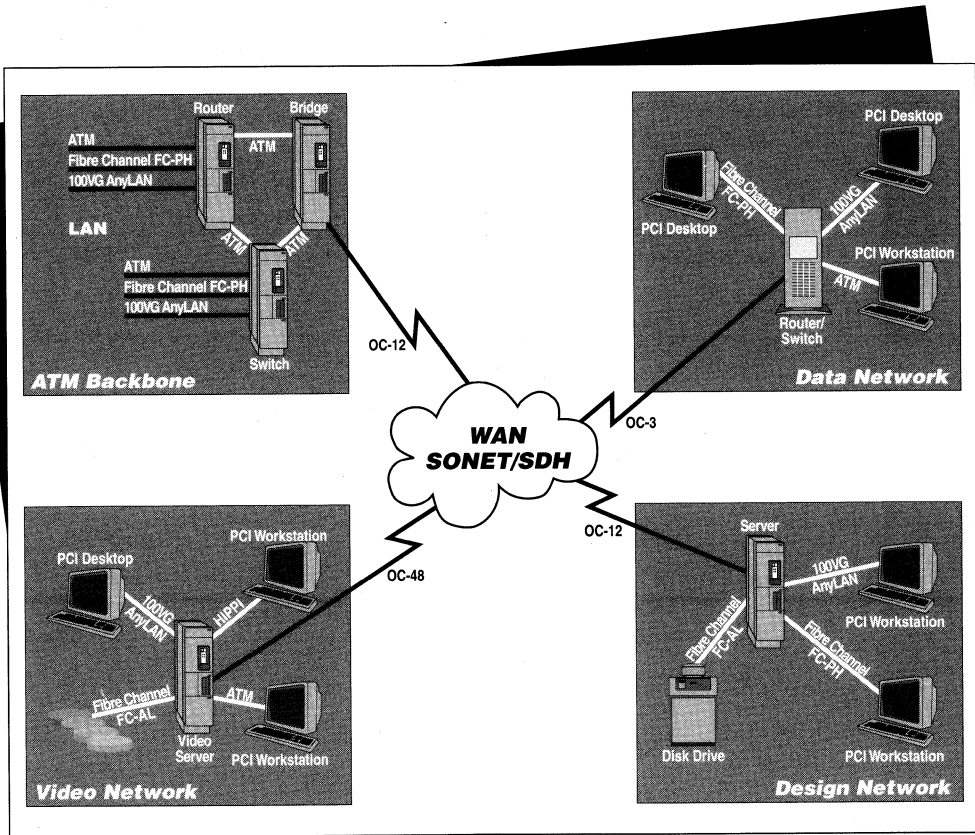


Network Interface Products Data Book





Network Interface Products Data Book

For Marketing and Application Information Contact:

**Applied Micro Circuits Corporation
6195 Lusk Blvd.
San Diego, CA 92121-2793
(619) 450-9333
(800) 755-2622**

The material in this document supersedes
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AMCC reserves the right to ship devices of higher grade in place of those of lower grade.

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AMCC holds the patent for the Clock Driver Output, U.S. Patent 4,970,414. Japan Patent 2-177686.

AMCC holds the patents for the Turbo Design: U.S. Patent 4,835,420; U.S. Patent 4,874,970; U.S. Patent 4,926, 065.

AMCC

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ATM AND 100VG ANYLAN INTERFACE PRODUCT SELECTION GUIDE					
Product	Function	Operating Speed	Data Path	Package	Power Supply
S3011	SONET/ATM/ E-4 Tx	139/155 Mbit/s	8:1 bit	80 TEP	+5.0V
S3012	SONET/ATM/ E-4 Rx	139/155 Mbit/s	1:8 bit	80 TEP	+5.0V
S3020	ATM Tx	622 Mbit/s	8:1 bit	52 TEP	+5.0V
S3021	ATM Rx	622 Mbit/s	1:8 bit	52 TEP	+5.0V
S2100	100VG AnyLAN Transceiver	120 Mbit/s	4:1/1:4 bit	52 PQFP	+5.0V

FIBRE CHANNEL PRODUCT SELECTION GUIDE					
Product	Function	Operating Speed	Data Path	Package	Power Supply
S2036	Open Fiber Control	266/531/1062 Mbit/s	N/A	28 SOIC	+5V
S2042	Fibre Channel Transmitter	266/531/1062 Mbit/s	10:1/20:1 bit	44 PQFP 52 TQFP	3.3V
S2043	Fibre Channel Receiver	266/531/1062 Mbit/s	1:10/1:20 bit	44 PQFP 52 TQFP	3.3V
S2044	GLM Compliant Fibre Channel Transmitter	266/531/2062 Mbit/s	10:1/20:1 bit	52 TQFP	3.3V
S2045	GLM Compliant Fibre Channel Receiver	266/531/2062 Mbit/s	1:10/1:20 bit	52 TQFP	3.3V
S2052	Fibre Channel Transceiver	266/531/1062 Mbit/s	10:1/1:10 bit	52 PQFP	3.3V
S2060	8B/10B Encoder/Decoder	266/531/1062 Mbit/s	10 or 20 bit	120 PQFP	3.3V

HIPPI PRODUCT SELECTION GUIDE					
Product	Function	Operating Speed	Data Path	Package	Power Supply
S2020	HIPPI Source	800 Mbit/s	32 bit	225 PGA/ 208 TEP	-5.2/+5V
S2021	HIPPI Destination	800 Mbit/s	32 bit	225 PGA/ 208 TEP	-5.2/+5V

PCI BUS PRODUCT SELECTION GUIDE		
Product	Function	Description
S5930	PCI Controller	16-Bit Add-on Bus/Serial EPROM Interface
S5931	PCI Controller	16-Bit Add-on Bus/Parallel EPROM Interface
S5932	PCI Controller	32-Bit Add-on Bus/Serial EPROM
S5933	PCI Controller	32-Bit Add-on Bus/Parallel or Serial EPROM

SONET/SDH PRODUCT SELECTION GUIDE					
Product	Function	Operating Speed	Data Path	Package	Power Supply
S3005	SONET/E-4 Tx	139/155/622 Mbit/s	8:1 bit	68 LDCC 80 TEP	-4.5/5.0V
S3006	SONET/E-4 Rx	139/155/622 Mbit/s	1:8 bit	68 LDCC 80 TEP	-4.5/5.0V
S3014	CSU/CRU	155/622 Mbit/s	1 bit	44 PLCC	-5.2/+5.0V
S3015	E4/OC-3/STM-1 Interface Tx	139/155 Mbit/s	1 bit	52 TEP	+5V
S3016	E4/OC-3/STM-1 Interface Rx	139/155 Mbit/s	1 bit	52 TEP	+5V
S3017	SONET/SDH Tx	622 Mbit/s	8:1 bit	52 TEP	+5V
S3018	SONET/SDH Rx	622 Mbit/s	8:1 bit	52 TEP	+5V
S3019	SONET/SDH /ATM Transceiver	155/622 Mbit/s	1:8/8:1 bit	52 PQFP	+3.3V
S3022	SONET STPC	155/622 Mbit/s	1:8/8:1 bit	120 TEP	+5V
S3025	SONET/SDH CRU	155/622 Mbit/s	1 bit	16 PLCC	+5V

CROSSPOINT SWITCH PRODUCT SELECTION GUIDE					
Product	Function	Operating Speed	Data Path	Package	Power Supply
S2016	Crosspoint Switch	1.5 Gbit/s	16 x16	120 TEP	+5V
S2024	Crosspoint Switch	600/800 Mbit/s	32x32	196 LDCC	-5.2/+5V
S2025	Crosspoint Switch	1.5 Gbit/s	32x32	196 LDCC	+5V

5V SUPPLY-TTL I/O CLOCK DRIVER SELECTION GUIDE						
	Output Frequency with Respect to Input Frequency					
P/N	Total Outputs	Number of Outputs + 1	Number of Outputs + 2	Number of Outputs + 2 or 4	Special Features	Package
SC3500	20	10	5 + 1 or 2	5	—	52 PQFP
SC3506	20	10	10	N/A	—	52 PQFP
SC3507	20	10	N/A	10	—	52 PQFP
SC3508	20	20	N/A	N/A	—	52 PQFP
SC3517	10	5	N/A	5	—	28 SOIC
SC3518	10	10	N/A	N/A	—	28 SOIC
SC3526	9	5	4	N/A	Sync Output	28 SOIC
SC3527	10	3	7	N/A	Selectable single or dual clock input.	28 SOIC
SC3528	10	10	N/A	N/A	—	28 SOIC
SC3529	10	10	N/A	N/A	Power Down	28 SOIC

5V SUPPLY-LVTTL I/O CLOCK DRIVER SELECTION GUIDE					
	Output Frequency with Respect to Input Frequency				
P/N	Total Outputs	Number of Outputs + 1	Number of Outputs + 2	Special Features	Package
SC3306	20	10	10		52 PQFP
SC3308	20	20	N/A		52 PQFP
SC3318	10	10	N/A		28 SOIC
SC3327	10	3	7	Selectable single or dual clock input.	28 SOIC
SC3367	14	7	7	Selectable single or dual clock input, 1 output early.	28 SOIC
SC3368	14	6	8	Selectable single or dual clock input.	28 SOIC

3.3V SUPPLY-LVTTL I/O CLOCK DRIVER SELECTION GUIDE					
	Output Frequency with Respect to Input Frequency				
P/N	Total Outputs	Number of Outputs + 1	Number of Outputs + 2	Special Features	Package
S3LV306	20	10	10		52 PQFP
S3LV308	20	20	N/A		52 PQFP
S3LV318	10	10	N/A		28 SOIC
S3LV368	14	6	8	Selectable single or dual clock input.	28 SOIC

CLOCK GENERATOR AND SYNTHESIZER SELECTION GUIDE							
	Output Frequency Group with Respect to Input Frequency						
P/N	Description	Input Reference	Number	Type	Max. Freq.	Min. Delay Adjust Increment	Number of Selectable Output Relationships
S4402	Multiphase Clk Generator	TTL	6	TTL	80	3.2 ns	21
S4403	Multiphase Clk Generator	TTL	10	TTL	80	3.2 ns	21
S4405	Multiphase Clk Generator with PECL I/O	PECL/TTL	6 1	TTL PECL	80 160	3.2 ns —	21 —
S4406	Clock Generator with Delay Adj. & Invert	TTL	12	TTL	66	4 ns @ 66 MHz	7 x 4 Banks of 3 Outputs
S4501	Clock Multiplier	TTL	2	TTL	100	N/A	3
S4503	Clock Synthesizer	XTAL	2 1	TTL PECL	80 300	N/A	Multiply 2-32 Divide 2-16
S4505S	RAMBUS™ Compatible Clock Generator	XTAL	2	RAMBUS Compatible	270	N/A	1
S4LV406	3.3V Clock Generator	TTL	12	LVTTL	80	1.25 ns	7 x 4 Banks of 3 Outputs

ASIC PRODUCT SELECTION GUIDE				
Part Number	Technology	Equivalent Gates (Full Adder Method)	Number of I/O	Structured Array Blocks
Q20004	1 Micron Bipolar	671	28	None
Q20010	1 Micron Bipolar	1469	66	None
Q20025	1 Micron Bipolar	4032	100	None
Q20045	1 Micron Bipolar	6782	128	None
Q20080	1 Micron Bipolar	11242	162	None
Q20120	1 Micron Bipolar	18777	198	None
Q20P010	1 Micron Bipolar	928	34	1 GHz PLL
Q20P025	1 Micron Bipolar	3120	51	1 GHz PLL
Q20M100	1 Micron Bipolar	13475	195	RAM

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COMPANY OVERVIEW

AMCC defines, develops, manufactures and markets application specific standard products (ASSPs) and application specific integrated circuits (ASICs) for high speed, high performance network interface applications. Utilizing CMOS, BiCMOS and proprietary MicroPower Bipolar technology, AMCC provides precision clocking devices and interface solutions for PCI, ATM, SONET, and Fibre Channel standards.

Since 1979, AMCC has designed and produced five generations of semicustom bipolar ECL logic arrays and two generations of BiCMOS logic arrays. AMCC ASIC expertise includes its mixed ECL/TTL interface, phase-locked loop (PLL), precision vernier, skew control, high-speed VCO and controlled edge rate output.

AMCC Product Development Strategy

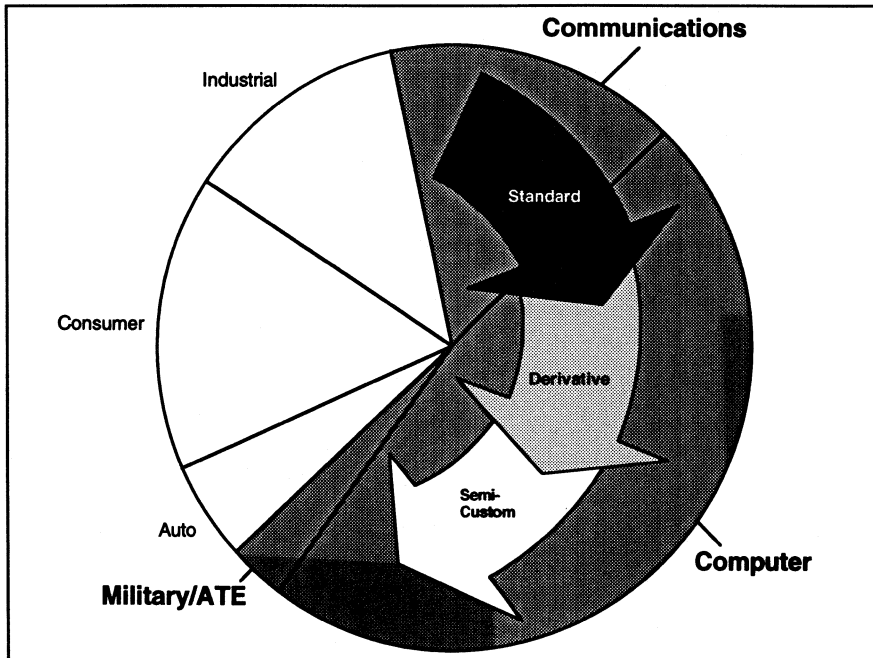
AMCC's product development strategy utilizes the company's expertise in the computer, communications, ATE and military markets. Initially ASSPs are defined based on key industry standards. Then, as additional applications are identified, derivative products based on the "cores" of the original devices are introduced. The "cores" are then also made available for high volume proprietary ASIC designs.

Network Interface Products

High performance network interface encompasses a wide range of applications, all requiring data transmission rates from >100 Mbit per second to over 1 Gbit per second, and beyond. These applications include computer data transmission, fiber-optic telecommunications transmission systems, digital video broadcasting and many more.

AMCC interface circuits, transmitter/receiver chip sets and switches are designed to implement emerging network technologies such as the ANSI or ITU approved Asynchronous Transfer Mode (ATM), Synchronous Optical Network (SONET), Fibre Channel, and High Performance Parallel Interface (HIPPI) telecommunications standards. Jitter, speed, power and size are critical design issues of these technologies. AMCC's devices are based on its unique bipolar process which has superior noise isolation characteristics that significantly reduce jitter. The inherent physical structure of the company's process makes 1 to 3 GigaHertz (GHz) data rates possible at relatively low power. The low device power consumption of AMCC's products helps to minimize the cost and size of packaging.

AMCC Product Development Strategy



Peripheral Component Interconnect (PCI) Controllers

Increased bandwidth available on high speed networks creates a bottleneck at the desktop. One of the causes of this problem is the latency associated with connection to high speed peripheral equipment, including LANs and WANs. The 132 Megabyte per second backplane PCI bus breaks the bottleneck.

AMCC has developed the industry's first line of general purpose master/slave controllers for the PCI bus. These circuits provide a high performance single-chip interface for add-on boards and adapter cards.

Precision Clock and Timing Products

AMCC provides a growing line of precision clock and timing standard products for exacting system designs. AMCC has also tailored clock and timing devices to specific customer needs for high performance clock generation and distribution, clock synchronization and de-skewing, frequency synthesis, and pulse shaping applications. Offerings include low EMI, low skew clock drivers and low jitter clock generators for high performance server and workstation applications.

Strategic Partnerships

AMCC manufactures its own 1.0 micron BiCMOS and Bipolar wafers using proven processes. The Company follows a "semi-fabbed" manufacturing strategy and has reciprocal foundry relationships in place with major domestic and international semiconductor partners that provide for significant additional production capacity. Wafer purchases from strategic foundry partners both expand capacity and provide alternate sources. Additional high-volume assembly and test facilities are located offshore.

AMCC's "quick turn, semi-fabbed" manufacturing approach blends together the strengths of both the "fabbed" and "fabless" semiconductor strategies. Fabbed advantages include the security of total in-house control and time to market. Fabless advantages include multiple sourcing and allows the company to focus investment on new high performance products.

AMCC COMMITMENT TO QUALITY

Quality is the degree to which a product meets a customer's expectations with regard to delivery time, cost, and performance to the requirements of the application.

Reliability is "...the probability of a product performing, without failure, a specified function under given conditions for a specified period of time."¹

AMCC is committed to achieving the highest quality and reliability level in the integrated circuit products we provide. Every year for over a decade we have established industry-leading reliability and outgoing quality targets and then beat them.

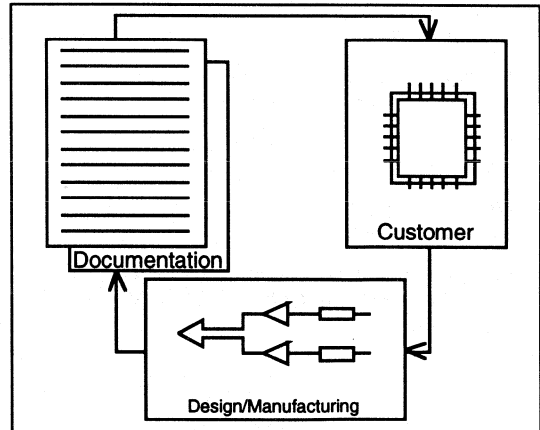
The quality and reliability philosophy at AMCC starts with the premise that for AMCC to continue to excel in the ever expanding market place, the quality expectations of customers must be met or exceeded.

Our team operating philosophy is to:

- 1) design in manufacturability and reliability during the new product development phase (plan);
- 2) build in quality at all manufacturing steps (do);
- 3) execute thorough product inspections, internal audits and reliability confirmation (check);
- 4) incorporate feedback from internal and external sources into continuous quality improvement programs (act).

Reliability and Manufacturability—Designed In From The Start

Reliability and manufacturability is designed in up front through a team infrastructure which focuses on active participation by Design, Manufacturing and Reliability Engineering throughout all phases of the design process. This includes extensive design verification through computer modeling and design validation by product characterization and application simulation. Final team design review and production readiness approval is required prior to release of products to production.



QA gates and subsequent feedback ensures quality confirmation of AMCC's final product in a continuous improvement program.

Quality Built In During Wafer Fabrication and Manufacturing

AMCC's manufacturing and quality teams employ documented operating procedures, work instructions, in-process inspections and SPC methodology to provide assurance of continued process control and compliance to specification.

Inspection, Audit and Reliability Confirmation

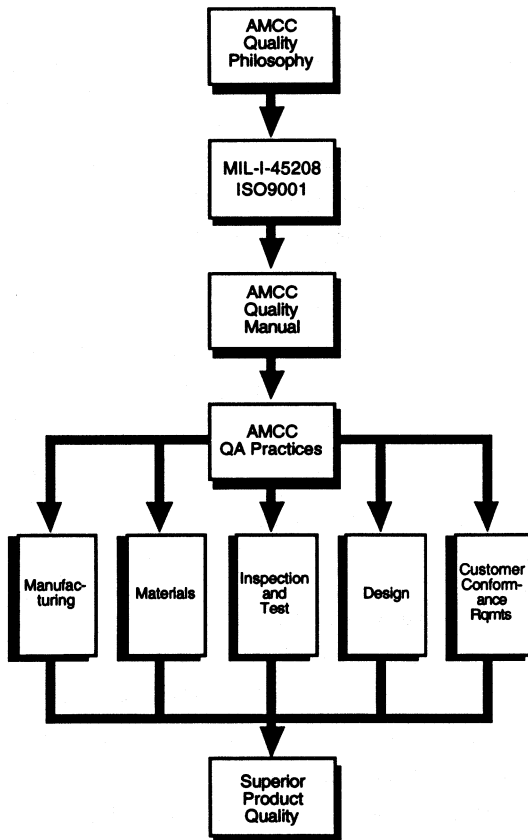
AMCC has strategically placed In-Process Quality Control (IPQC) gates, internal process/area audits and lot/time specific reliability monitors to verify performance against customer requirements and internal design/manufacturing process capabilities. Metrics generated by these activities are intended to provide continuous improvement feedback data for review and action as driven by senior management.

- Die visual and precap gate
- Final outgoing inspection gate
- Modified MIL-STD-105D sampling program
- Lot specific group A and B testing
- Ongoing reliability monitors
- SPC/Data metric review of key subcontractors
- Visual/mechanical and electrical outgoing indices and PPM goals
- Cost-of-quality pareto analysis

¹ JURAN

Continuous Quality Improvement Program

- Corporate-wide commitment driven by the Executive Staff
- A program plan that is flexible enough to comprehend dynamic customer inputs
- Statistical tools in place for analysis and action planning
- Weekly and monthly review meetings to share performance data
- Self examination consistent with elements in ISO9001 and the *Malcolm Baldrige National Quality Award*



AMCC QUALITY SYSTEM

The Quality System had been modeled after the stringent military requirements of MIL-I-45208, MIL-Q-9858 and MIL-I-38535 Appendix A. Heading into the 21st century, AMCC is now modifying its Quality System to also align with ISO9001. This will strengthen the closed loop improvement cycle by tying internal audits with corrective/preventative action through continuous management review.

AMCC's Quality System has the following components integrated throughout the factory to meet or exceed the above requirements.

- Quality Organization
- Quality Planning
- Management Review
- Contract Review
- Design Control
- Document and Data Control
- Purchasing
- Supplier Selection and Control
- Control of Customer Supplied Materials
- Product Identification and Traceability
- Operating Procedures
- Work Instructions
- Inspection and Test
- Inspection, Measurement and Test Equipment Calibration
- Inspection Status System
- Control of Nonconforming Material
- Corrective and Preventive Action
- ESD Safe Handling, Storage, Packaging, Preservation and Delivery Methods
- Records Retention and Maintenance
- Internal Process/Area Auditing System
- Training/Certification
- SPC and Statistical Techniques
- Failure Analysis

ISO9001 REGISTRATION

Based on the restructure of the Quality System to ISO9001 requirements and successful completion of internal and third-party audits, AMCC plans to be ISO registered by June of 1996. Please contact the factory for further details and schedule updates.

PRODUCT QUALIFICATIONS

A qualification is a sequence of tests in which all parameters, including the reliability of the device are tested. It is this sequence of tests which **initially qualifies** the part to be released for production.

Thorough reliability testing is performed on new product and package families in order to ensure the expectations of our customers are met. These tests include environmental, mechanical and life testing performed in accordance with Military Standards, industrial accepted methods and AMCC Test Procedures. Contact the factory for specific details regarding your selected product/package combination.

AMCC provides MIL-STD-883 Methods 5005, 5008, and 5010 testing for our military customers on contract.

MIL-STD-883 Method 5005

“Qualification And Quality Conformance Procedures”

Method 5005 establishes qualification and quality-conformance inspection procedures for semiconductors to ensure that the quality of devices and lot conform with the requirements of the applicable procurement document. The full requirements of Group A, B, C, D, and E test and inspections are intended for use in initial device qualification—or requalification in the event of product or process change—and in periodic testing for retaining qualification.

Group A consists of electrical tests performed on an inspection lot which has already passed the 100% screening requirements. After a lot has passed the 100% screen tests, a random sample of parts is selected from the total population of devices to form the inspection lot. The inspection lot is then subjected to these Group A electrical tests.

Group B inspection tests are used to monitor the fabrication and assembly processes performed on each inspection lot.

Group C consists of a 1000-hour life test conducted to verify die integrity.

Group D verifies the material integrity and the reliability of the package.

Group E demonstrates the radiation hardness capability of the device. Performed on a generic basis by device type or as required for an application.

MIL-STD-883 Method 5010

“Test Procedures For Custom Monolithic Microcircuits”

This method establishes screening and quality conformance procedures for the testing of custom and semicustom monolithic semiconductors to verify Class B or Class S quality and reliability levels. Testing is performed in conjunction with other documentation such as MIL-I-38535 and an applicable detail specification. It establishes the design, material, performance, control, and documentation requirements needed to achieve prescribed levels of device quality and reliability. AMCC can support qualification using this method.

Until August of 1983, the qualification most commonly used was Method 5005. Since that time, the newer revision of MIL-STD-883 includes Method 5010, which is better suited for semicustom devices (logic arrays included). Either qualification is adequate, but it is desirable to use the 5010 qualification procedure in qualifying custom or semicustom devices.

Qualification Method 5005 VS. 5010

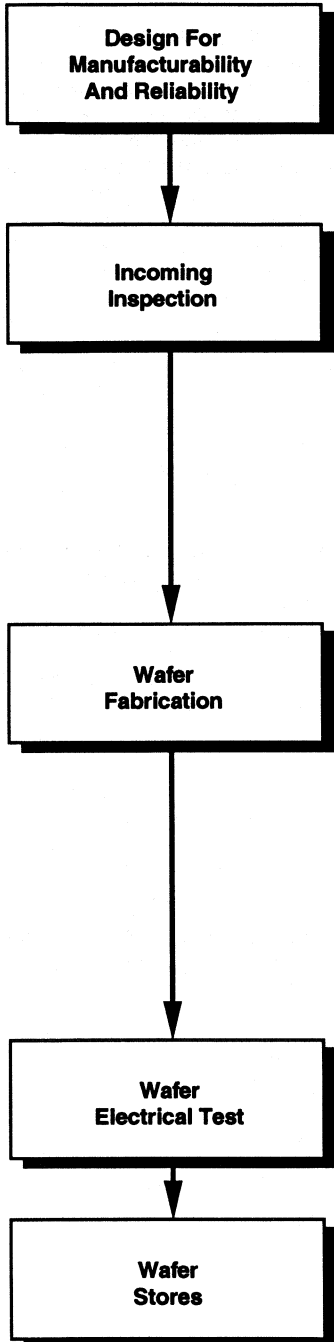
The primary difference between the two methods is in the Group D test. Method 5005 uses electrically-good devices, where method 5010 uses electrical rejects and package-only parts for environmental tests. In addition, Method 5010 is designed for smaller production releases (i.e., 2000 devices/year) while Method 5005 is designed for large production releases.

Generic Data

Under the provision of MIL-I-38535, a customer can elect to qualify using generic data (similar device/family). However, the provisions of the applicable contract should be reviewed. In most cases generic data will satisfy full qualification requirements.

Since many of the qualifications at AMCC are on-going, generic data may be available for this purpose.

AMCC Product Assurance Product Flow Detail

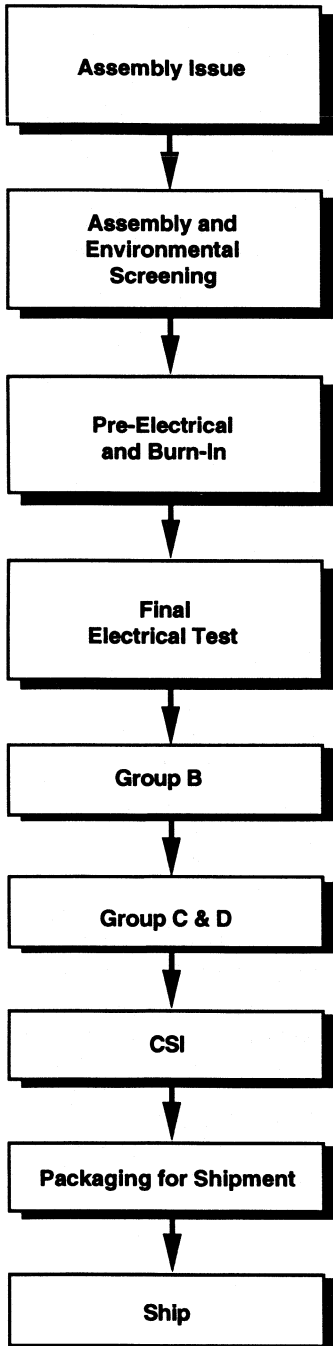


- Component Selection
 - Definition — Specification
 - Supplier: Selection — Qualification — Approval
 - Qualified Vendors List (QVL)

- Acceptance Documents and Operating Procedures
 - Purchase Order
 - Component/Material Specifications
 - Product Assurance and General Procedures
 - QVL
 - Sample Inspection of All Direct Materials

- Class 10 Clean Room — FED-STD-209
- Measurements in Adherence with MIL-STD-977
- SPC:
 - In-process Monitors
 - PCM Electricals
- SEM Inspection on All Military Lots
- QA Audits
 - CV Plots — Weekly (minimum)
 - DI Water — Weekly
 - Particle Counts
 - Bacteria Count
 - Airborne Particle Count — Weekly

AMCC Product Assurance Product Flow Detail



- IPQC Audit
- Manufacturing Procedures

Hermetic Military Flow

- Method 5004¹
- IPQC
 - Customer Source Inspection (CSI)
 - Assembly Final Inspection
- Methods 5004 & 5005¹

Hermetic Commercial Flow

- Method 5004 (No Centrifuge)
- IPQC
 - Assembly Final Inspection
- 25°C — 100%
- 0°C & 70°C — AQL=0.25% Sample

Plastic Flow

- Precap Visual
 - Die Shear SPC
 - Wire Bond SPC
- Mold/External Visual
- Lead Trim and Coplanarity Inspection

- Methods 5004 & 5005¹
- IPQC
 - Group A

- Method 5005¹
- IPQC
 - Final Inspection
- Method 5005¹
- Performed by Customer Order

- IPQC
 - Final Inspection
 - Coplanarity Check

- Per Order

- IPQC
 - Outgoing Inspection

- IPQC
 - Outgoing Inspection

¹Method 5008 or 5010 available

AMCC'S RELIABILITY VIGIL

AMCC's internal reliability vigil consists of three phases:

- New/changed processes and material qualifications
- In-process Quality monitors
- Periodic operating life and environmental testing

New/Changed Wafer Processes and Material Qualifications

In order to initially release a device to production a standard set of MIL-STD-883 tests must be completed successfully. These tests include:

Wafer Process and Design

- Operating Life Method 1005
- ESD Characterization Method 3015
- Wire Bond Pull Method 2011
- Thermal Shock or Method 1011 or 1010 Temperature Cycling

Package and Related Materials

- Selected Subgroups of MIL-STD-883, Method 5005, Group B and D

AMCC adheres to MIL-I-38535 with regards to changes.

If changes to production released devices are determined to be major, the appropriate qualification testing must be successfully completed prior to change approval.

In-Process Quality Monitors

- CV plots
- Airborne particle count
- Bacteria, particle count, and resistivity on DI water
- ESD work stations and procedures
- In-line testing of process gases
- Temperature and humidity control
- SPC in wafer fabrication
- SEM of all military lots

Periodic Operating Life and Environmental Testing

- Performed on a product from each process family quarterly.
- 1000 hour operating life test (minimum), Method 5005, Group C.
- Temperature cycling per Method 1010, 100 cycles, condition C: $-65^{\circ}\text{C}/150^{\circ}\text{C}$
- Environmental testing per AMCC standard test procedures. Consult factory for further details.

Final Measure and Assurance of Quality

The cost of defects depends on when the failure occurs. For example, costs rise significantly as undetected defective ICs are integrated into systems. High quality parts cut costs substantially, and the extra quality built into every AMCC device means added value to our customers.

To achieve maximum quality, AMCC employs 100% testing of all devices, followed by stringent QA sampling.

AMCC performs QA sampling measurements at full specification temperature, both DC and AC, to achieve the tightest AQLs in the industry.

RADIATION HARDNESS

High energy radiation can cause structural changes in the silicon and silicon dioxide crystal lattice by displacing atoms from their normal crystal sites. These changes can be responsible for increased junction leakage, degraded transistor current gain (b), and increased parasitic Si/SiO₂ interface leakage currents. The damage is generally induced by neutrons, X-rays, and gamma rays. The effects of the damage induced by this radiation can change both AC and DC parameters, affect functional performance, and, in severe cases, destroy the device.

Certain of AMCC's high performance products are inherently radiation resistant. The radiation resistance of AMCC IC's is the result of the small geometries, the structure of the fabrication process itself, and the use of ECL logic within the device. Contact your AMCC representative regarding radiation resistance characteristics associated with a specific product.

CONTENTS

ATM AND 100VG ANYLAN PRODUCTS

S3011/S3012–SONET/SDH/ATM OC-3 Transmitter and Receiver	3-3
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FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLL for clock generation and clock recovery
- Supports 155.52 Mbit/s (OC-3)
- Reference frequency of 19.44 MHz
- Interface to both PECL and TTL/CMOS logic
- 8-bit TTL/CMOS datapath
- Compact 80 PQFP package
- Diagnostic loopback mode
- Lock detect
- Low jitter PECL interface
- < 2.5 Watt per set

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET
- Section repeaters
- Add drop multiplexors
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

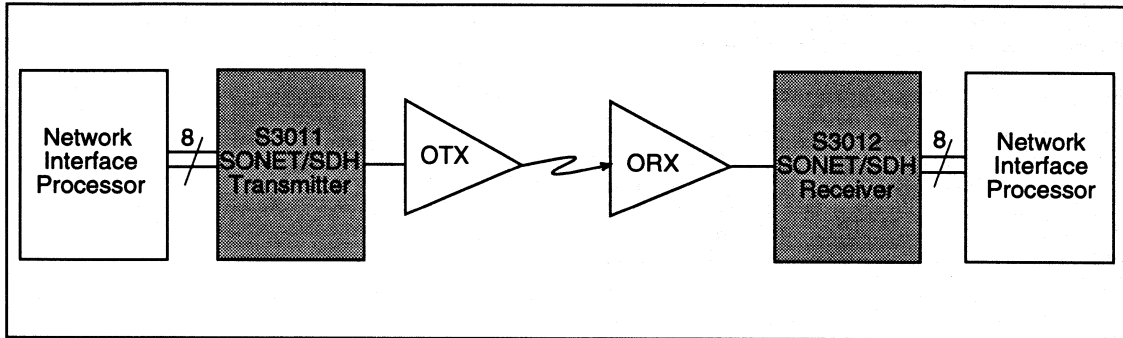
GENERAL DESCRIPTION

The S3011/S3012 SONET/SDH transmitter and receiver chips are fully integrated serialization/deserialization SONET OC-3 (155.52 Mbit/s) interface devices. With architecture developed by the Pacific Microelectronics Centre (PMC), the chipset performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The devices are also suitable for ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3011 transmitter chip allowing the use of a slower external transmit clock reference. Clock recovery is performed on the S3012 receiver chip by synchronizing its on-chip VCO directly to the incoming data stream. The S3012 also performs SONET/SDH frame detection. The chipset can be used with 19.44 MHz reference clocks, in support of existing system clocking schemes.

The low jitter PECL interface guarantees compliance with the bit-error rate requirements of the Bellcore, ANSI, and ITU-T standards. The S3011/S3012 chipset is packaged in a 80 PQFP, offering designers a small package outline.

Figure 1. Link Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Figure 2. SONET Structure

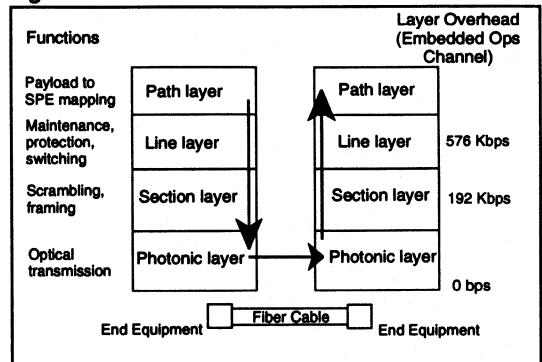


Table 1. SONET Signal Hierarchy

Elec.	ITU-T	Optical	Data Rate (Mbit/s)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-9		OC-9	466.56
STS-12	STM-4	OC-12	622.08
STS-18		OC-18	933.12
STS-24		OC-24	1244.16
STS-36		OC-36	1866.24
STS-48	STM-16	OC-48	2488.32

Data Rates and Signal Hierarchy

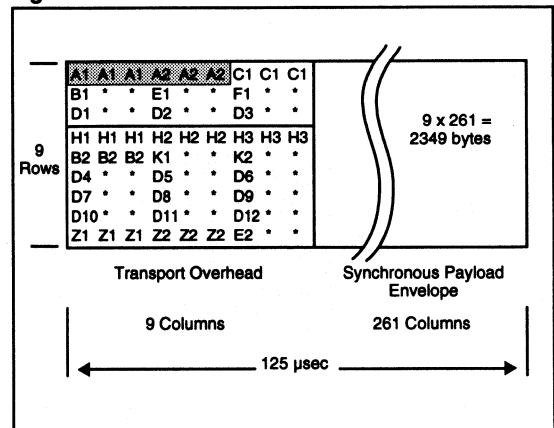
Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3011/S3012 chipset supports OC-3 rates (155.52 Mbit/s).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-3 consists of nine transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 9 overhead and 261 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the ANSI SONET standard document.

Figure 3. STS-3/OC-3 Frame Format



S3011/S3012 OVERVIEW

The S3011 transmitter and S3012 receiver implement SONET/SDH serialization/deserialization, transmission, and frame detection/recovery functions. The block diagrams in Figures 4 and 5 show basic operation of both chips. These chips can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface (S3011) and the serial receive interface (S3012). The chipset handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation and recovery, and system timing, which includes management of the datastream, framing, and clock distribution throughout the front end.

Operation of the S3011/S3012 chips is straightforward. The sequence of operations is as follows:

Transmitter

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver

1. Clock and data recovery from serial input
2. Frame detection
3. Serial-to-parallel conversion
4. 8-bit parallel output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 9 through 14.

A lock detect feature is provided on the S3012, which indicates that the PLL is locked (synchronized) to the data stream, and facilitates continuous down-stream clocking in the absence of data.

Suggested Interface Devices

PMC PM5345	SUNI	Saturn User Network Interface
IGT WAC-013-A		SONET LAN ATM Processor
Fujitsu MB86683	NTC	Network Termination Controller
PMC PM5301	SSTX	Section Overhead Transceiver
Siemens	V23806-A8-C1	Fiber Optic Transceiver
HP	HFBR-520X	Fiber Optic Transceiver
CTS	ODL-1408	Fiber Optic Transceiver
Sumitomo	SDM4123-XC	Fiber Optic Transceiver
AMP	269039-1	Fiber Optic Transceiver
Mitsubishi	MF-156DS-TR124	Fiber Optic Transceiver

Figure 4. S3011 Transmitter

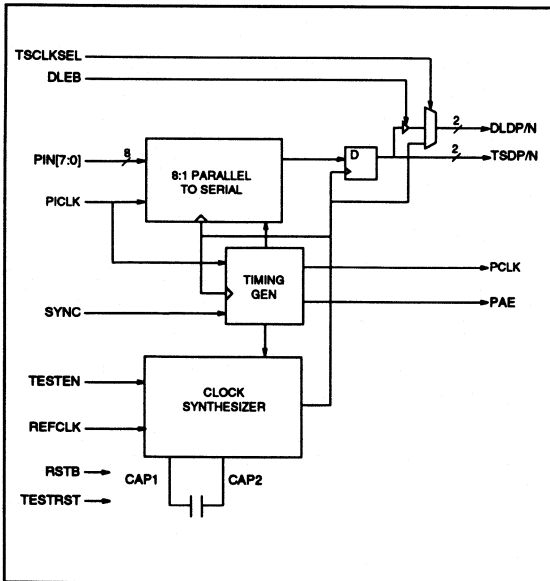
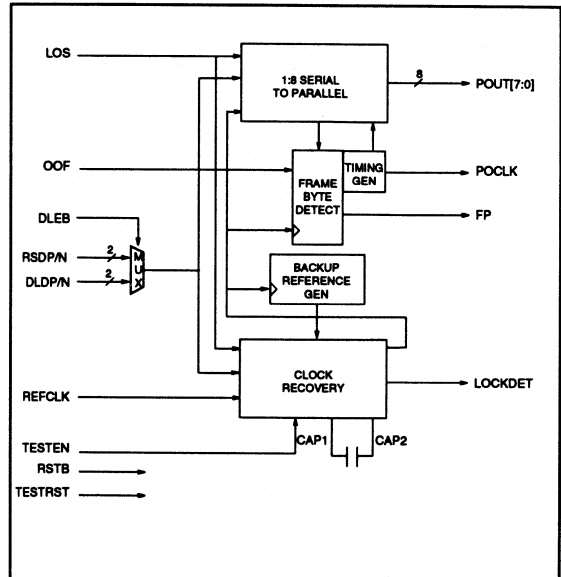


Figure 5. S3012 Receiver



S3011 TRANSMITTER ARCHITECTURE/FUNCTIONAL DESIGN

The S3011 transmitter chip performs the serializing stage in the processing of a transmit SONET STS-3 bit serial data stream. It converts the byte serial 19.44 Mbyte/sec data stream to bit serial format at 155.52 Mbit/sec.

A high-frequency bit clock can be generated from a 19.44 MHz frequency reference by using an integral frequency synthesizer consisting of a phase-locked loop circuit with a divider in the loop.

Diagnostic loopback is provided (transmitter to receiver) when used with the compatible S3012. (See Other Operating Modes.)

Clock Synthesizer

The Clock Synthesizer, shown in the block diagram in Figure 4, is a monolithic PLL that generates the serial output clock phase synchronized with the input reference clock (REFCLK).

The REFCLK input must be generated from a TTL crystal oscillator which has a frequency accuracy of better than 20 ppm in order for the TSCCLK frequency to have the same accuracy required for operation in a SONET system. Lower accuracy crystal oscillators may be used in applications less demanding than SONET/SDH.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCLK input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

Timing Generator

The Timing Generator, seen in Figure 4, provides two separate functions. It provides a byte rate version of the transmit serial clock, and a mechanism for aligning the phase between the incoming byte clock and the clock which loads the parallel-to-serial shift register.

The PCLK output is a byte rate version of transmit serial clock at 19.44 MHz. PCLK is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for up-

stream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3011 device.

In the parallel-to-serial conversion process, the incoming data is passed from the PICKLK byte clock timing domain to the internally generated byte clock timing domain, which is phase aligned to transmit serial clock. Although the frequency of PICKLK and the internally generated byte clock is the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PICKLK and the internally generated byte clock. Should the magnitude of the phase difference be less than one bit period, and if the SYNC input is high, the timing block inverts the internal byte clock.

Since the inversion of the internal byte clock will corrupt one byte of data, SYNC should be held low except when a phase correction is desired. When a timing domain phase difference of less than one bit period is detected, the Phase Alignment Event output (PAE) pulses high for one PCLK clock period. If the condition persists, PAE will remain high. When PAE conditions occur, SYNC should be activated until the condition is no longer present.

After the S3011 device is reset, two cycles of PICKLK are required to initialize the internal byte clock. The starting point of the internal byte clock is four serial bit times after the detected rising edge of PICKLK. The relative phase between PICKLK and the PCLK output is arbitrary, but it must remain constant with variations within the range of -2 to +3 bit times (-90° to +135°) in order to avoid generating PAE pulses. This operating constraint must be observed if the SYNC and PAE functions are not used or desired.

Parallel-to-Serial Converter

The Parallel-to-Serial converter shown in Figure 4 is comprised of two byte-wide registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PICKLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

An internally generated byte clock, which is phase aligned to the transmit serial clock as described in the Timing Generator description, activates the parallel data transfer between registers. The serial data shifts out of the second register and into the output selection logic at the transmit serial clock rate.

TRANSMITTER PIN DESCRIPTIONS

Input Signals

Parallel Data Input [PIN]<7:0>. TTL. A 19.44 Mbyte/sec word, aligned to the PICKL parallel input clock. PIN<7> is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PIN<0> is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). PIN<7:0> is sampled on the rising edge of PICKL.

Parallel Input Clock [PICKL]. TTL. A 19.44 MHz nominally 50% duty cycle input clock, to which PIN<7:0> is aligned. PICKL is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PICKL samples PIN<7:0>. After a Master Reset two rising edges of PICKL are required to fully initialize the internal datapath.

Test Clock Enable [TESTEN]. TTL. Set high to provide access to the PLL during production tests.

Synchronization Enable [SYNC]. TTL. Active high input that enables the timing generator to invert the internal byte transfer clock if transfers from the PIN<7:0> input holding register are occurring less than one bit period before or after clocking new data into the holding register. The SYNC pin is an asynchronous input.

Reference Clock [REFCLK]. TTL. Input used as the reference for the internal bit clock frequency synthesizer.

Diagnostic Loopback Enable [DLEB]. TTL. Enables the DLD output when low and TSCLKSEL is low. When DLEB is high, the DLD output is held in the inactive state to prevent interference between the transmit and receive devices.

Master Reset [RSTB]. TTL. Reset input for the device, active low.

Transmit Clock Select [TSCLKSEL]. TTL. Active high input which when enabled directs the transmit serial clock through the DLDP/N output.

Test Reset [TESTRST]. TTL. Used to reset portions of the clock recovery PLL during production testing. Held low for normal operation.

Loop Filter Capacitor [CAP1, CAP2]. The loop filter capacitor is connected to these pins. The capacitor value should be 0.01 μ f \pm 10% tolerance, X7R dielectric. 50 volt is recommended (16 volt is acceptable).

Output Signals

Transmit Serial Data [TSDP/N]. Differential PECL. Serial data stream signals, normally connected to an optical transmitter module.

Diagnostic Loopback Data [DLDP/N]. Differential PECL. Serial data stream signals, normally connected to a companion S3012 device for diagnostic loopback purposes. They are held inactive when DLEB is high and TSCLKSEL is low. The serial data stream is output when DLEB is low and TSCLKSEL is low. When enabled by the TSCLKSEL input the transmit serial clock will be output through this pin. The transmit serial clock is a buffered version of the internal frequency synthesizer clock, which is phase-aligned with the TSD output signal. The TSD is updated on the falling edge of the transmit serial clock.

Parallel Clock [PCLK]. TTL/CMOS. A reference clock generated by dividing the internal bit clock by eight. It is normally used to coordinate byte-wide transfers between upstream logic and the S3011 device.

Phase Alignment Event [PAE]. TTL/CMOS. Pulses high during each PCLK cycle for which there is less than one bit period between the internal byte clock and PICKL timing domains. PAE is updated on the falling edge of the PCLK output.

S3012 RECEIVER ARCHITECTURAL/FUNCTIONAL DESIGN

The S3012 receiver chip provides the first stage of digital processing of a receive SONET STS-3 bit-serial stream. It converts the bit-serial 155.52 Mbit/sec data stream into a 19.44 Mbyte/sec byte-serial data format.

Clock recovery is performed on the incoming scrambled NRZ data stream. A 19.44 MHz reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference to the nominal bit rate.

A loopback mode is provided for diagnostic loopback (transmitter to receiver), when used with the compatible S3011 device.

Clock Recovery

Clock Recovery, as shown in the block diagram in Figure 5, generates a clock that is at the same frequency as the incoming data bit rate at the RSD or DLD inputs. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock. Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost.

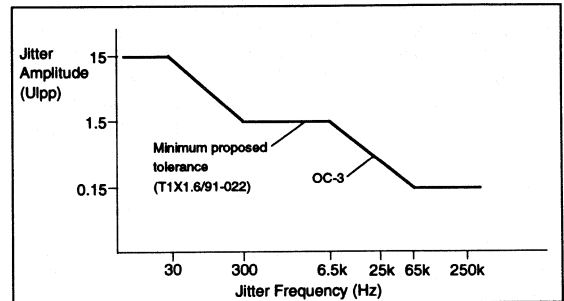
The clock recovery circuit monitors the incoming data stream for loss of signal. If the incoming data stream has had no transitions for between 96 and 208 bit times (depending upon the state of an internal counter at the time of last transition), loss of signal is declared and the PLL will switch from locking onto the incoming data to locking onto the reference clock. Alternatively, the loss-of-signal (LOS) input can be used to force a loss-of-signal condition. When set low, LOS squelches the incoming data stream, and thus causes the PLL to switch its source of reference 64 to 128 bit times afterwards. Loss-of-signal condition is removed when LOS is high, and good data, with acceptable pulse density and run length, returns on the incoming data stream.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields a typical capture time of 32 μ s for random incoming NRZ data. A single

external clean-up capacitor is utilized as part of the loop filter.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which meets, with ample margin, the minimum tolerance proposed for SONET equipment by the T1X1.6/91-022 document, shown in Figure 6.

Figure 6. Clock Recovery Jitter Tolerance



Backup Reference Generator

The Backup Reference Generator seen in Figure 5 provides backup reference clock signals to the clock recovery block when the clock recovery block detects a loss of signal condition. It contains a counter that divides the clock output from the clock recovery block down to the same frequency as the reference clock REFCLK.

Frame and Byte Boundary Detection

The Frame and Byte Boundary Detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. Framing pattern detection is enabled and disabled by the out-of-frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration that OOF is set high. It is disabled when a framing pattern is detected and OOF is no longer set high. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (RSD or DLD). The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). The frame boundary is reported on the frame pulse (FP) output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an STS-3 stream will generate the 48-bit framing pattern is extremely small. It is highly improbable that a mimic pattern would occur within one frame of data. Therefore, the time to match the first frame pattern and to verify it with down-stream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 μ s, even for extremely high bit error rates.

Once down-stream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input can be set low to disable the frame search process from trying to synchronize to a mimic frame pattern.

Serial-to-Parallel Converter

The Serial-to-Parallel Converter consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the clock recovery block. The second is an 8-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the Serial-to-Parallel converter can vary from 1.5 to 2.5 byte periods (12 to 20 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries, with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial to parallel converter is that POCLK is neither truncated nor extended during reframe sequences.

S3012 RECEIVER PIN DESCRIPTIONS

Input Signals

Receive Serial Data [RSDP/N]. Differential PECL. Serial data stream signals normally connected to an optical receiver module. A clock is recovered from transitions on the RSD inputs.

Diagnostic Loopback Data [DLDP/N]. Differential PECL. Serial data stream signal, normally connected to a companion S3011 device for diagnostic loopback purposes. Clock is recovered from transitions on the DLD inputs while in diagnostic loopback.

Diagnostic Loopback Enable [DLEB]. TTL. Selects diagnostic loopback. When DLEB is high, the S3012 device uses the primary data (RSD) input. When low, the S3012 device uses the diagnostic loopback data (DLD) input, and the LOS signal is disabled.

Test Clock Enable [TESTEN]. TTL. Set high to provide access to the PLL during production tests.

Out of Frame [OOF]. TTL. Indicator used to enable framing pattern detection logic in the S3012. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set low, whichever is longer. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. (See Figures 13 and 14.)

Loss of Signal [LOS]. PECL. Active low. A single-ended 10K ECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When LOS is low, the data on the Serial Data In (RSDP/N) pins will be internally forced to a constant zero, LOCKDET forced low, and the PLL forced to lock to the REFCKINP/N inputs. When DLEB is low, LOCKDET remains high if there are transitions on DLDP/N for either state of LOS.

This signal must be used to assure correct automatic reacquisition to serial data following an interruption and subsequent reconnection of the optical path. This will assure that the PLL does not "wander" out of reacquisition range by tracking the random phase/frequency content of the optical detector's noise floor while monitoring "dark" fiber.

When LOS is high, data on the RSDP/N pins will be processed normally.

Reference Clock [REFCLK]. TTL. Input normally used as the reference for the integral clock recovery PLL.

Test Reset [TESTRST]. TTL. Used to reset portions of the clock recovery PLL during production testing. Held low for normal operation.

Master Reset [RSTB]. TTL. Reset input for the device, active low. Initializes the device to a known state and forces the PLL to acquire to the reference clock. A reset of at least 16 ms should be applied at power-up and whenever the user wishes to force the PLL to re-acquire to the reference clock. The S3012 will also re-acquire to the reference clock if the serial data input is held quiescent for at least 16 ms.

Loop Filter Capacitor [CAP1, CAP2]. The loop filter capacitor is connected to these pins. The capacitor value should be 0.1 μ f \pm 10% tolerance, X7R dielectric. 50 volt is recommended (16 volt is acceptable).

Output Signals

Parallel Output [POUT]<7:0>. TTL/CMOS. Parallel data bus, a 19.44 Mbyte/sec word, aligned to the parallel output clock (POCLK). POUT<7> is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT<0> is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). POUT<7:0> is updated on the falling edge of POCLK.

Frame Pulse [FP]. TTL/CMOS. Indicates frame boundaries in the incoming data stream (RSD). If framing pattern detection is enabled, as controlled by the OOF input, FP pulses high for one POCLK cycle when a 48 bit sequence matching the framing pattern is detected on the RSD inputs. When framing pattern detection is disabled, FP pulses high when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK.

Parallel Output Clock [POCLK]. TTL/CMOS. A 19.44 MHz nominally 50% duty cycle, byte rate output clock, that is aligned to POUT<7:0> byte serial output data. POUT<7:0> and FP are updated on the falling edge of POCLK.

Lock Detect [LOCKDET]. TTL. Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming data stream. LOCKDET is an asynchronous output.

OTHER OPERATING MODES

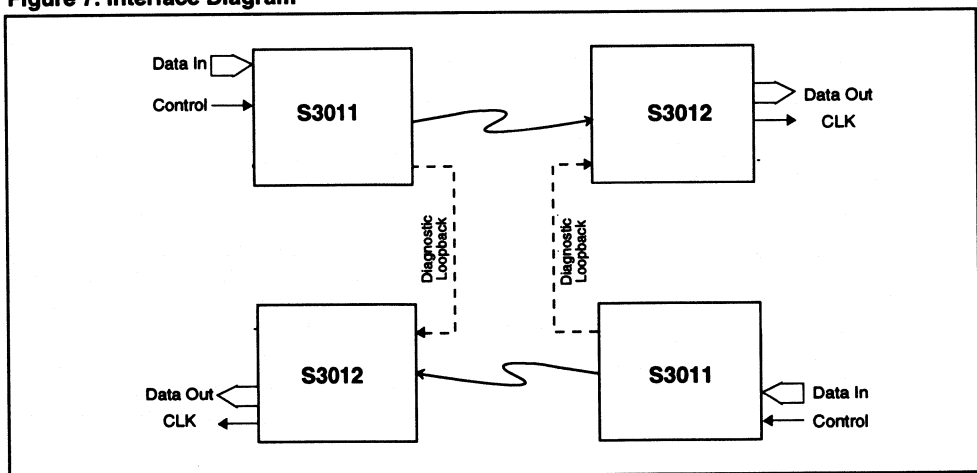
Diagnostic Loopback

The Diagnostic Loopback consists of alternate serial data outputs (in the case of the S3011) and inputs (in the case of the S3012).

On the S3011, the differential PECL output DLD provides Diagnostic Loopback serial data. When the Diagnostic Loopback Enable (DLEB) input and TSCLKSEL are low, this data output is a replica of TSD. When DLD is connected to the S3012, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. When DLEB is high and TSCLKSEL is low, DLD is held in the inactive state, with the positive output high and the negative output low. In the inactive state, there will be no interference from the transmitter to the receiver.

On the receiver side, the differential PECL input DLD is the Diagnostic Loopback serial data input. When the Diagnostic Loopback Enable (DLEB) input is set low, the DLD input is routed in place of the normal data stream (RSD).

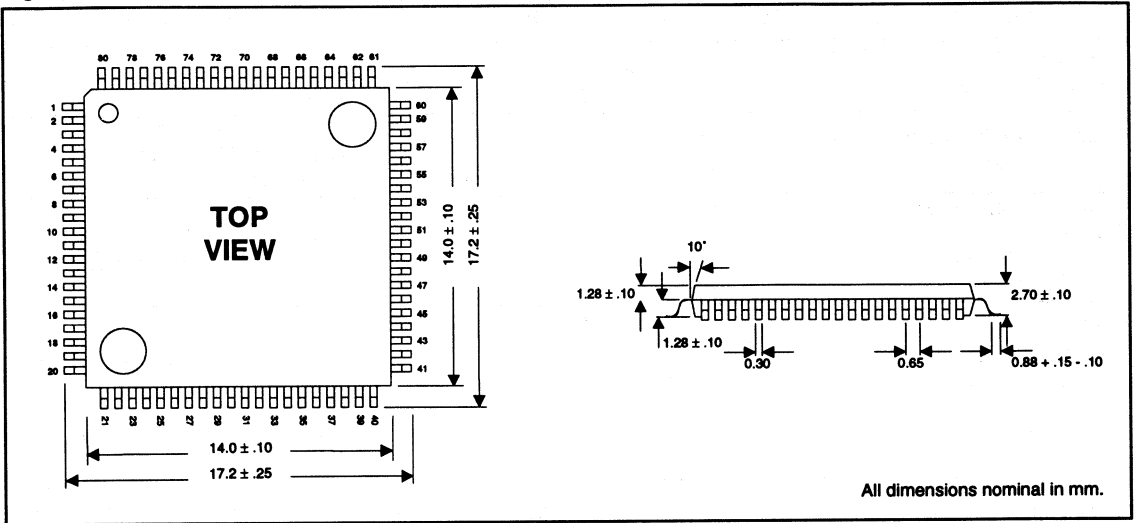
Figure 7. Interface Diagram



Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	
PECL Data Output Jitter OC-3/STS-3			64	ps (rms)	In CSU mode, given 56 ps rms jitter on REFCLK in 12KHz to 1 MHz band
Reference Clock Frequency Tolerance ¹ Clock Synthesis Clock Recovery	-20 -100		+20 +100	ppm ppm	Required to meet SONET/ATM output frequency specification
OC-3/STS-3 Capture Range Lock Range Clock Output Duty Cycle	48	±200ppm +8%, -12%	52	% of UI	With respect to fixed reference frequency Minimum transition density of 20%
Acquisition Lock Time			64.0	μsec	With device already powered up and valid REFCLK
Reference Clock Input Duty Cycle	30		70	% of period	
Reference Clock Rise & Fall Times			5.0	ns	10% to 90% of amplitude
PECL Output Rise & Fall Times			600	ps	20% to 80%, 50Ω to VCC -2 equivalent load, 5 pf cap

Figure 8. 80-pin PQFP Package



ABSOLUTE MAXIMUM RATINGS

PARAMETER	Min	Typ	Max	Unit
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Respect to GND	-0.5		+7.0	V
Voltage on Any TTL Input Pin	-0.5		+5.5	V
Voltage on Any PECL Input Pin	VCC-3		VCC	V
TTL Output Sink Current			20	mA
TTL Output Source Current			10	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage		500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	Min	Typ	Max	Unit
Ambient Temperature under Bias	0		70	°C
Junction Temperature under Bias	20		125	°C
Voltage on VCC with Respect to GND	4.75	5.0	5.25	V
Voltage on Any TTL Input Pin	0		VCC	V
Voltage on Any PECL Input Pin	VCC-2		VCC	V
S3011 ICC			210	mA
S3012 ICC			270	mA

TTL/CMOS INPUT/OUTPUT DC CHARACTERISTICS
 $(T_A = 0^\circ\text{C to } +70^\circ\text{C}, V_{CC} = 5\text{ V } \pm 5\%)$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}^1	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}^1	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
I_{IL}	Input LOW Current	-400.0			μA	$V_{CC} = \text{MAX}, V_{IN} = 0.5\text{V}$
I_{IH}	Input HIGH Current			50.0	μA	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$
I_I	Input HIGH Current at Max VCC			1.0	mA	$V_{CC} = \text{MAX}, V_{IN} = 5.5\text{V}$
I_{OS}	Output Short Circuit Current	-100.0		-25.0	mA	$V_{CC} = \text{MAX}, V_{OUT} = 0.5\text{V}$
V_{IK}	Input Clamp Diode Voltage	-1.2			Volts	$V_{CC} = \text{MIN}, I_{IN} = -18\text{ ma}$
V_{OL}	Output LOW Voltage			0.5	Volts	$V_{CC} = \text{MIN}, I_{OL} = 8\text{ ma}$
V_{OH}	Output HIGH Voltage	2.7			Volts	$V_{CC} = \text{MIN}, I_{OH} = -1\text{ ma}$

1. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

PECL INPUT/OUTPUT DC CHARACTERISTICS^{1,2}
 $(T_A = 0^\circ\text{C to } +70^\circ\text{C}, V_{CC} = 5\text{ V } \pm 5\%)$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}	Input LOW Voltage	$V_{CC} - 2.000$		$V_{CC} - 1.450$	Volts	Guaranteed Input LOW Voltage for single-ended inputs
V_{IH}	Input HIGH Voltage	$V_{CC} - 1.180$		$V_{CC} - 0.600$	Volts	Guaranteed Input HIGH Voltage for single-ended inputs
V_{IL}	Input LOW Voltage	$V_{CC} - 2.000$		$V_{CC} - 0.700$	Volts	Guaranteed Input LOW Voltage for differential inputs
V_{IH}	Input HIGH Voltage	$V_{CC} - 1.750$		$V_{CC} - 0.450$	Volts	Guaranteed Input HIGH Voltage for differential inputs
V_{ID}	Input Diff. Voltage	0.250	0.500	1.400	Volts	Differential Input Voltage
I_{IH}	Input High Current	-0.500		20.000	μA	$V_{ID} = 500\text{mV}$
I_{IL}	Input Low Current	-0.500		20.000	μA	$V_{ID} = 500\text{mV}$
V_{OL}	Output LOW Voltage	$V_{CC} - 2.000$		$V_{CC} - 1.565$	Volts	50 ohm termination to $V_{CC} - 2\text{V}$
V_{OH}	Output HIGH Voltage	$V_{CC} - 1.070$		$V_{CC} - 0.695$	Volts	50 ohm termination to $V_{CC} - 2\text{V}$
V_{OD}	Output Diff. Voltage	0.495		1.305	Volts	Differential Output Voltage

1. These conditions will be met with no airflow.
2. When not used, tie the positive differential PECL pin to V_{CC} and the negative differential ECL pin to ground via a 3.9K resistor.

3

S3011 TRANSMITTER PINOUT

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	GND	21	GND	41	GND	61	GND
2	GND	22	GND	42	GND	62	GND
3	CAP1	23	TTL VCC	43	IOGND	63	N.C.
4	AGND3	24	ECLIO VCC	44	PAE	64	AGND0
5	A+5V3	25	PIN1	45	SYNC	65	N.C.
6	TESTEN	26	PIN2	46	TSCLKSEL	66	A+5V0
7	+5V	27	+5V	47	+5V	67	DLDN
8	GND	28	PIN3	48	GND	68	N.C.
9	N.C.	29	GND	49	N.C.	69	DLDP
10	PCLK	30	PIN4	50	DLEB	70	N.C.
11	N.C.	31	PIN5	51	TESTRST	71	TSDN
12	N.C.	32	GND	52	N.C.	72	AGND4
13	GND	33	N.C.	53	GND	73	TSDP
14	+5V	34	+5V	54	+5V	74	A+5V4
15	RSTB	35	PIN6	55	N.C.	75	REFCLK
16	PICK	36	PIN7	56	A+5V1	76	TGND
17	PIN0	37	ECLIO VCC	57	AGND1	77	N.C.
18	IO GND	38	TTL VCC	58	N.C.	78	CAP2
19	GND	39	GND	59	GND	79	GND
20	GND	40	GND	60	GND	80	GND

S3012 RECEIVER PINOUT

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	GND	21	GND	41	GND	61	GND
2	GND	22	GND	42	GND	62	GND
3	CAP1	23	TTL VCC	43	IOGND	63	RSDP
4	AGND3	24	ECLIO VCC	44	POUT0	64	AGND0
5	A+5V3	25	POUT5	45	POCLK	65	RSDN
6	TESTEN	26	POUT4	46	ITPWR	66	A+5V0
7	+5V	27	+5V	47	+5V	67	DLDP
8	GND	28	POUT3	48	GND	68	AGND2
9	LOS	29	GND	49	TESTRST	69	DLDN
10	OOF	30	ITGND	50	RSTB	70	A+5V2
11	ITGND	31	ITPWR	51	DLEB	71	N.C.
12	FP	32	GND	52	LOCKDET	72	N.C.
13	GND	33	ITGND	53	GND	73	N.C.
14	+5V	34	+5V	54	+5V	74	N.C.
15	ITGND	35	POUT2	55	N.C.	75	REFCLK
16	POUT7	36	POUT1	56	A+5V1	76	TGND
17	POUT6	37	ECLIO VCC	57	AGND1	77	N.C.
18	IO GND	38	TTL VCC	58	N.C.	78	CAP2
19	GND	39	GND	59	GND	79	GND
20	GND	40	GND	60	GND	80	GND

Power Supply Connections:

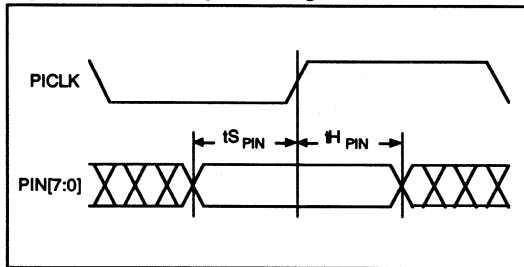
A+5V0, A+5V1, A+5V2, A+5V3, A+5V4	=	ANALOG+5V
AGND0, AGND1, AGND2, AGND3, AGND4	=	ANALOG 0V
+5V, TTLVCC, ECLIOVCC, ITPWR	=	DIGITAL +5V
GND, IOGND, TGND, ITGND	=	DIGITAL 0V
N.C.	=	NOT CONNECTED

Table 2. S3011 AC Timing Characteristics

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

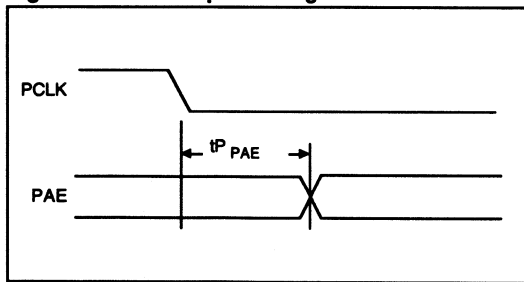
Symbol	Description	Min	Max	Units
	TCLK Frequency		156	MHz
	TCLK Duty Cycle	40	60	%
t_{SPIN}	PIN [7:0] Set-up Time w.r.t. PCLK	5		ns
t_{HPIN}	PIN [7:0] Hold Time w.r.t. PCLK	5		ns
$t_{P_{PAE1}}$	PCLK Low to PAE Valid Propagation Delay		10	ns
	PCLK Duty Cycle	35	65	%

Figure 9. PIN AC Input Timing



1. When a set-up time is specified on TTL signals between an input and a clock, the set-up time is the time in nanoseconds from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on TTL signals between an input and a clock, the hold time is the time in nanoseconds from the 50% point of the clock to the 50% point of the input.

Figure 10. PAE Output Timing



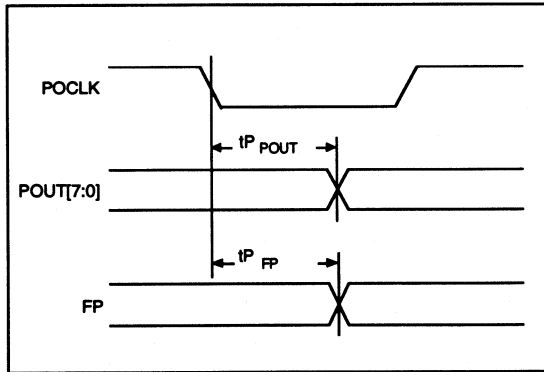
Notes on TTL Output Timing

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays are measured with a 15 pF load on the outputs.

Table 3. S3012 AC Timing Characteristics

Symbol	Description	Min	Max	Units
	POCLK Duty Cycle	40	60	%
tP_{POUT}	POCLK Low to POUT[7:0] Valid Prop. Delay		15	ns
tP_{FP}	POCLK Low to FP Valid Propagation Delay		15	ns
	RSD Minimum Pulse Width	1.6		ns

Figure 11. Output Timing Diagram



Notes on Output Timing:

1. Output propagation delay time of TTL outputs is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays of TTL outputs are measured with a 15 pF load and 500 ohms to ground on the outputs.

RECEIVER FRAMING

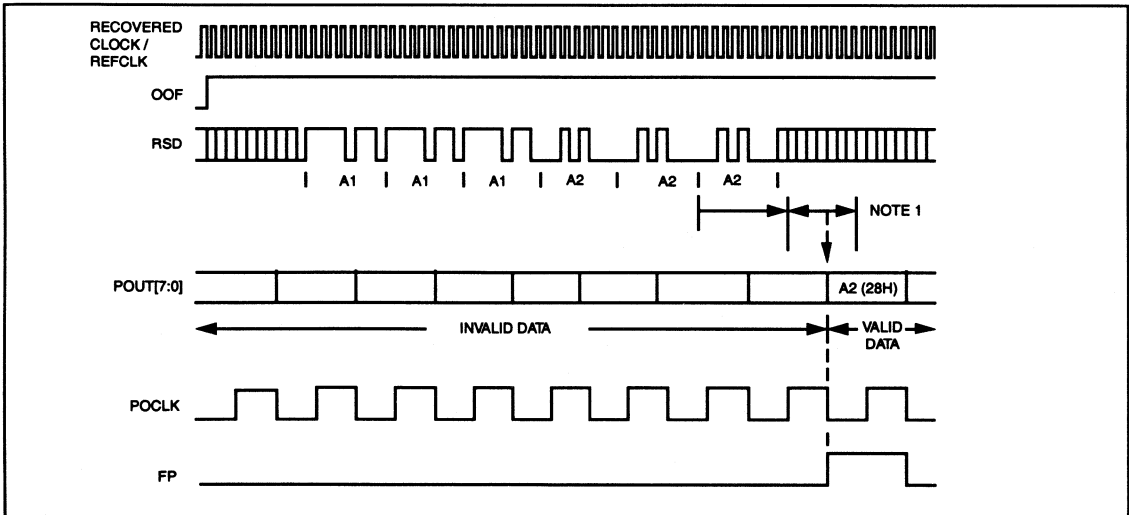
Figure 12 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is high. Both boundaries are recognized upon receipt of the third A2 byte which is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUT[7:0]). Concurrently, the frame pulse is set high for one POCLK cycle.

When interfacing with a section terminating device, the OOF input remains high for one full frame after the first frame pulse while the section terminating device verifies internally that the frame and byte alignment are correct, as shown in Figure 13. Since at least one framing pattern has been detected since the rising edge of OOF, boundary detection is disabled when OOF is set low.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse or until OOF goes low, whichever occurs last. Figure 13 shows a typical OOF timing pattern which occurs when the S3012 is connected to a down stream section terminating device. OOF remains high for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes low.

Figure 14 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 12. Frame and Byte Detection



NOTE 1: Range of input to output delay can be 1.5 to 2.5 POCLK cycles

Figure 13. OOF Operation Timing with SSTX

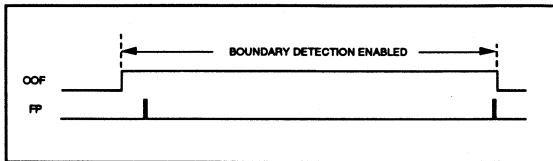
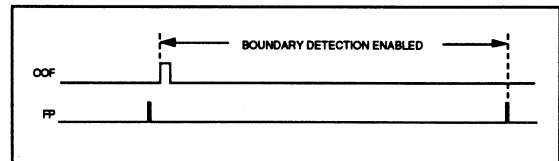


Figure 14. Alternate OOF Timing



Ordering Information

GRADE	TRANSMITTER	PACKAGE
S – commercial	3011	A – 80 PQFP

GRADE	RECEIVER	PACKAGE
S – commercial	3012	A – 80 PQFP

X XXXX X
Grade Part number Package

FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLL for clock generation and clock recovery
- Supports 622.08 Mbit/s (OC-12/STM-4)
- Reference frequencies of 19.44 and 77.76 MHz
- Interface to both PECL and TTL logic
- 8-bit TTL datapath
- Compact 52 PQFP TEP package
- Diagnostic loopback mode
- Lock detect
- Low jitter PECL interface
- < 2.0 Watt per set typically

APPLICATIONS

- ATM adapter cards
- ATM switches, hubs, routers
- ATM over SONET/SDH
- ATM test equipment
- Fiber optic terminators
- Fiber optic test equipment

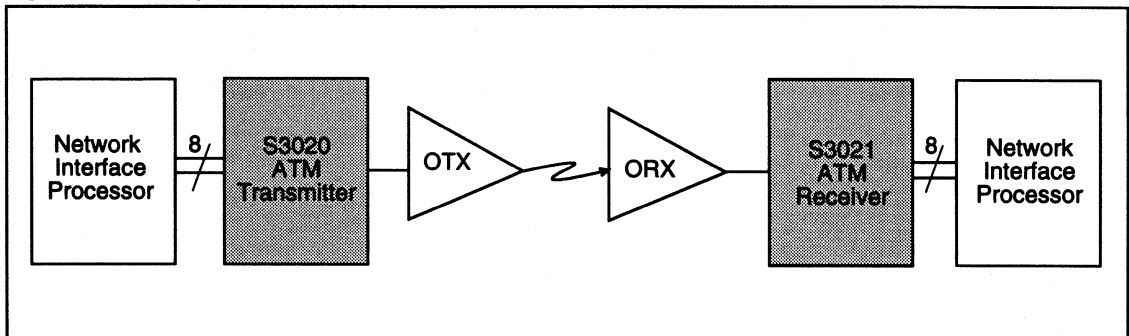
GENERAL DESCRIPTION

The S3020/S3021 ATM transmitter and receiver chips are fully integrated serialization/deserialization ATM 622 Mbit/s interface devices. The chipset performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with ATM transmission standards. The devices are suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3020 transmitter chip allowing the use of a slower external transmit clock reference. Clock recovery is performed on the S3021 receiver chip by synchronizing its on-chip VCO directly to the incoming data stream. The S3021 also performs ATM frame detection. The chipset can be used with a 19.44 or 77.76 MHz reference clock, in support of existing system clocking schemes.

The low jitter PECL interface guarantees compliance with the bit-error rate requirements of the Bellcore, ANSI, and ITU-T standards. The S3020 and S3021 are packaged in a compact 52 PQFP, offering designers a small package outline.

Figure 1. Link Diagram



S3020/S3021 OVERVIEW

The S3020 transmitter and S3021 receiver implement ATM serialization/deserialization, transmission, and frame detection/recovery functions. The block diagrams in Figures 2 and 3 show basic operation of both chips. These chips can be used to implement the front end of ATM equipment, which consists primarily of the serial transmit interface (S3020) and the serial receive interface (S3021). The chipset handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation and recovery, and system timing. The system timing circuitry consists of management of the datastream, framing, and clock distribution throughout the front end.

Operation of the S3020/S3021 chips is straightforward. The sequence of operations is as follows:

Transmitter

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver

1. Clock and data recovery from serial input
2. Frame detection
3. Serial-to-parallel conversion
4. 8-bit parallel output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 7 through 12.

A lock detect feature is provided on the S3021, which indicates that the PLL is locked (synchronized) to the data stream, and facilitates continuous down-stream clocking in the absence of data.

Suggested Interface Devices

PMC PM5312	STTX	SONET/SDH Transport Term.	Transceiver
PMC PM5355	SUNI-622	Saturn User Network Interface	
AT&T ASTROTEC 1227/1230		650 Mbit/s	Fiber Optic Transmitter
Mitsubishi MF-622DF-T12-XXX		622 Mbit/s	Fiber Optic Transmitter
Sumitomo ES-9304-TD		622 Mbit/s	Fiber Optic Transmitter
AT&T ASTROTEC 1310		650 Mbit/s	Fiber Optic Receiver
Mitsubishi MF-622DS-R1X-XXX		622 Mbit/s	Fiber Optic Receiver
Sumitomo ES-9216-RD		622 Mbit/s	Fiber Optic Receiver
Finisar		1000 Mbit/s	Fiber Optic Transceiver

Figure 2. S3020 Transmitter

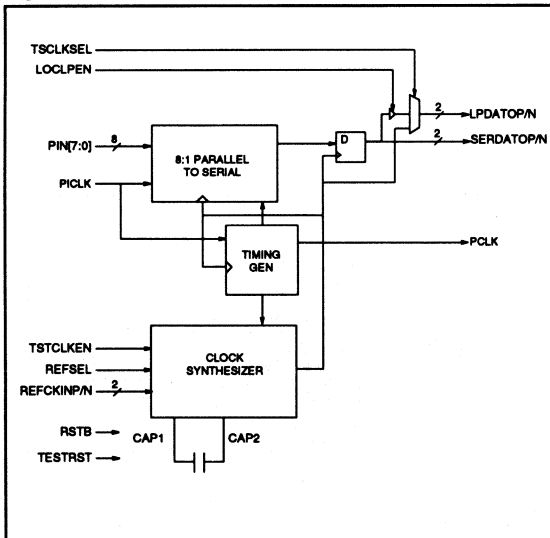
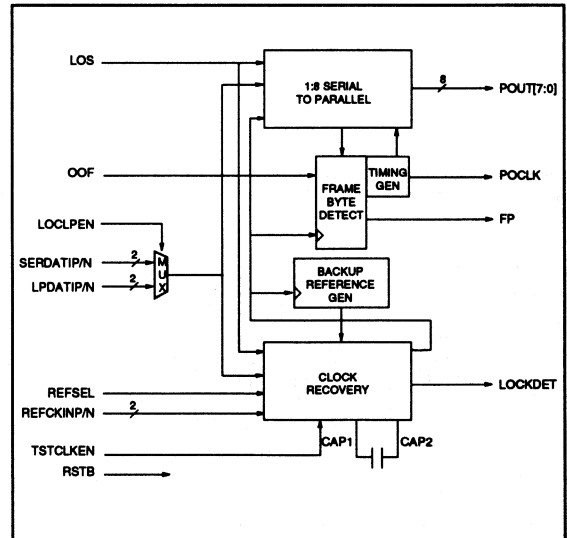


Figure 3. S3021 Receiver



S3020 TRANSMITTER ARCHITECTURE/FUNCTIONAL DESIGN

The S3020 transmitter chip performs the serializing stage in the processing of a transmit ATM 622 Mbit/s serial data stream. It converts the byte serial 77.76 Mbyte/sec data stream to bit serial format at 622.08 Mbit/sec.

A high-frequency bit clock can be generated from a 19.44 MHz or a 77.76 MHz frequency reference by using an integral frequency synthesizer consisting of a phase-locked loop circuit with a divider in the loop.

Diagnostic loopback is provided (transmitter to receiver) when used with the compatible S3021. (See Other Operating Modes.)

Clock Synthesizer

The Clock Synthesizer, shown in the block diagram in Figure 2, is a monolithic PLL that generates the serial output clock phase synchronized with the input reference clock (REFCKINP/N).

The REFCKINP/N input must be generated from a differential PECL crystal oscillator which has a frequency accuracy of better than 20 ppm in order for the TSCLK frequency to have the accuracy required for operation in an ATM system.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCKINP/N input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

Timing Generator

The Timing Generation function, seen in Figure 2, provides a byte rate version of the transmit serial clock. This circuitry also provides an internally generated load signal, which transfers the PIN[7:0] data from the parallel input register to the serial shift register.

The PCLK output is a byte rate version of transmit serial clock at 77.76 MHz. PCLK is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3020 device.

Parallel-to-Serial Converter

The Parallel-to-Serial converter shown in Figure 2 is comprised of two byte-wide registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PCLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

The load signal, which latches the data from the parallel to the serial shift register, has a fixed relationship to PCLK. If PCLK is tied to PCLK, the PIN[7:0] data latched into the parallel register will meet the timing specifications with respect to the load signal. If PCLK is not tied to PCLK, the delay must meet the timing requirements shown in Figure 7, and PCLK must be frequency locked to the reference clock input.

TRANSMITTER PIN DESCRIPTIONS**Input Signals**

Parallel Data Input [PIN]<7:0>. TTL. A 77.76 Mbyte/sec word, aligned to the PCLK parallel input clock. PIN<7> is the most significant bit (corresponding to the first bit transmitted). PIN<0> is the least significant bit (corresponding to the last bit transmitted). PIN<7:0> is sampled on the rising edge of PCLK.

Parallel Input Clock [PCLK]. TTL. A 77.76 MHz nominally 50% duty cycle input clock, to which PIN<7:0> is aligned. PCLK is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PCLK samples PIN<7:0>.

Test Clock Enable [TSTCLKEN]. TTL. Active High. Enables the reference clock to be used in place of the VCO for testing. Allows a means of testing the functions of the chip without the use of the PLL. Set low for normal operation.

Reference Clock [REFCKINP/N]. Differential PECL. Input used as the reference for the internal bit clock frequency synthesizer.

Local Loopback Enable [LOCLPEN]. TTL. Enables the LPDATO output when low and TSCLKSEL is low. When LOCLPEN is high, the LPDATO output is held in the inactive state to prevent interference between the transmit and receive devices.

Master Reset [RSTB]. TTL. Reset input for the device, active low. During reset, PCLK does not toggle.

Transmit Clock Select [TSCLKSEL]. TTL. Active high input which when enabled directs the transmit serial clock through the LPDATOP/N output.

Test Reset [TESTRST]. TTL. Used to reset portions of the clock recovery PLL during production testing. Held low for normal operation.

Reference Select [REFSEL]. TTL. Used to select the reference clock frequency. Set low to select 77.76 MHz. Set high to select 19.44 MHz.

Loop Filter Capacitor [CAP1, CAP2]. The loop filter capacitor is connected to these pins. The capacitor value should be 0.01 μ f \pm 10% tolerance, X7R dielectric. 50 volt is recommended (16 volt is acceptable).

Output Signals

Serial Data Out [SERDATOP/N]. High-speed, source-terminated differential PECL. Serial data stream signals, normally connected to an optical transmitter module.

Loopback Data [LPDATOP/N]. Differential PECL. Serial data stream signals, normally connected to a companion S3021 device for diagnostic loopback purposes. They are held inactive when LOCLPEN is high and TSCLKSEL is low. The serial data stream is output when LOCLPEN is low and TSCLKSEL is low. When enabled by the TSCLKSEL input the transmit serial clock will be output through this pin. The transmit serial clock is a buffered version of the internal frequency synthesizer clock, which is phase-aligned with the SERDATO output signal. The SERDATO is updated on the falling edge of the transmit serial clock.

Parallel Clock [PCLK]. TTL. A reference clock generated by dividing the internal bit clock by eight. It is normally used to coordinate byte-wide transfers between upstream logic and the S3020 device.

S3021 RECEIVER ARCHITECTURAL/FUNCTIONAL DESIGN

The S3021 receiver chip provides the first stage of digital processing of a receive ATM 622 Mbit/s bit-serial stream. It converts the bit-serial 622.08 Mbit/sec data stream into a 77.76 Mbyte/sec byte-serial data format.

Clock recovery is performed on the incoming scrambled NRZ data stream. A 77.76 MHz reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference to the nominal bit rate.

A loopback mode is provided for diagnostic loopback (transmitter to receiver), when used with the compatible S3020 device.

Clock Recovery

The Clock Recovery PLL, as shown in the block diagram in Figure 3, generates a clock that is at the same frequency as the incoming data bit rate at the SERDATI or LPDATI inputs. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock. Frequency stability without incoming data is guaranteed by an alternate reference input (REFCKIN) that the PLL locks onto when data is lost.

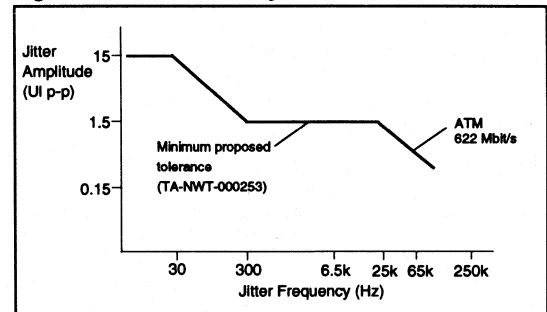
The clock recovery circuit monitors the incoming data stream for loss of signal. If the incoming data stream has had no transitions for between 96 and 224 bit times (depending upon the state of an internal counter at the time of last transition), loss of signal is declared and the PLL will switch from locking onto the incoming data to locking onto the reference clock. Alternatively, the loss-of-signal (LOS) input can be used to force a loss-of-signal condition. When set low, LOS squelches the incoming data stream, and thus causes the PLL to switch its source of reference within 128 bit times afterwards. Loss-of-signal condition is removed when LOS is high, and good data, with acceptable pulse density and run length, returns on the incoming data stream.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received ATM data signal. This transfer function yields a typical capture

time of 16 μ s for random incoming NRZ data. A single external clean-up capacitor is utilized as part of the loop filter.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which meets, with ample margin, the minimum tolerance proposed by the Bellcore TA-NWT-000253 standard, shown in Figure 4.

Figure 4. Clock Recovery Jitter Tolerance



Backup Reference Generator

The Backup Reference Generator seen in Figure 3 provides backup reference clock signals to the clock recovery block when the clock recovery block detects a loss of signal condition. It contains a counter that divides the clock output from the clock recovery block down to the same frequency as the reference clock REFCKINP/N.

Frame and Byte Boundary Detection

The Frame and Byte Boundary Detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. Framing pattern detection is enabled and disabled by the out-of-frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration that OOF is set high. It is disabled when a framing pattern is detected and OOF is no longer set high. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (SERDATI or LPDATI). The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). The frame boundary is reported on the frame pulse (FP) output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an ATM 622 Mbit/s stream will generate the 48-bit framing pattern is extremely small. It is highly improbable that a mimic pattern would occur within one frame of data. Therefore, the time to match the first frame pattern and to verify it with down-stream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 μ s, even for extremely high bit error rates.

Once down-stream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input can be set low to disable the frame search process from trying to synchronize to a mimic frame pattern.

Serial-to-Parallel Converter

The Serial-to-Parallel Converter consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the clock recovery block. The second is an 8-bit internal holding register, which transfers data from the serial-to-parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the Serial-to-Parallel converter can vary from 1.5 to 2.5 byte periods (12 to 20 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries, with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial to parallel converter is that POCLK is neither truncated nor extended during reframe sequences.

S3021 RECEIVER PIN DESCRIPTIONS

Input Signals

Receive Serial Data [SERDATIP/N]. Differential PECL. Serial data stream signals normally connected to an optical receiver module. A clock is recovered from transitions on the SERDATI inputs.

Diagnostic Loopback Data [LPDATIP/N]. Differential PECL. Serial data stream signal, normally connected to a companion S3020 device for diagnostic loopback purposes. Clock is recovered from transitions on the LPDATI inputs while in diagnostic loopback.

Local Loopback Enable [LOCLPEN]. TTL. Selects diagnostic loopback. When LOCLPEN is high, the S3021 device uses the primary data (SERDATI) input. When low, the S3021 device uses the diagnostic loopback data (LPDATI) input.

Test Clock Enable [TSTCLKEN]. TTL. Active High. Enables the reference clock to be used in place of the VCO for testing. Allows a means of testing the functions of the chip without the use of the PLL. Set low for normal operation.

Out of Frame [OOF]. TTL. Indicator used to enable framing pattern detection logic in the S3021. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set low, whichever is longer. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. (See Figures 11 and 12.)

Loss of Signal [LOS]. PECL. Active low. A single-ended 10K ECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When LOS is low, the data on the Serial Data In (SERDATIP/N) pins will be internally forced to a constant zero, LOCKDET will be forced low, and the PLL will lock to the REFCKINP/N inputs.

This signal must be used to assure correct automatic reacquisition to serial data following an interruption and subsequent reconnection of the optical path. This will assure that the PLL does not "wander" out of reacquisition range by tracking the random phase/frequency content of the optical detector's noise floor while monitoring "dark" fiber.

When LOS is high, data on the SERDATIP/N pins will be processed normally.

Reference Clock [REFCKINP/N]. Differential PECL. Input normally used as the reference for the integral clock recovery PLL.

Master Reset [RSTB]. TTL. Reset input for the device, active low. Initializes the device to a known state and forces the PLL to acquire to the reference clock. A reset of at least 16 ms should be applied at power-up and whenever the user wishes to force the PLL to re-acquire to the reference clock. The S3021 will also re-acquire to the reference clock if the serial data input is held quiescent for at least 16 ms.

Reference Select [REFSEL]. TTL. Used to select the reference clock frequency. Set low to select 77.76 MHz. Set high to select 19.44 MHz.

Loop Filter Capacitor [CAP1, CAP2]. The loop filter capacitor is connected to these pins. The capacitor value should be 0.1 μ f \pm 10% tolerance, X7R dielectric. 50 volt is recommended (16 volt is acceptable).

Output Signals

Parallel Output [POUT]<7:0>. TTL. Parallel data bus, a 77.76 Mbyte/sec word, aligned to the parallel output clock (POCLK). POUT<7> is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT<0> is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). POUT<7:0> is updated on the falling edge of POCLK.

Frame Pulse [FP]. TTL. Indicates frame boundaries in the incoming data stream (SERDATI). If framing pattern detection is enabled, as controlled by the OOF input, FP pulses high for one POCLK cycle when a 48 bit sequence matching the framing pattern is detected on the serial data inputs. When framing pattern detection is disabled, FP pulses high when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK.

Parallel Output Clock [POCLK]. TTL. A 77.76 MHz nominally 50% duty cycle, byte rate output clock, that is aligned to POUT<7:0> byte serial output data. POUT<7:0> and FP are updated on the falling edge of POCLK.

Lock Detect [LOCKDET]. TTL. Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming data stream. LOCKDET is an asynchronous output.

OTHER OPERATING MODES

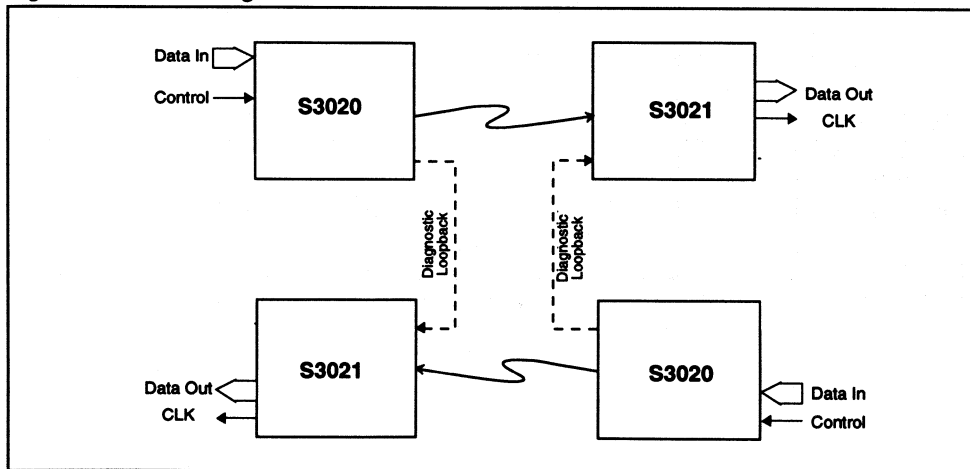
Diagnostic Loopback

The Diagnostic Loopback consists of alternate serial data outputs (in the case of the S3020) and inputs (in the case of the S3021).

On the S3020, the differential PECL output LPDATO provides Diagnostic Loopback serial data. When the Local Loopback Enable (LOCLPEN) input and TCLKSEL are low, this data output is a replica of SERDATO. When LPDATO is connected to the S3021, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. When LOCLPEN is high and TCLKSEL is low, LPDATO is held in the inactive state, with the positive output high and the negative output low. In the inactive state, there will be no interference from the transmitter to the receiver.

On the receiver side, the differential PECL input LPDATI is the Diagnostic Loopback serial data input. When the Local Loopback Enable (LOCLPEN) input is set low, the LPDATI input is routed in place of the normal data stream (SERDATI).

Figure 5. Interface Diagram



PERFORMANCE SPECIFICATIONS

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	
PECL Data Output Jitter OC-12/STS-12 ¹			16	ps (rms)	In CSU mode, given 14 ps rms jitter on REFCKIN in 12KHz to 5 MHz band. REFCLK = 77.76 MHz
Reference Clock Frequency Tolerance Clock Synthesis Clock Recovery	-20 -100		+20 +100	ppm ppm	Required to meet SONET/ATM output frequency specification
OC-12/STS-12 Capture Range Lock Range		±200ppm +2,-8%			With respect to fixed reference frequency Minimum transition density of 20%
Acquisition Lock Time			16	μsec	With device already powered up and valid reference clock
Reference Clock Input Duty Cycle	30		70	% of period	
Reference Clock Rise & Fall Times			2.0	ns	10% to 90% of amplitude
PECL Output Rise & Fall Times (S3020 LPDATOP/N)			600	ps	20% to 80%, 50 Ω to Vcc -2V equivalent load, 5pF cap
Source Terminated Diff. PECL Compatible Output Rise & Fall Times (S3020 SERDATOP/N)			450	ps	20% to 80%, 100 Ω line to line

1. For REFCLK = 19.44 MHz, multiply the specified value by three.

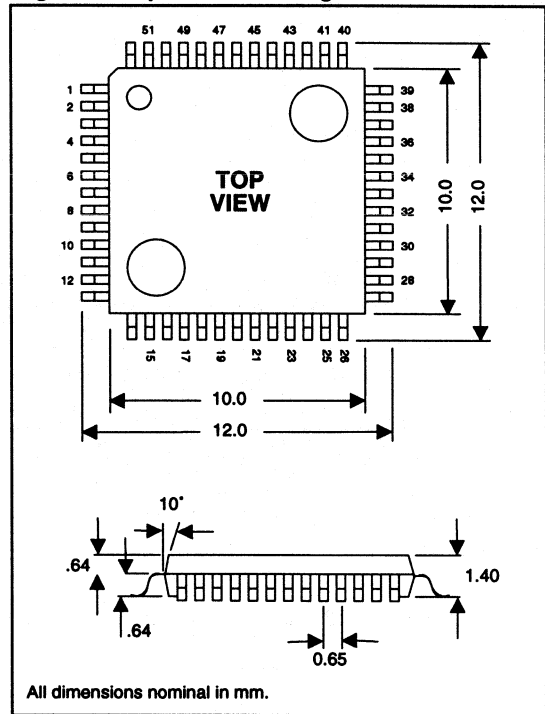
ABSOLUTE MAXIMUM RATINGS

PARAMETER	Min	Typ	Max	Unit
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Respect to GND	-0.5		+7.0	V
Voltage on Any TTL Input Pin	-0.5		+5.5	V
Voltage on Any PECL Input Pin	VCC -3		VCC	V
TTL Output Sink Current			20	mA
TTL Output Source Current			10	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage		500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	Min	Typ	Max	Unit
Ambient Temperature under Bias	0		70	°C
Junction Temperature under Bias	20		125	°C
Voltage on VCC with Respect to GND	4.75	5.0	5.25	V
Voltage on Any TTL Input Pin	0		VCC	V
Voltage on Any PECL Input Pin	VCC -2		VCC	V
S3020 ICC		178	238	mA
S3021 ICC		216	270	mA

Figure 6. 52-pin PQFP Package



3

TTL INPUT/OUTPUT DC CHARACTERISTICS

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}^1	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}^1	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
I_{IL}	Input LOW Current	-400.0			μA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.5\text{V}$
I_{IH}	Input HIGH Current			50.0	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7\text{V}$
I_I	Input HIGH current at Max. VCC			1.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 5.25\text{V}$
I_{OS}	Output Short Circuit Current	-100.0		-25.0	mA	$V_{CC} = \text{MAX}$, $V_{OUT} = 0.5\text{V}$
V_{IK}	Input Clamp Diode Voltage	-1.2			Volts	$V_{CC} = \text{MIN}$, $I_{IN} = -18\text{ ma}$
V_{OL}	Output LOW Voltage			0.5	Volts	$V_{CC} = \text{MIN}$, $I_{OL} = 8\text{ ma}$
V_{OH}	Output HIGH Voltage	2.7			Volts	$V_{CC} = \text{MIN}$, $I_{OH} = -1\text{ ma}$

1. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

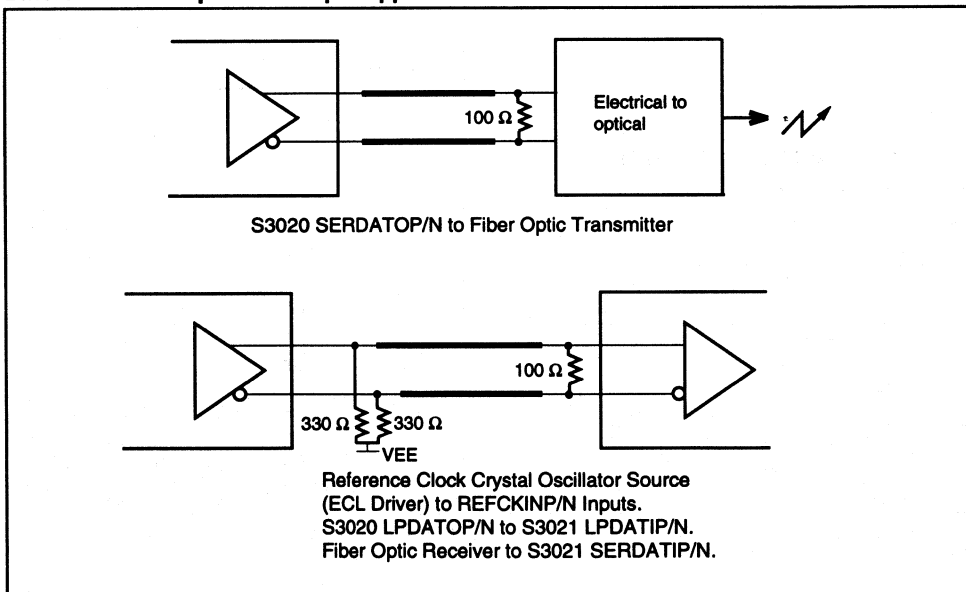
PECL INPUT/OUTPUT DC CHARACTERISTICS^{1,2}

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}	Input LOW Voltage	$V_{CC} - 2.000$		$V_{CC} - 1.441$	Volts	Guaranteed Input LOW Voltage for single-ended inputs
V_{IH}	Input HIGH Voltage	$V_{CC} - 1.225$		$V_{CC} - 0.570$	Volts	Guaranteed Input HIGH Voltage for single-ended inputs
V_{iL}	Input LOW Voltage	$V_{CC} - 2.000$		$V_{CC} - 0.700$	Volts	Guaranteed Input LOW Voltage for differential inputs
V_{iH}	Input HIGH Voltage	$V_{CC} - 1.750$		$V_{CC} - 0.450$	Volts	Guaranteed Input HIGH Voltage for differential inputs
V_{ID}	Input Diff. Voltage	0.250	0.500	1.400	Volts	Differential Input Voltage
I_{IH}	Input High Current	-0.500		20.000	μA	$V_{ID} = 500\text{mV}$
I_{iL}	Input Low Current	-0.500		20.000	μA	$V_{iD} = 500\text{mV}$
V_{OL}	Output LOW Voltage	$V_{CC} - 2.000$		$V_{CC} - 1.500$	Volts	50 ohm termination to $V_{CC} - 2\text{V}$
V_{OH}	Output HIGH Voltage	$V_{CC} - 1.110$		$V_{CC} - 0.670$	Volts	50 ohm termination to $V_{CC} - 2\text{V}$
V_{OD}	Output Diff. Voltage	0.390		1.330	Volts	Differential Output Voltage

1. These conditions will be met with no airflow.
2. When not used, tie the positive differential PECL pin to V_{CC} and the negative differential ECL pin to ground via a 3.9K resistor.

Differential ECL Input and Output Applications



S3020 Pinouts

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	CAP1	14	TTLVCC	27	TTLGND	40	AVCC0
2	AVEE3	15	ECLVCC	28+	ECLVCC	41	AVEE0
3	AVCC3	16	PCLK	29	PIN4	42	AVEE2
4	TSTCLKEN	17	TTLGND	30	PIN5	43	LPDATON
5	ECLVCC	18	ECLVEE	31	PIN6	44	LPDATOP
6	ECLVEE	19	PIN0	32	ECLVEE	45	SERDATON
7	REFSEL	20	PIN1	33	PIN7	46	AVCC2
8	LOCLPEN	21	ECLVEE	34	NC	47	SERDATOP
9	RSTB	22	PIN2	35	TSCLKSEL	48	REFCKINN
10	ECLVEE	23	PIN3	36	ECLVEE	49	REFCKINP
11	TESTRST	24	TTLVCC	37	ECLVCC	50	AVCC4
12	PICK	25	ECLVCC	38	AVCC1	51	AVEE4
13	TTLGND	26	TTLVCC	39	AVEE1	52	CAP2

S3021 Pinouts

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	CAP1	14	TTLVCC	27	TTLGND	40	AVCC0
2	AVEE3	15	ECLVCC	28	ECLVCC	41	AVEE0
3	AVCC3	16	POUT1	29	POUT6	42	LPDATIP
4	TSTCLKEN	17	TTLGND	30	POUT7	43	AVEE2
5	ECLVCC	18	ECLVEE	31	OOF	44	LPDATIN
6	ECLVEE	19	POUT2	32	ECLVEE	45	SERDATIP
7	REFSEL	20	POUT3	33	RSTB	46	SERDATIN
8	LOCLPEN	21	ECLVEE	34	LOS	47	AVCC2
9	POCLK	22	POUT4	35	LOCKDET	48	REFCKINN
10	ECLVEE	23	POUT5	36	ECLVEE	49	REFCKINP
11	FP	24	TTLVCC	37	ECLVCC	50	ECLVCC
12	POUT0	25	ECLVCC	38	AVCC1	51	NC
13	TTLGND	26	TTLVCC	39	AVEE1	52	CAP2

Power Supply Connections:

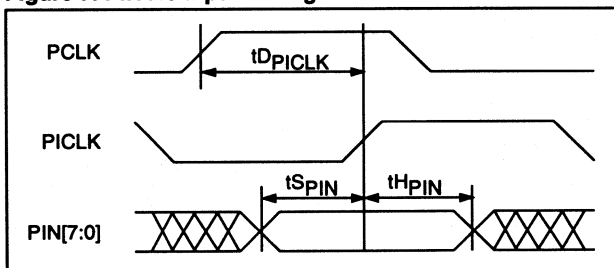
AVCC0, AVCC1, AVCC2, AVCC3, AVCC4	=	ANALOG+5V
AVEE0, AVEE1, AVEE2, AVEE3, AVEE4	=	ANALOG 0V
ECLVCC, TTLVCC	=	DIGITAL +5V
ECLVEE, TTLGND	=	DIGITAL 0V
N.C.	=	NOT CONNECTED

Table 1. S3020 AC Timing Characteristics

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Symbol	Description	Min	Typ	Max	Units
$t_{D_{PICKL}}$	PICKL Delay from PCLK	0		5.5	ns
$t_{S_{PIN}}$	PIN [7:0] Set-up Time w.r.t. PICKL	2			ns
$t_{H_{PIN}}$	PIN [7:0] Hold Time w.r.t. PICKL	1			ns
$t_{D_{SER}}$	Serial Clock (LPDATOP) low to SERDATOP/N Valid Prop Delay	0		500	ps
	Serial Clock (LPDATOP) Duty Cycle	40		60	%
$t_{D_{RP}}$	REFCKINP High to PCLK High Valid Prop Delay	7.0		11.0	ns

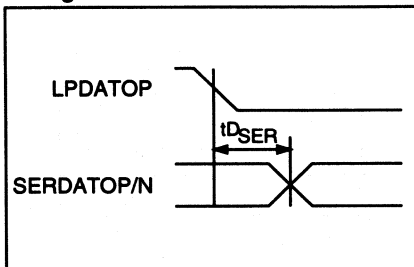
Figure 7. PIN AC Input Timing



Notes on TTL Output Timing:

1. When a set-up time is specified on TTL signals between an input and a clock, the set-up time is the time in nanoseconds from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on TTL signals between an input and a clock, the hold time is the time in nanoseconds from the 50% point of the clock to the 50% point of the input.

Figure 8a. Clock and Data Output Timing with TSCLKSEL Asserted



Notes on PECL Output Timing:

1. Output propagation delay time of high speed PECL outputs is the time in nano seconds from the cross-over point of the reference signal to the cross-over point of the output.

Figure 8b. REFCKIP High to PCLK High Valid Prop Delay

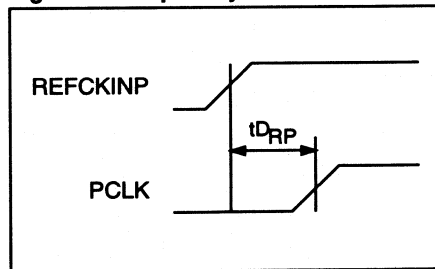


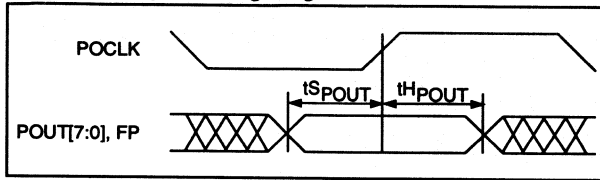
Table 2. S3021 AC Timing Characteristics

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Symbol	Description	Min	Typ	Max	Units
	POCLK Duty Cycle	40		60	%
$t_{S_{POUT}}$	POUT[7:0] and FP Set-up Time w.r.t. POCLK	3			ns
$t_{H_{POUT}}$	POUT[7:0] and FP Hold Time w.r.t. POCLK	2			ns
	SERDATIP/N Minimum Pulse Width	400			ps

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Figure 9. Output Timing Diagram



Notes on TTL Output Timing:

1. Output propagation delay time of TTL outputs is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays and duty cycles of TTL outputs are measured with a 15 pF load and 500 ohms to ground on the outputs.

RECEIVER FRAMING

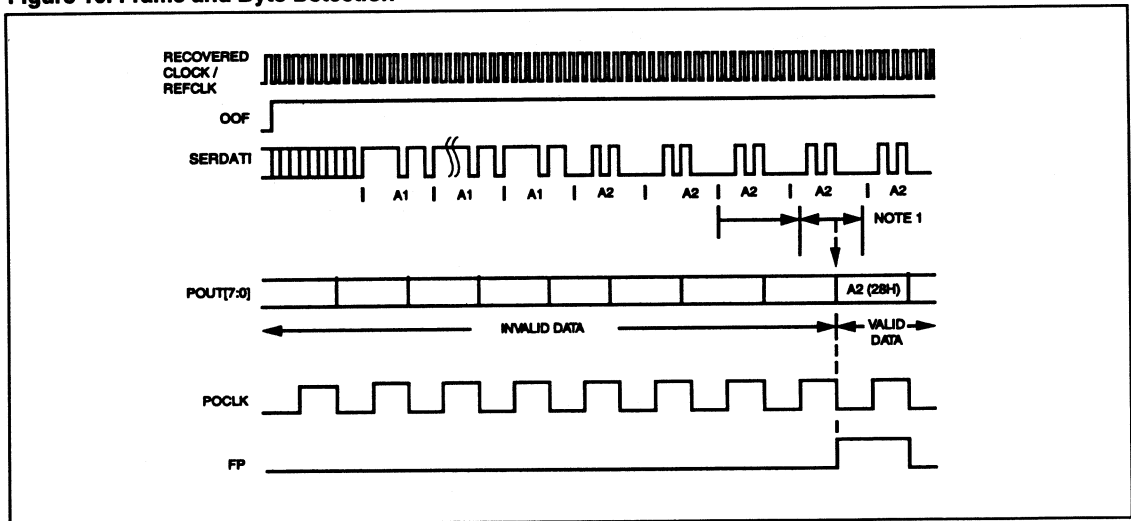
Figure 10 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is high. Re-alignment occurs upon receipt of the first A1 byte. The frame boundary is recognized upon receipt of the third A2 byte, which is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUT[7:0]). Concurrently, the frame pulse is set high for one POCLK cycle.

When interfacing with a section terminating device, the OOF input remains high for one full frame after the first frame pulse while the section terminating device verifies internally that the frame and byte alignment are correct, as shown in Figure 11. Since at least one framing pattern has been detected since the rising edge of OOF, boundary detection is disabled when OOF is set low.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse or until OOF goes low, whichever occurs last. Figure 11 shows a typical OOF timing pattern which occurs when the S3021 is connected to a down stream section terminating device. OOF remains high for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes low.

Figure 12 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 10. Frame and Byte Detection



NOTE 1: Range of input to output delay can be 1.5 to 2.5 POCLK cycles

Figure 11. OOF Operation Timing with PM5312 STTX or PM5355 SUNI-622

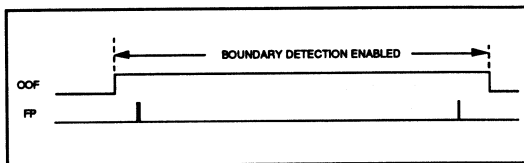
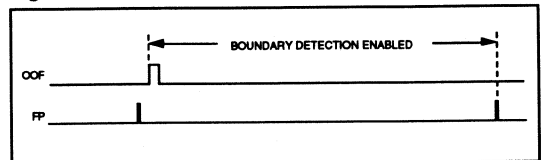


Figure 12. Alternate OOF Timing



S3020 WITH DATA CLOCK SYNCHRONOUS TO REFERENCE CLOCK

INTRODUCTION

In some applications it is necessary to “forward clock” the data in an ATM system. In this application the reference clock from which the high speed serial clock is synthesized and the parallel data clock both originate from the same (usually TTL/CMOS) clock source. This application note explains how the AMCC S3020 can be configured to operate in this mode.

The connections required to implement the design are shown in Figure 13, and the timing specifications are shown in Figure 14. The setup and hold times for the PICKL to the data must be met by the controller ASIC. We recommend latching the data on the falling edge of the output reference clock in order to meet the required specifications.

Clock Control Logic Description

The timing control logic in the S3020 automatically generates an internal load signal which has a fixed relationship to the reference clock. The logic takes into account the variation of the reference clock to the internal load signal over temperature and voltage.

Figure 13. S3020 with Data Clocked by Reference Clock

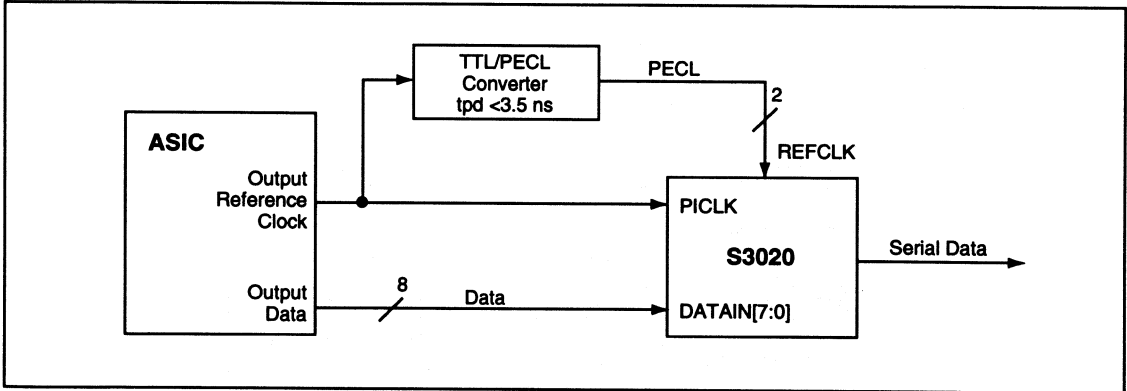


Figure 14. Data Timing with Respect to PICKL

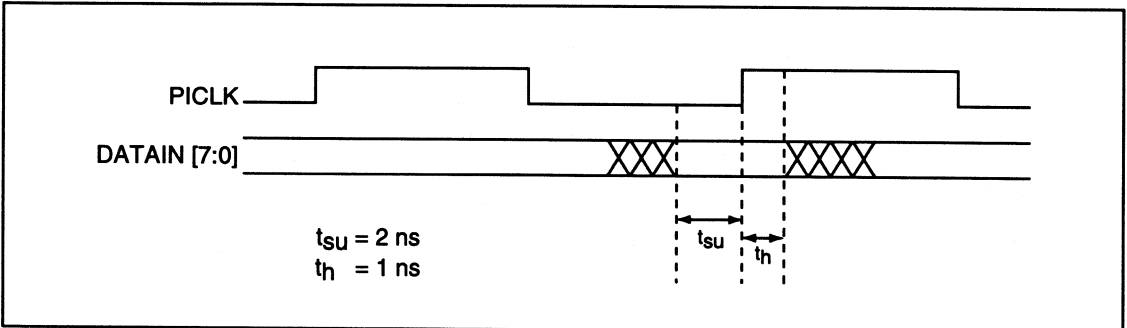
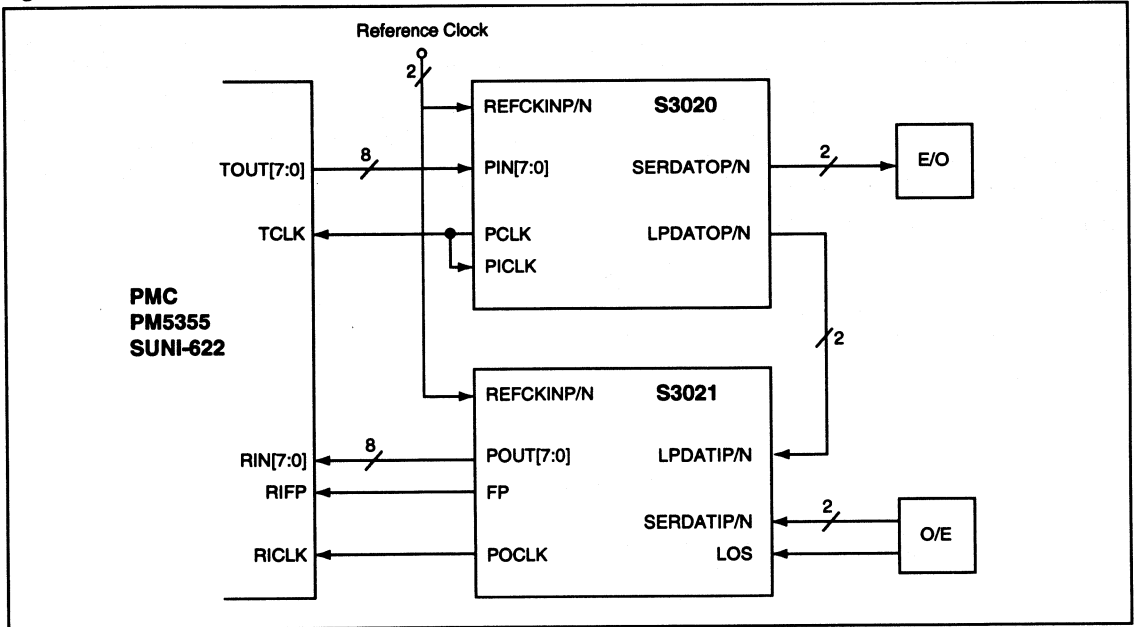


Figure 15. System Block Diagram



Ordering Information

GRADE	TRANSMITTER	PACKAGE
S - commercial	3020	A - 52 PQFP TEP B - Bare Die

GRADE	RECEIVER	PACKAGE
S - commercial	3021	A - 52 PQFP TEP B - Bare Die

X **XXXX** **X**
 Grade Part number Package

OVERVIEW

The S6008 Evaluation Manual describes two evaluation boards that allow demonstration of AMCC's S3020 and S3021 STM-4/OC-12 SONET/SDH/ATM interface circuits. This document provides information on board contents and layout. It should be used in conjunction with the S3020/S3021 data sheet, which contains full technical details on chip operation.

Figure 1 depicts a block diagram of board connectivity for parallel input to parallel output evaluation, while Figure 2 illustrates the connectivity required for serial input to serial output evaluation. Power is supplied to the boards from external supplies connected through the on-board power connectors. Connectors and dip switches allow easy access to all of the interface signals on the S3020/S3021 chips. All required external circuitry, including translation buffers and all passive components, are included on the boards.

Separate boards are provided for the S3020 and the S3021 chips. Layouts for both boards are depicted in Figures 3 and 4, showing the location of connectors, dip switches and components.

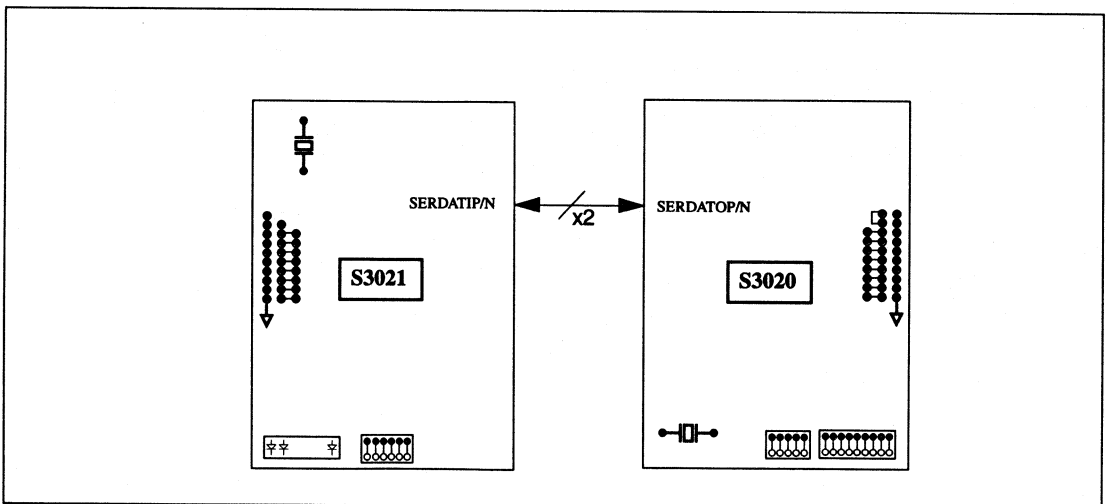
Power Connections

Connections are provided on the board for VCC, ground (GND) and output buffer supplies VCC016 and VEE016. VCC016 and VEE016 are used for level translation between the S3020 device and external test equipment or other standard ECL or +5V Referenced ECL interface circuitry. The buffers that interface to the S3020 and S3021 inputs AC couple and translate between standard ECL and/or +5V referenced ECL to supply the correct +5v referenced ECL levels to the devices. Table 1 illustrates the nominal input voltages for VCC and GND, and gives three possible configurations (vertically aligned) for powering up VCC016 and VEE 016.

Table 1. Power Connections for Test Equipment Interface

Power Supply	Nominal Input Voltage
VCC	5.0V
GND	0.0V
VCC016	2.0V 5.0V 0.0V
VEE016	-3.0V 0.0V -5.0V

Figure 1. S3020 In/S3021 Out Parallel Interface Setup Block Diagram



S3020 Signals

A top level view of the S3020 board is illustrated in Figure 3. The dip switch labeled S1 provides access to all of the S3020 control signals, while Header H1 and dip switch S2 provide access to the TTL input signals PIN[7:0], the parallel input clock PCLK and the output clock PCLK. The OFF position on the dip switches corresponds to a logic 0, while the ON position corresponds to a logic 1.

When it is desired to evaluate the S3020 in a stand-alone mode, jumper H1-A to H1-B for signals PIN[7:0] and jumper PCLK (H1-B) to PCLK (H1-B). In this configuration, the PIN[7:0] inputs can be controlled using the dip switch S2.

When it is desired to interface the S3020 to the S3021 for testing parameters such as jitter tolerance (serial into the S3021, parallel out fed back to the parallel inputs of the S3020 and then monitoring the serial output of the S3020), connect the QC-1 jumper block that is included with the board, as shown in Figure 2.

When the RSTB push button switch is depressed, the S3020 goes into RESET mode and the part will remain in this mode until the button is released.

S3021 Signals

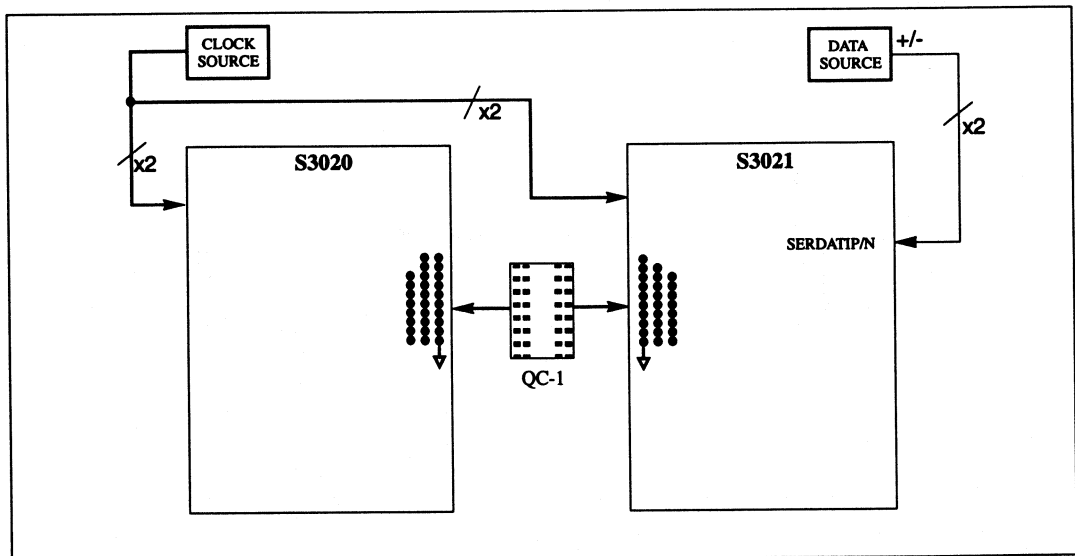
A top level view of the S3021 board is illustrated in Figure 4. The dip switch labeled S3 provides access to all of the S3021 control signals, while Header H2 and LED bank U1 provide access to the TTL output signals POUT[7:0], the output clock POCLK and the LOCKDET output.

When it is desired to evaluate the S3021 in a stand-alone mode, jumper header pins H2-B to H2-C for all of the POUT pins and the LEDs will turn on for each occurrence of a 1 and off for each occurrence of a 0. Another option is to create a ribbon cable or to use single discrete cables attached to the header H2-B pins and then connect the TTL outputs to a SONET analyzer or a standard logic analyzer.

When it is desired to interface the S3021 to the S3020 for testing parameters such as jitter tolerance (serial into the S3021, parallel out fed back to the parallel inputs of the S3020 and then monitoring the serial outputs of the S3020), connect the QC-1 jumper block that is included with the board, as shown in Figure 2.

When the RSTB push button switch is depressed, the S3020 goes into RESET mode and the part will remain in this mode until the button is released.

Figure 2. S3021 In - S3020 Out Serial Interface Setup - Block Diagram

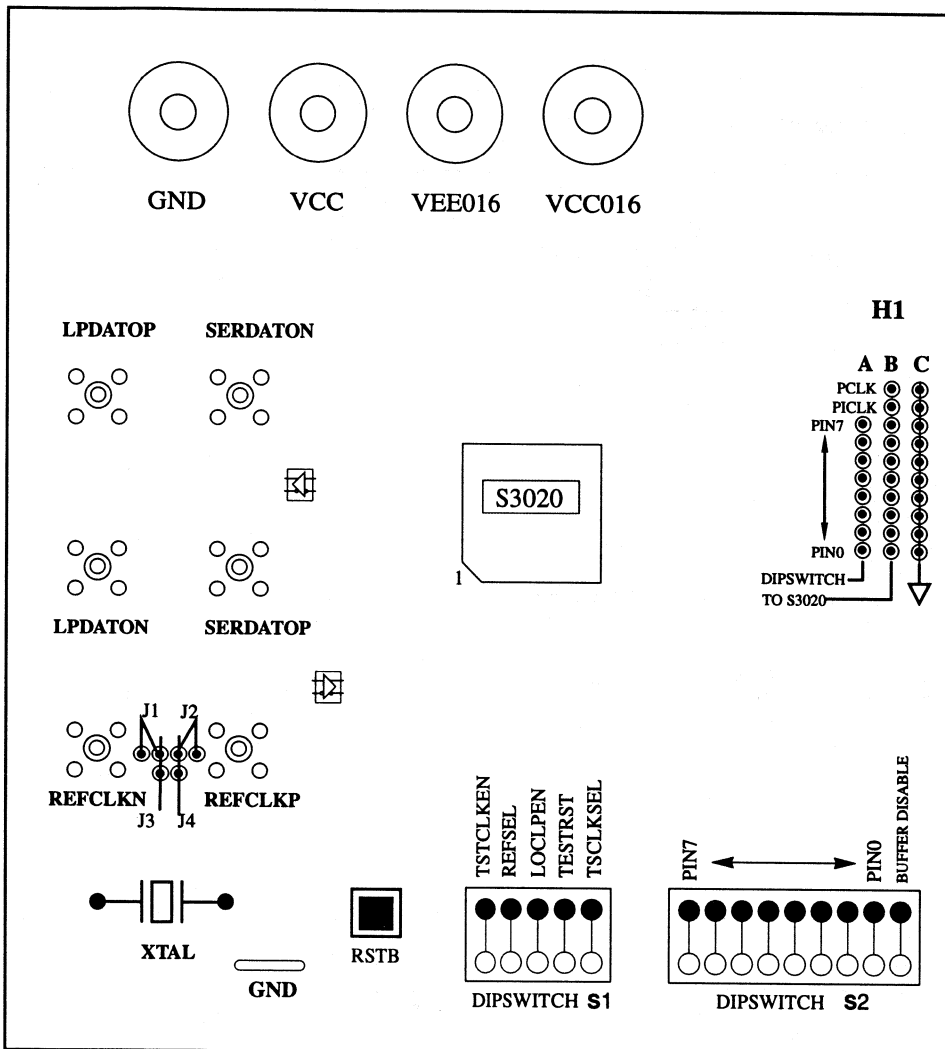


CRYSTAL REFERENCES AND CLOCK GENERATION

19.44 MHz or 77.76 MHz differential ECL crystal oscillators with 100-ppm stability should be used for the reference clocks.

One 77.76 MHz crystal is provided for each board. If 19.44 MHz crystals are needed, AMCC can recommend crystal vendors.

Figure 3. S3020 Board Layout



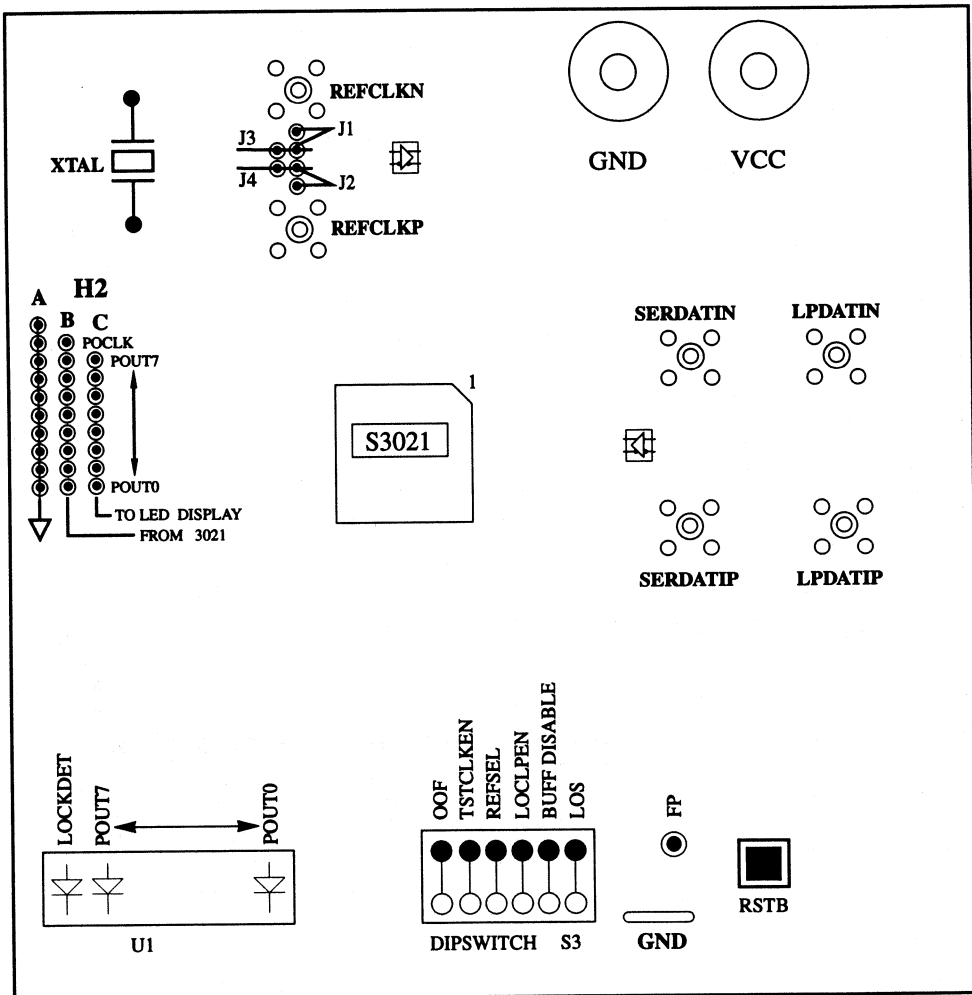
JUMPER CONFIGURATION

The jumpers labeled J1 - J4 on both boards allow the user to control whether an on-board crystal reference or external clock reference is used. Jumpers J1 and J2 must be installed when an external reference is used (input into the REFCLKP/N SMAs), while jumpers J3 and J4 must be installed to use the on-board crystal reference.

SMA CONNECTIONS

SMA connections provide input/output capability for a number of signals, including all serial data I/O and the reference clocks. All of these connectors are labeled on the boards and are also shown in Figures 3 and 4.

Figure 4. S3021 Board Layout



FEATURES

- IEEE 802.12 compliant
- Full Duplex Capability
- Single +5 V supply
- STP or Fiber support
- Fixed receiver based equalization
- Transmit clock generation
- Receive data/clock recovery
- Transmit Control State generation
- Receive Control State detection
- Standard 52 PQFP package

APPLICATIONS

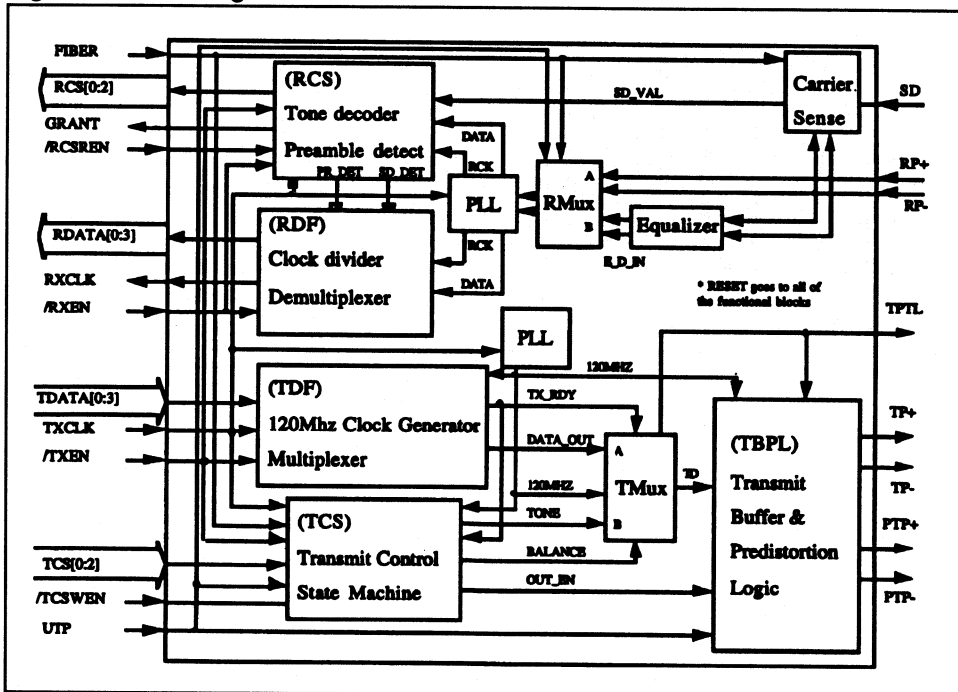
- High-speed Local Area Networks
- The S2100 can be used in all 100VG-AnyLAN network applications that require Fiber or STP cabling in either the HUB or END-NODE end.

DESCRIPTION

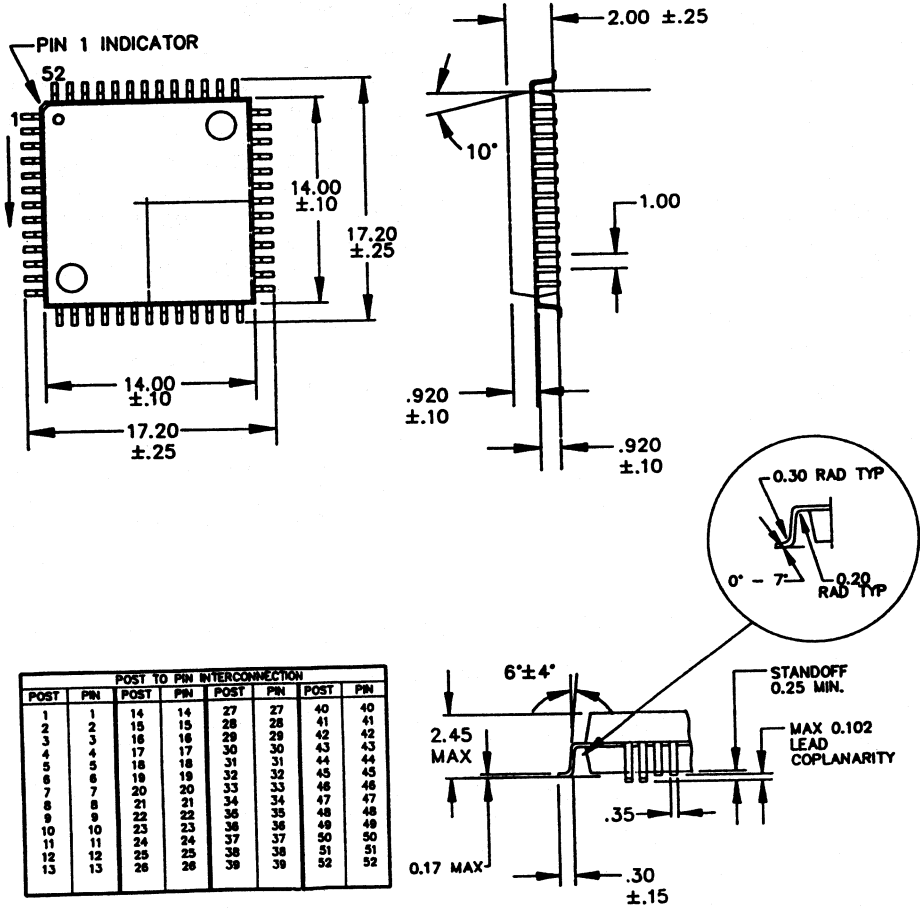
The S2100 100VG-AnyLAN STP/Fiber-optic Transceiver chip contains all of the functionality required to implement the IEEE 802.12 PMD specifications for transmission onto (or reception from) 150 ohm STP cable. The differential transmit and receive circuits are PECL compatible which makes them suitable for direct connection to a filter module, or to a Fiber-optic transceiver like the HFBR-5103. The transmit pre-distortion function will provide an optional 2 pair CAT-V functionality when used with the receive equalizer.

The TCS machine indicates a node's status to the network and the RCS machine decodes the network status. The TDF circuit formats and multiplexes the nibble wide data into a single 120Mbit/s data stream, and the RDF de-multiplexes then re-formats the data into a 30M nibble/s bus. For STP applications, carrier detect and equalization are also performed.

Figure 1. Block Diagram



52-Pin PQFP (14mm x 14mm)



All dimensions are in mm.

CONTENTS

FIBRE CHANNEL PRODUCTS

S2036—Open Fiber Control	4-3
S2042/S2043—High Performance Serial Interface Circuits	4-17
S2044/S2045—GLM Compliant Serial Interface Circuits	4-37
S2052—High Performance Serial Interface Circuit	4-55
S2060—Fibre Channel 8B/10B ENDEC	4-57

FEATURES

- Implements redundant safety interlock for laser-based fiber optic systems
- Functionally compliant with ANSI XT311 Fibre Channel physical standard
- Enables Class 1 safety compliance for FDA, ANSI, and IEC guidelines
- Operates with the AMCC S2042/S2043, and S2044/S2045 Fibre Channel Chipsets at 265.625, 531.25, and 1062.5 Mbit/s
- On-chip ring oscillator
- Ultra low power operation
- 28-pin SOIC package
- PECL Interface

APPLICATIONS

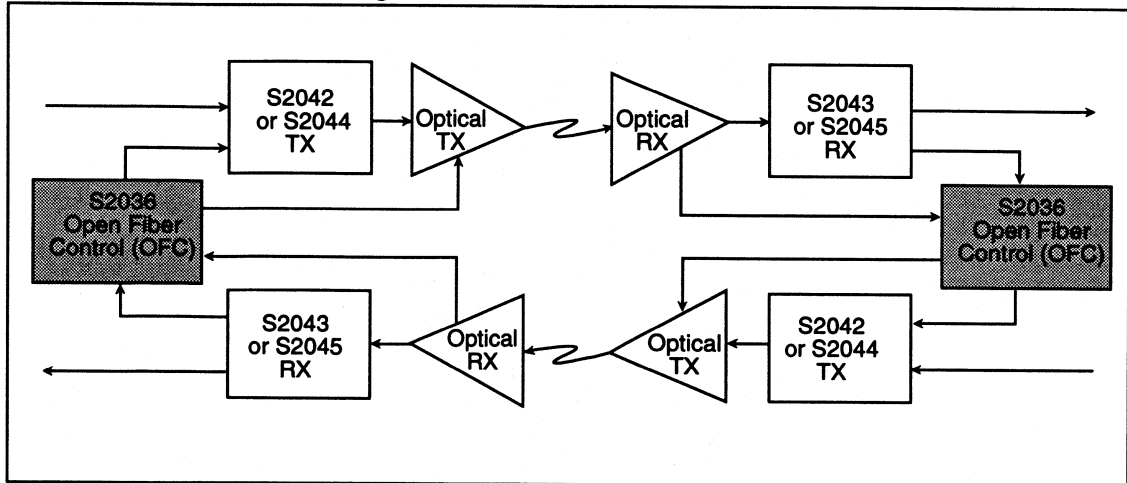
- Laser-based fiber optic systems
- Medical and laboratory instrumentation
- High-speed data and telecommunications
 - Supercomputer
 - Mainframe
 - Broadcast Environments
 - Frame buffer
 - Switched networks
 - Mass storage/RAID
 - Workstation

GENERAL DESCRIPTION

The S2036 is designed specifically to implement the Fibre Channel Open Fiber Control (OFC) system, a redundant safety interlock feature for laser-based fiber optic systems. It is functionally compliant with the ANSI XT311 Fibre Channel physical standard and implements the OFC system defined by that standard, to detect when the optical link has been disrupted and shut down the laser or reduce the optical power level. The S2036 employs effectively redundant paths, each of which can independently turn off the laser.

The chip meets the requirements of Class 1 safety limits defined by FDA, ANSI, and IEC. It is fully compatible with AMCC's S2042/S2043 and S2044/S2045 Fibre Channel chipsets at 265.625, 531.25, and 1062.5 Mbit/s operation. It features low-power operation and a 28-pin SOIC package. Figure 1 shows the S2036 used in a typical network configuration.

Figure 1. Typical Network Configuration



OPEN FIBER CONTROL OVERVIEW

The OFC system is an open fiber link detection and laser control system specified in ANSI XT311 Fibre Channel physical standard. It is used as a safety interlock for point-to-point optical fiber links that use semiconductor laser diodes as the optical source. The major reason for implementing OFC is that the optical power levels required to obtain the desired level of system performance in Fibre Channel exceeds the Class 1 limits defined by national and international laser safety standards, if the optical fiber link between two optical ports is disconnected, such as would occur with an opened connector or a cut fiber. It is extremely important that requirements for Class 1 classification are met, due to the potential for customer exposure to laser radiation.

Since it is only when an optical link is opened that a user can be exposed to laser radiation, implementing OFC allows Class 1 classification requirements to be met, since it can detect when the link has been disrupted and can shut down the laser or reduce the optical power level. The S2036 complies fully with the OFC specifications and Class 1 requirements.

Refer to the ANSI Fibre Channel standard document for details of OFC operation.

CIRCUIT OPERATION

Whenever the fiber data link is disrupted (by a cut fiber or a disconnected connector), the S2036 detects the disruption and forces the transceiver into a repetitive pulsing mode of operation with a very low

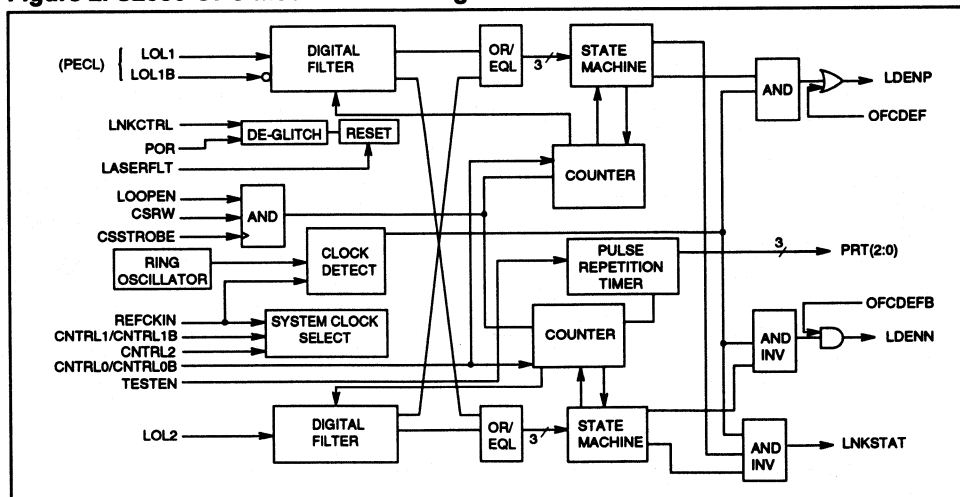
duty cycle. The link returns to normal operation only when the device detects that the disruption has been repaired and the proper reconnection handshake has taken place between the two transceivers in the link.

As seen in the module block diagram in Figure 2, two loss-of-light control paths are provided and both must be satisfied before the laser can be activated. Each path has a separate digital filter, state machine, and a counter. Two loss-of-light detectors each feed a digital filter. The output of each filter is "OR/EQUALed" to produce an interval Loss-of-Light (LOL) signal. If the REFCKIN is too fast or too slow, the clock detector causes the laser to be deactivated. Two laser driver control outputs are independently capable of disabling the laser drive circuitry. They are of opposite polarity to prevent voltage control problems from accidentally activating the laser. The link status output signals the user system when the link is inactive.

A power-on-reset signal is used to synchronize the counters and state machines. Three user system control lines, Laser Fault, Link Control and Loopback Enable, force the S2036 to disable the laser drive circuitry and turn off the laser.

The two state machines are independent and identical, and contain the logic to detect when the optical link becomes open due to a disconnection or break. They also preside over the link reconnection handshake when it detects that the link is reconnected.

Figure 2. S2036 OFC Module Block Diagram



OFC Time Periods

The OFC system uses a repetitive pulsing technique (i.e., laser activated for t microseconds every T seconds) during the time that a link is open in order to reduce the maximum possible exposure to a value which allows for classification as a Class 1 laser product. The maximum average power level per pulse is a function of the wavelength, pulse duration (t), and pulse repetition frequency ($PRF = 1/T$).

To function correctly, each short-wavelength optical link port must contain a transmitter/receiver unit that has implemented the OFC system with compatible OFC interface timings. The timing values that are consistent with the stated maximum transmitter receptacle power and current (1990) IEC laser safety restrictions for a Class 1 system are shown in Table 1.

These time periods, when used according to the OFC interface specification described in this section, should result in a laser product which conforms to current (1990) emission requirements for Class 1 classification worldwide. Note, however, that classification of a laser product must always be verified with measurements and calculations and not assumed.

The connection and disconnection handshake timing is shown in Figures 5 and 6. The connection handshake is performed at link initialization or at the automatic recovery from intentional or accidental interruption of the optical path. The Pulse duration, t , is chosen to meet the maximum average power level

while allowing for the propagation delay through both fibers and the light detection and laser turn-on delay of the complete transceiver system. This margin is shown as t_{setH} . Similarly, the Stop time t_s is set at either $2t$ or $4t$ to assure that the detected pulse originates from a properly functioning OFC node. This is accomplished by the detection of loss of light for a time t_{setL} prior to the end of the Stop time. In Figure 5, the Master node is the one whose 10.1 second timer expires first after the reconnection is complete.

Figure 6 illustrates the reaction of the system to the disruption of one fiber (the one between the Master transmitter and the Slave receiver). Since the other fiber is still intact in this example, the Master transmitter is shown as again having its 10.1 second timer expire first, but then resynchronizing to the received pulse from the Slave transmitter.

Safety Documentation/Usage Restrictions

Shortwave laser transceiver products incorporating the OFC system in order to assure Class 1 compliance shall include the following two usage restrictions as part of the product's user, maintenance, and safety documentation:

- a) The laser product shall be used in point-to-point optical links only. The OFC safety system is incompatible with other types of link connections (i.e., multiple input or output links). Failure to

Table 1. Selectable OFC Time Periods

Symbol	Description	25 Mbyte/s	50/100 Mbyte/s	Units
CNTRL0/0B	Counter Control 0	Low	High	—
t	Pulse duration time	617	154	μ sec
T	Pulse repetition time	10.1	10.1	sec
t_s	Stop time	1234	617	μ sec
t_{LDENon}	LOL1 & LOL2 inactive to LDENP/N	2-4	2-4	μ sec
$t_{LDENoff}$	LOL1 or LOL2 active to LDENP/N	20-40	20-40	μ sec
t_{ldon}	Laser turn-on time	LDENon + Laser activation time		—
t_{ldoff}	Laser turn-off time	LDENoff + Laser deactivation time		—
t_{pdf1}	Propagation delay, fiber 1			—
t_{pdf2}	Propagation delay, fiber 2			—

comply with this usage restriction may result in incorrect operation of the link and points of access that may emit laser radiation above the limit for Safety Class 1 systems established by one or more national or international laser safety standards.

- b) Normal operation of the point-to-point optical link requires that the laser product shall be connected only to another Fibre Channel compatible laser product that includes the OFC safety system. In addition, each of these products must be certified as Safety Class 1 laser products according to the laser safety regulations and/or standards in existence at the time of manufacture.

The certification ensures that each of the products will function correctly in the event of a fault in one of the safety control systems.

It is the responsibility of the interface designer to assure that the redundancy and freedom from single point failure sensitivity incorporated in the Fibre Channel standard and the design of the S2036 are fully implemented in the final laser product. These implementation criteria shall include but are not limited to:

- a) Biasing of the LDENP/N signal lines with 10KΩ resistors external to the S2036 assures that the non-operating state of the laser is forced if the S2036 is removed or destroyed while the system is operating.

- b) Use of the redundant control signals (CNTRL0B and CNTRL1B) to assure safe operation or no operation in the event of a single point failure of any control signal.

WARNING! IMPORTANT!

The S2036 is equipped with an override function to permit activation of the attached laser during module level testing. This function is operable with the TESTEN held in the active high state and OFCDEF held High and OFCDEFB held Low only. It is the responsibility of the manufacturer to isolate these inputs from accidental activation by the end user. Failure to do so may void the certification of the module or the OEM system for Laser Safety Class 1 operation.

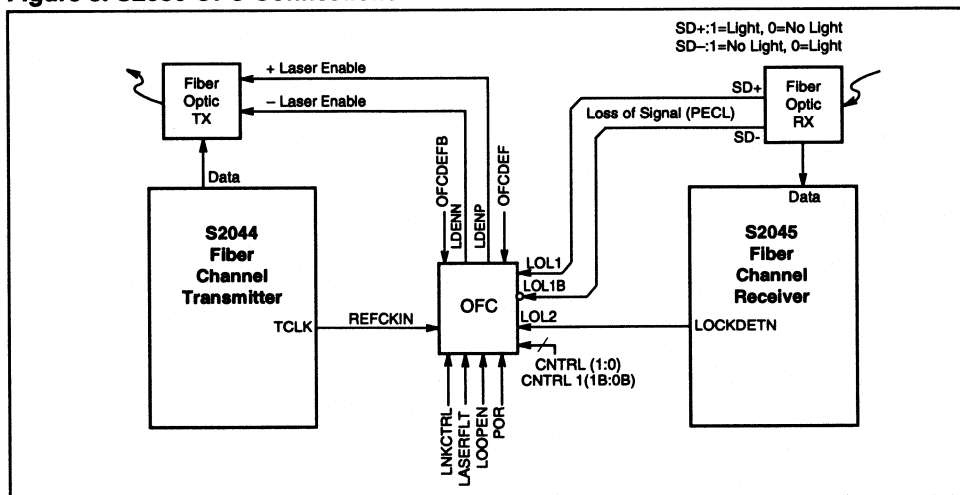
Digital Filter

The digital filters integrate the incoming signals to improve their reliability. The filters sample at a faster rate when acquiring a light-present signal and at a slower rate when dropping a light-present signal, while maintaining the correct handshake timing.

State Machine

The state machine is implemented per the Fibre Channel FC-PH document, Paragraph 6.2.3 and annex I. The OFC time periods are user-selectable to comply with the operating frequency of the serial link. The selectable OFC time periods are seen in Table 1. The pulse repetition time is fixed for both 25, 50, and 100 Mbyte applications to 10.1 seconds.

Figure 3. S2036 OFC Connections



The inputs to the state machine are the loss of light indicators (DC and AC) and the power-on reset. The timing of the state machine transitions is controlled by the decode times. The timing of the laser control signals will not necessarily be synchronous to the system clock because of the long counter times involved.

Link Initialization

Following a power-on-reset cycle, the OFC device will be in the Stop State as defined in the Fibre Channel Standard. The default state for the internal loopback control is loopback active. A Control/Status Write cycle is required together with a logic high on the LOOPEN input in order to place the OFC in the Reconnect State allowing the repetitive pulsed output operation. The required timing for this write cycle is shown in Figure 5.

Reference Clock Select

The reference clock is user-selectable to be 53 MHz or 26 MHz. The reference clock input is divided by four if a 53-MHz clock is used, or by two for a 26-MHz clock so that all state machine and counter clocks operate at 13 MHz. Refer to Figure 3 and Figures 7 through 10 for suggested connections.

Clock Detect

The clock detect circuitry compares the reference clock input and the ring oscillator. If the ring oscillator and the reference clock frequencies do not compare as selected by CTRL2, CTRL1/1B, and CTRL0/0B, the laser is disabled to prevent it from staying on or increasing the laser duty cycle.

De-Glitch Logic

The de-glitch logic debounces the power-on reset and the link control pin to eliminate potential glitching of the laser control lines.

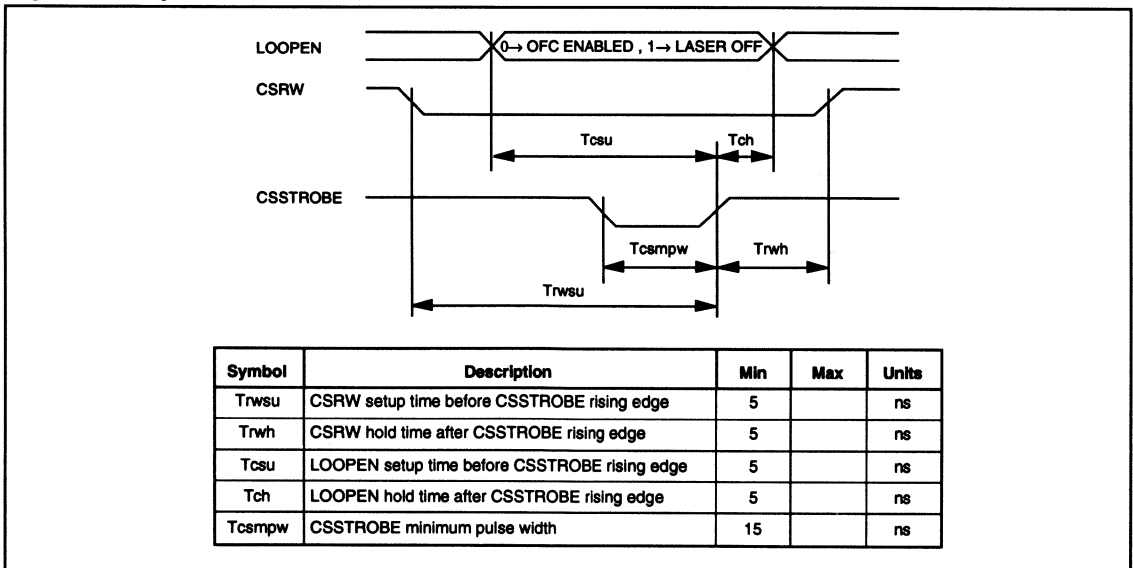
Counter

The two counter blocks are redundant functions which generate the selected decode timing used by the state machines. (See Table 1 for OFC time periods.) One of the counters is used as the lower part of the 10.1 sec pulse repetition timer.

Pulse Repetition Timer

The pulse repetition timer generates the 10.1 sec decode timer used by the state machines. In test mode it is broken up into three counter stages which is output on the PRT<0> pin.

Figure 4. Loopback Enable Write Access



PIN DESCRIPTIONS

INPUT SIGNALS

Power On Reset [POR]. TTL. Active Low. Power-on reset signal which is sampled by the de-glitching circuitry.

Reference Clock [REFCKIN]. TTL. 53 MHz or 26-MHz clock used as the master clock for the state machine and the counters. This clock is monitored by the ring oscillator for correct frequency. This pin should be tied to TCLK of the S2044.

Control/Status Read/Write [CSRW]. TTL. This input must be low to enable the clocking of the Loopback Enable signal.

Counter Control 0 [CNTRL0]. TTL. This pin controls the counter values which determine the decode time periods. It should be set to low for 617 μ s laser pulses and high for 154 μ s laser pulses. (See Table 1). It is also used during device testing to verify the ring oscillator circuitry.

Counter Control 0B [CNTRL0B]. TTL. This pin is a backup for CNTRL0 and should be independently driven to the same logic state. The full use of this pin prevents the unwanted generation of a 617 μ sec pulse due to a single point failure of CNTRL0 to logic low.

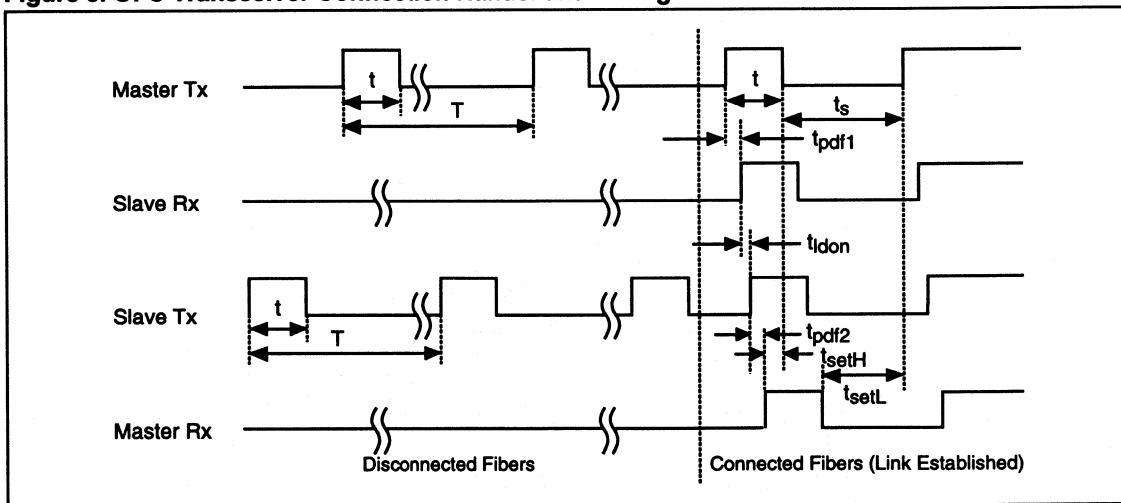
A false low on CNTRL0 or a false high on CNTRL0B will result in a reset of the S2036 and selects the ring oscillator to TESTOUT when TESTEN is low. A false high on CNTRL0 will result in 154 μ sec pulses.

Counter Control 1 [CNTRL1]. TTL. This pin, together with the CNTRL2 pin, selects the reference clock frequency. If the reference clock is 53 MHz, this pin must be high, and CNTRL2 must be low. If the reference clock is 26 MHz, this pin and CNTRL2 must both be low.

Counter Control 1B [CNTRL1B]. TTL. This pin is a backup for CNTRL1 and should be independently driven to the same logic state.

Test Clock [TESTCK]. TTL. This clock input is used in test to replace the ring oscillator when OFCDEF and OFCDEFB are both High or Low.

Figure 5. OFC Transceiver Connection Handshake Timing



Counter Control 2 [CNTRL2]. TTL. This pin is used with CNTRL1 to select the reference clock frequency and should be set to Low.

Loss of Light 1 [LOL1/1B]. PECL. Active Low. When low, indicates that an optical signal is *not* present at the input to the fiber optic receiver. These pins must be tied to the Loss of Signal pin of the fiber optic receiver for a DC loss of signal function. (See Figure 3.)

Loss of Light 2 [LOL2]. TTL. Active High. When high, indicates that an optical signal is *not* present at the input to the fiber optic receiver. This pin must be tied to the S2044 LOCKDETN signal for an AC loss of signal function. (See Figure 3.)

Loopback Enable [LOOPEN]. TTL. Active High. This pin, when high, deactivates the laser diode enable pins (both LDENP and LDENN) regardless of the state of the state machine. It is enabled by the CSRW and clocked by the TCLK of the S2044/45 devices. Once the laser is turned off, only the OFC system can turn it back on by performing a link reconnection handshake.

Laser Fault [LASERFLT]. TTL. Active High. This pin, when high, will deactivate the laser diode enable pins (both LDENP and LDENN) regardless of the state of the state machine. Asserts LNKSTAT. Once the laser is turned off, only the OFC system can turn it back on by performing a link reconnection handshake.

Link Control [LNKCTRL]. TTL. Active High. This pin, when high, will deactivate the laser diode enable pins (both LDENP and LDENN) regardless of the state of the state machine. It is de-glitched to filter spurious transitions of the laser diode enabled signals. Once the laser is turned off, only the OFC system can turn it back on by performing a link reconnection handshake.

Control/Status Strobe [CSSTROBE]. TTL. This pin is used to clock the Loopback Enable signal. It is intended to be tied to the TCLK pin of the S2044. The Loopback Enable signal is clocked on the rising edge of CSSTROBE.

Test Mode Enable [TESTEN]. TTL. Active High. Internal pull-down resistor attached. This pin forces the pulse repetition counter to be broken up into five individual counters for test purposes and disables the LDENN output and selects TESTCK to TESTOUT when OFCDEF and OFCDEFB are both High or Low.

Positive Laser Diode Enable Forced [OFCDEF]. TTL. Active High. Internal pull-down resistor attached. This pin will override the OFC control of the positive laser diode enable and force the laser to be enabled for test, when TESTEN is High.

Negative Laser Diode Enable Forced [OFCDEFB]. TTL. Active Low. Internal pull-up resistor attached. This pin will override the OFC control of the negative laser diode enable and force the laser to be enabled for test, when TESTEN is High.

OUTPUT SIGNALS

Link Status [LNKSTAT]. TTL. High = Link inactive. This pin indicates to the system when the link is inactive due to a loss of signal condition detected by the OFC system. This signal is active during LOOPBACK mode. Asserted when LASERFLT signal is asserted.

Test Output [TESTOUT]. TTL. Outputs TESTCK input when TESTEN is High and OFCDEF and OFCDEFB are both High or Low, or outputs ring oscillator divided by 4 when TESTEN is Low and CNTRL0 is Low and CNTRL0B is High. Otherwise, outputs high impedance.

Positive Laser Diode Enable [LDENP]. TTL. Active High. This pin is an output of the state machine and should be tied to the positive enable pin of the laser diode transmitter. Each of the laser diode enable pins are independently capable of disabling the laser drive circuitry (via separate control paths). The enable pins are of opposite polarity to prevent voltage control problems from accidentally activating the laser.

Negative Laser Diode Enable [LDENN]. TTL. Active Low. This pin is an output of the state machine and should be tied to the negative enable pin of the laser diode transmitter. Each of the laser diode enable pins are independently capable of disabling the laser drive circuitry (via separate control paths). The enable pins are of opposite polarity to prevent voltage control problems from accidentally activating the laser.

Pulse Repetition Time [PRT] <2:0>. TTL. In normal operating mode this bus monitors the output of the LOL2 and LOL1 digital filters (on PRT2 and PRT1 respectively). Logic high represents loss of light. PRT0 monitors the internal reset of the S2036. In TESTEN mode, PRT2 and PRT1 monitor the laser on output of state machines 2 and 1, while PRT 0 monitors the end of the counter chain (REFCLK/4096 or REFCLK/9192).

Figure 6. OFC Transceiver Disconnect Handshake Timing

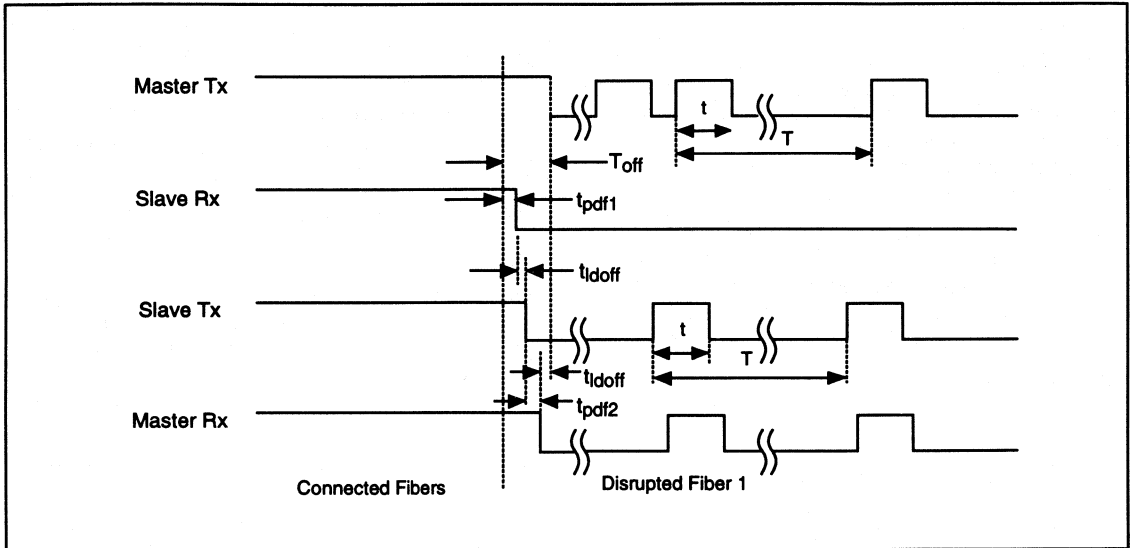
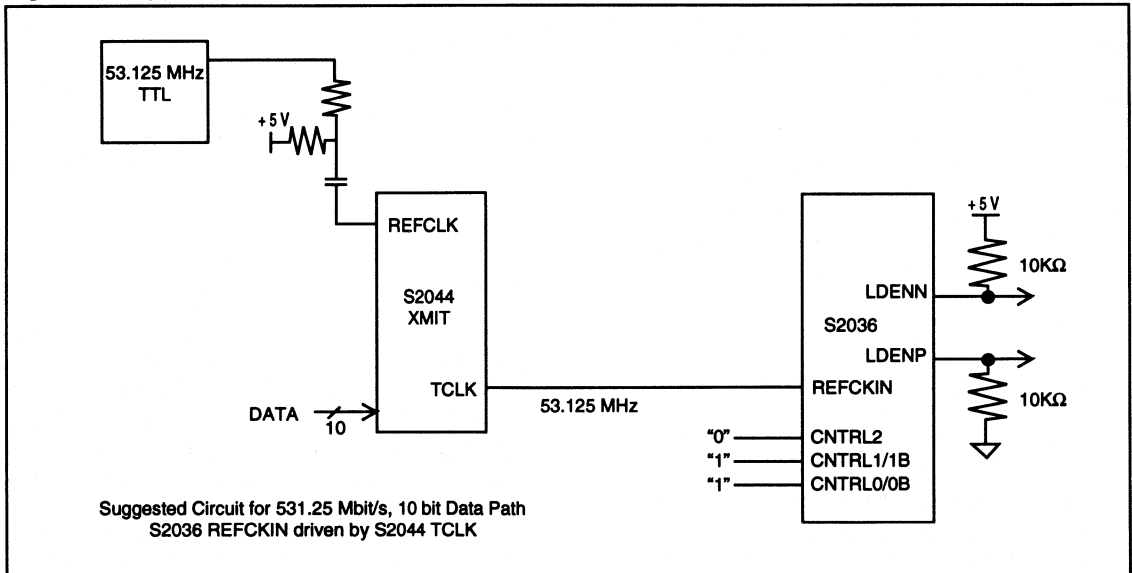


Figure 7. Suggested Circuit for 531.25 Mbit/s Operation with S2044 in 10-Bit Mode



APPLICATIONS SUGGESTIONS

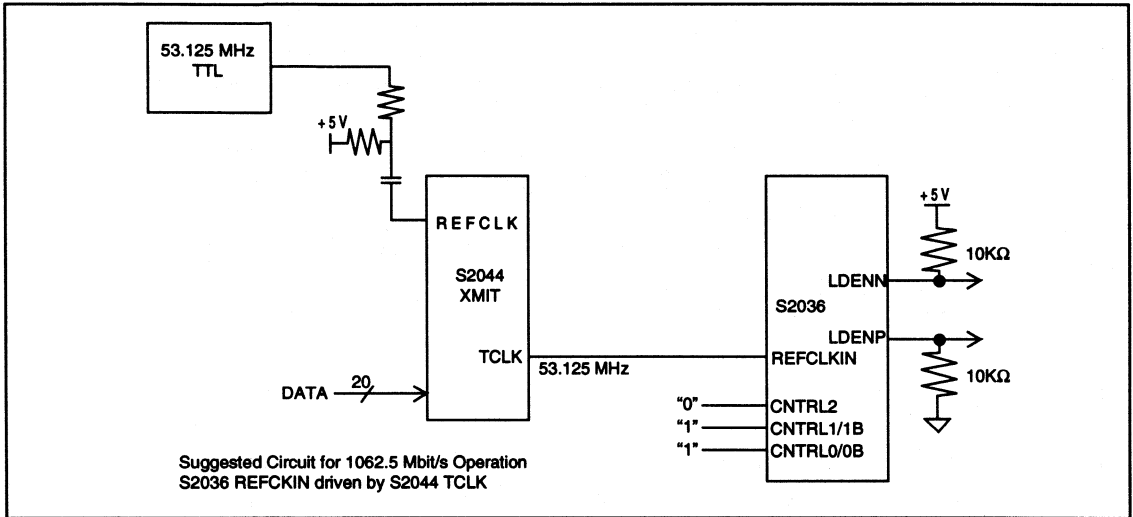
REFCKIN Connection Options

The S2036 can be used with the S2044 or S2045 with only the addition of attenuating resistors for the reference clock source. Figure 7 shows the connec-

tion of the reference clock with the S2044 operating in the 10 bit mode at 531 Mbit/s data rate. The clock trace lengths should be minimized.

Figures 8–10 illustrate representative (but not exhaustive) combinations of CNTRL inputs and REFCKIN drive sources.

Figure 8. Suggested Circuit for 1062.5 Mbit/s Operation with S2044 in 20-Bit Mode



4

Figure 9. Suggested Circuit for 531.25 Mbit/s Operation with S2044 in 20-Bit Mode

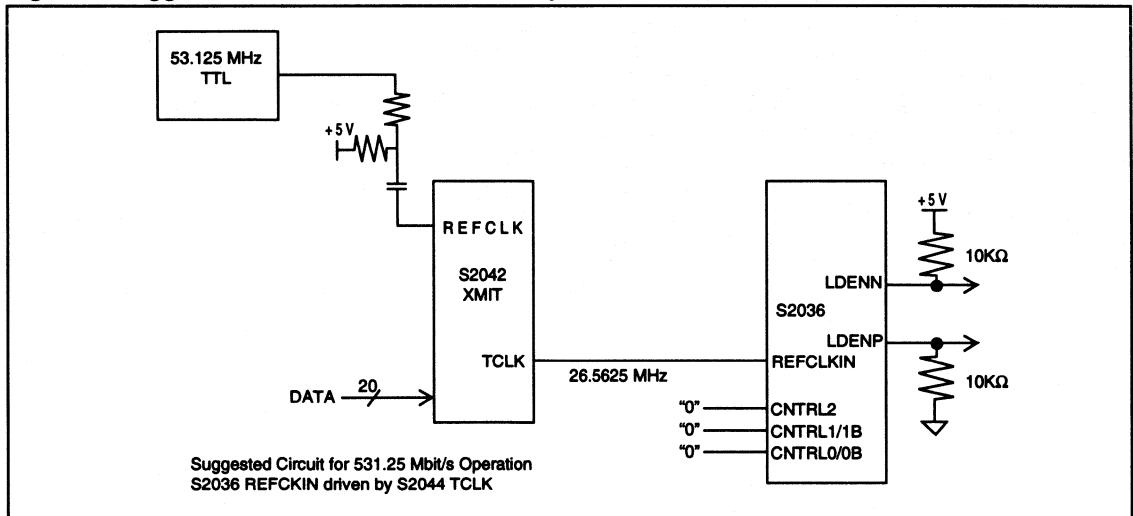
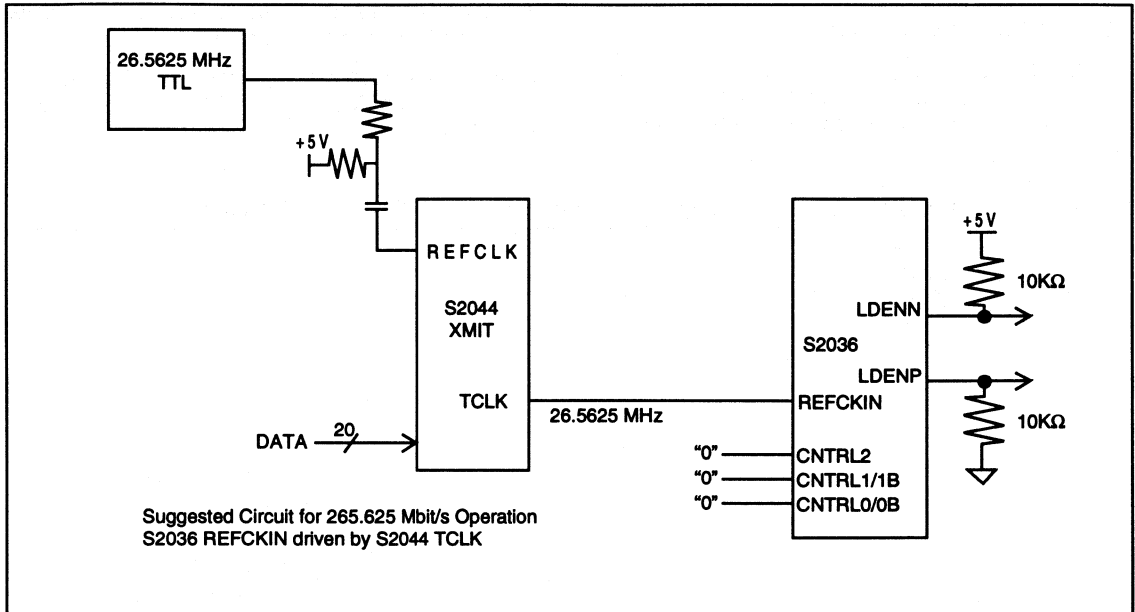


Figure 10. Suggested Circuit for 265.625 Mbit/s Operation with S2044 in 10-Bit Mode



LOL1/1B Single-Ended Application

The LOL1/LOL1B inputs are defined as PECL differential inputs. The macro design allows either input to be set to a fixed voltage in a range from 1.25V to 3.75V, and thus used as a threshold voltage for the other input. If the LOL1B input were connected to a resistor voltage divider providing ~1.5V, the LOL1 input can then be considered a single-ended TTL input. A suitable divider can be formed with a 33KΩ resistor and a 13KΩ resistor. For a Vcc of 5.0V, this would provide a threshold of 1.4V. If the TTL input levels of $V_{IHmin} = 2.0V$ and $V_{ILmax} = 0.8V$ are assumed, the 1.4V threshold gives a minimum of 600mV of margin. The macro requires 300mV for reliable switching, so this threshold gives a 2x margin at worst case TTL input levels.

Figure 11. LOL1/1B Single-Ended TTL Input

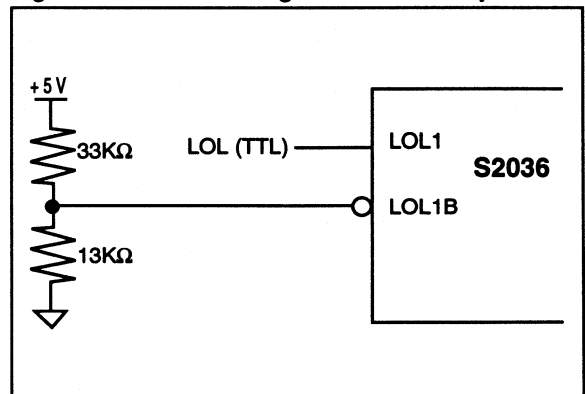
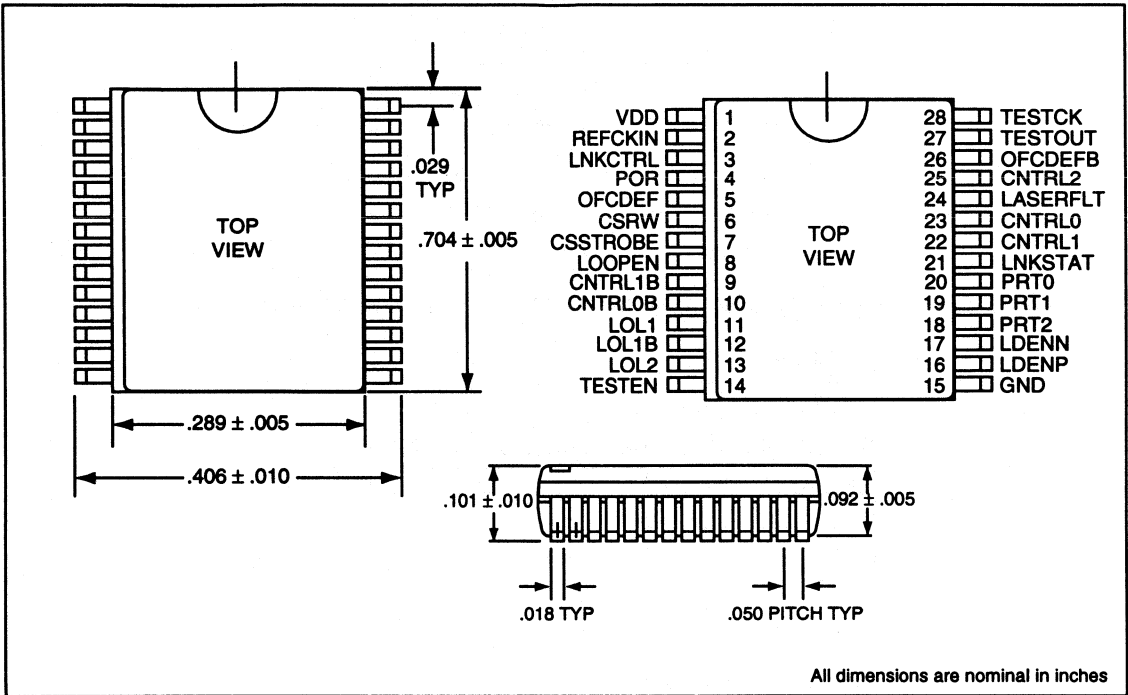


Figure 12. 28 SOIC Package and Pinout



Absolute Maximum Ratings

Supply Voltage V_{DD}	7.0V	
TTL Input Voltage	$V_{DD} + 0.3V$	
Operating Junction Temperature T_J	+150°C	
Storage Temperature	-55° to +150°C	
Input Pin Current	-10mA to 10mA	25°C
Lead Temperature	300°C	10 sec.

Recommended Operating Conditions

Parameter	MIN	NOM	MAX	Unit
Supply Voltage (V_{DD})	4.75	5.0	5.25	V
Operating Temperature	0 ambient		70 ambient	°C
Junction Temperature			130	°C
Supply Current (I_{DD})		14	19	mA

PECL Input DC Characteristics $V_{DD} = 4.75V$ to $5.25V$

Symbol	Conditions	MIN	TYP	MAX	Unit
V_{IH}				$V_{DD} - 600$	mV
V_{IL}		$V_{DD} - 2000$			mV
V_{ID}		250 ⁵	500	1400	mV
I_{IH}				20	μA
I_{IL}		-1			μA

TTL Input/Output DC Characteristics

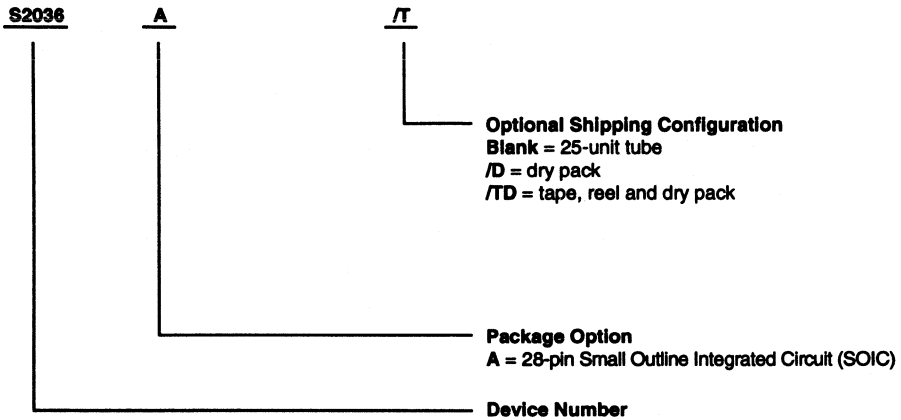
Symbol	Parameter	Test Conditions	COMM. 0° TO 70°C			Unit
			MIN	TYP ¹	MAX	
V_{IH}^2	Input voltage HIGH	Guaranteed input HIGH voltage for all inputs	2.0			V
V_{IL}^2	Input voltage LOW	Guaranteed input LOW voltage for all inputs			0.8	V
V_{OH}	Output voltage HIGH	$V_{DD} = \text{Min}$, $I_{OH} = -4\text{mA}$ for TESTOUT -8mA for all other outputs	2.4			V
V_{OL}	Output voltage LOW	$V_{DD} = \text{Min}$, $I_{OL} = 4\text{mA}$ for TESTOUT 8 mA for all other outputs			0.4	V
I_{OZH}	Output "off" current HIGH	$V_{DD} = \text{Max}$, $V_{OUT} = 2.4V$	-10		10	μA
I_{OZL}	Output "off" current LOW	$V_{DD} = \text{Max}$, $V_{OUT} = 0.4V$	-10		10	μA
I_{IH}	Input current HIGH	$V_{DD} = \text{Max}$, $V_{IN} = V_{DD} \text{ MAX}$			see note 3	μA
I_{IL}	Input current LOW	$V_{DD} = \text{Max}$, $V_{IN} = 0V$	see note 4			μA

- Typical limits are at 25°C, $V_{DD} = 5.0V$.
- These input levels provide a zero noise immunity and should only be tested in a static, noise-free environment.
- Use extreme care in defining input levels for dynamic testing. Many outputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for dynamic TTL testing and V_{ILMIN} and V_{IHMAX} for PECL testing.
- I_{IH} (min) = 36μA; I_{IH} (max) = 142μA for OFCDEF, TESTEN.
- I_{IH} (max) = 1μA for all other inputs.
- I_{IL} = -1μA for REFCKIN, LNKCTRL, POR, CSRW, CSSTROBE, LOOPEN, CNTRL1B, CNTRL0B, LOL2, CNTRL1, CNTRL0, LASERFLT, CNTRL2, TESTCK.
- I_{IL} (min) = -115μA; I_{IL} (max) = -33μA for OFCDEFB.
- Not production tested.

Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Optional Shipping Configuration**



Example: S2036A
28-pin SOIC package, shipped in the standard tube, dry packed.

FEATURES

- Functionally compliant with ANSI X3T11 Fibre Channel physical and transmission protocol standards
- S2042 transmitter incorporates phase-locked loop (PLL) providing clock synthesis from low-speed reference
- S2043 receiver PLL configured for clock and data recovery
- 1062, 531 and 266 Mb/s operation
- 10- or 20-bit parallel TTL compatible interface
- 1 watt typical power dissipation for chipset
- +3.3/+5V power supply
- Low-jitter serial PECL compatible interface
- Lock detect
- Local loopback
- Compact 44 or 52 PQFP package
- Fibre Channel framing performed by receiver
- Continuous downstream clocking from receiver
- TTL compatible outputs possible with +5V I/O power supply

APPLICATIONS

High-speed data communications

- Supercomputer
- Mainframe
- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes
- RAID drives
- Mass storage devices

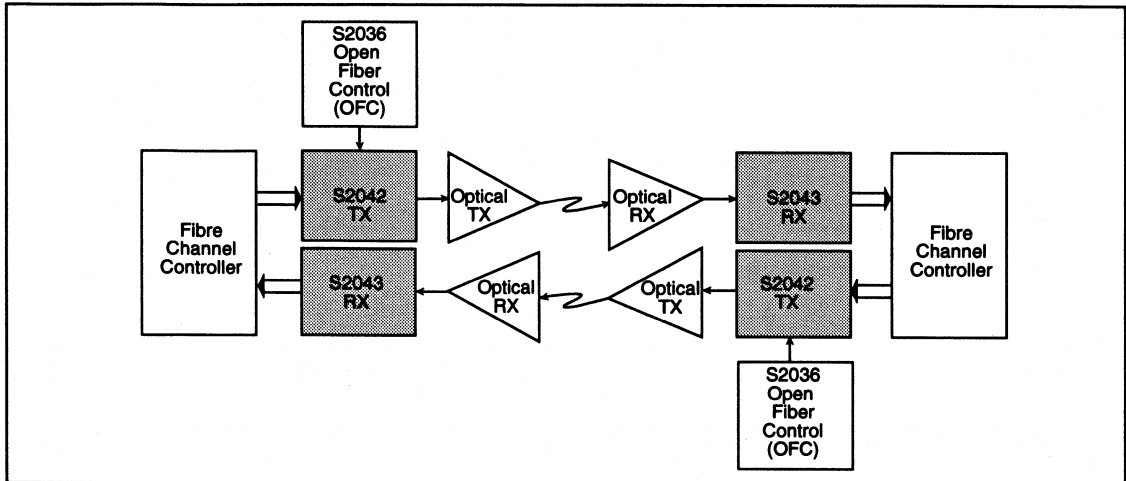
GENERAL DESCRIPTION

The S2042 and S2043 transmitter and receiver pair are designed to perform high-speed serial data transmission over fiber optic or coaxial cable interfaces conforming to the requirements of the ANSI X3T11 Fibre Channel specification. The chipset is selectable to 1062, 531 or 266 Mbit/s data rates with associated 10- or 20-bit data word.

The chipset performs parallel-to-serial and serial-to-parallel conversion and framing for block-encoded data. The S2042 on-chip PLL synthesizes the high-speed clock from a low-speed reference. The S2043 on-chip PLL synchronizes directly to incoming digital signals to receive the data stream. The transmitter and receiver each support differential PECL-compatible I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local loopback allows for system diagnostics. The TTL I/O section can operate from either a +3.3V or a +5V power supply. With a 3.3V power supply the chipset dissipates only 1 watt typically.

Figure 1 shows a typical network configuration incorporating the chipset. The chipset is compatible with AMCC's S2036 Open Fiber Control (OFC) device.

Figure 1. Typical Network Configuration



S2042/S2043 OVERVIEW

The S2042 transmitter and S2043 receiver provide serialization and deserialization functions for block-encoded data to implement a Fibre Channel interface. Operation of the S2042/S2043 chips is straightforward, as depicted in Figure 2. The sequence of operations is as follows:

Transmitter

1. 10/20-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver

1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10/20-bit parallel output

The 10/20-bit parallel data handled by the S2042 and S2043 devices should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters¹.

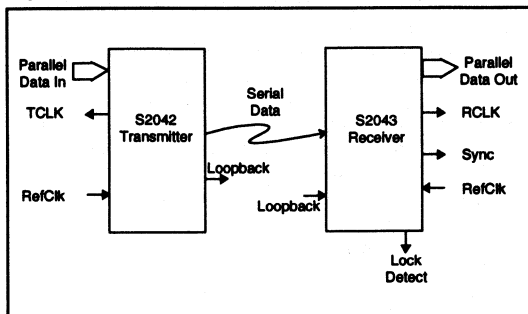
Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figure 3.

A lock detect feature is provided on the receiver, which indicates that the PLL is locked (synchronized) to the reference clock or the data stream.

Loopback

Local loopback is supported by the chipset, and provides a capability for performing offline testing of the interface to ensure the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

Figure 2. Interface Diagram

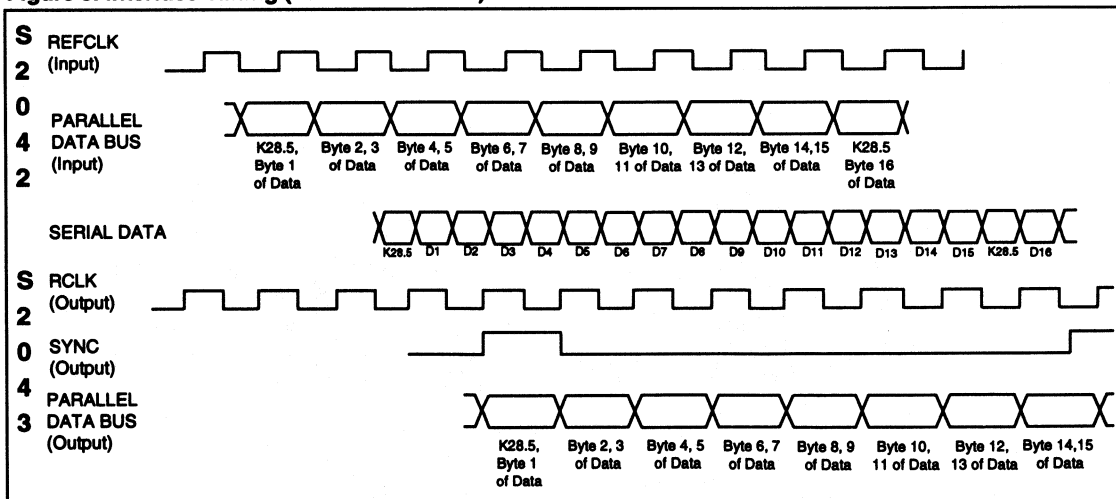


S2042 TRANSMITTER

Architecture/Functional Description

The S2042 transmitter accepts parallel input data and serializes it for transmission over fiber optic or coaxial cable media. The chip is fully compatible with the ANSI X3T11 Fibre Channel standard, and supports the Fibre Channel standard's data rates of 1062, 531 and 266 Mbit/sec.

Figure 3. Interface Timing (20-bit Data Words)



1. A.X. Widmer and P.A. Franaszek, "A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC 9391, May 1982.

The parallel input data word can be either 10 bits or 20 bits wide, depending upon DWS pin selection. A block diagram showing the basic chip operation is shown in Figure 4.

Parallel/Serial Conversion

The parallel-to-serial converter takes in 10-bit or 20-bit wide data from the input latch and converts it to a serial data stream. Parallel data is latched into the transmitter on the positive going edge of REFCLK. The data is then clocked synchronous to the clock synthesis unit serial clock into the serial output shift register. The shift register is clocked by the internally generated bit clock which is 10 times the REFCLK input frequency. The state of the serial outputs is controlled by the output enable pins, OE0 and OE1. D10 is transmitted first in 10-bit mode. D0 is transmitted first in 20-bit mode. Table 2 shows the mapping of the parallel data to the 8B/10B codes.

10-Bit/20-Bit Mode

The S2042 operates with either 10-bit or 20-bit parallel data inputs. Word width is selectable via the DWS pin. In 10-bit mode, D10–D19 are used and D0–D9 are ignored.

Reference Clock Input

The reference clock input (REFCLK) must be supplied with a single-ended AC coupled crystal clock source with 100 PPM tolerance to assure that the transmitted data meets the Fibre Channel frequency limits. The internal serial clock is frequency locked to the reference clock. The word rate clock (TCLK, TCLKN) output frequency is determined by the selected operating speed and word width. Refer to Table 1 for TCLK/TCLKN clock frequencies.

Table 1. Transmitter Operating Modes

RATESEL	DWS	REFSEL	Data Rate (Mbits/sec)	Word Width (Bits)	Reference Clock Frequency (MHz)	TCLK/TCLKN Frequency (MHz)
0	1	1	1062.5	10	106.25	53.125
0	0	0	1062.5	*20	53.125	53.125
1	1	1	531.25	*10	53.125	53.125
1	0	0	531.25	*20	26.5625	26.5625
Open	1	1	265.625	*10	26.5625	26.5625

* Not available in 44-pin package

Table 2. Data Mapping to 8b/10b Alphabetic Representation

TX(00:19) or RX(00:19) 8b/10b alphabetic representation	First Data Byte										Second Data Byte									
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	a	b	c	d	e	f	g	h	j		a	b	c	d	e	f	g	h	j	

↑ First bit transmitted in 20-bit mode

↑ First bit transmitted in 10-bit mode

Figure 4. S2042 Transmitter Block Diagram

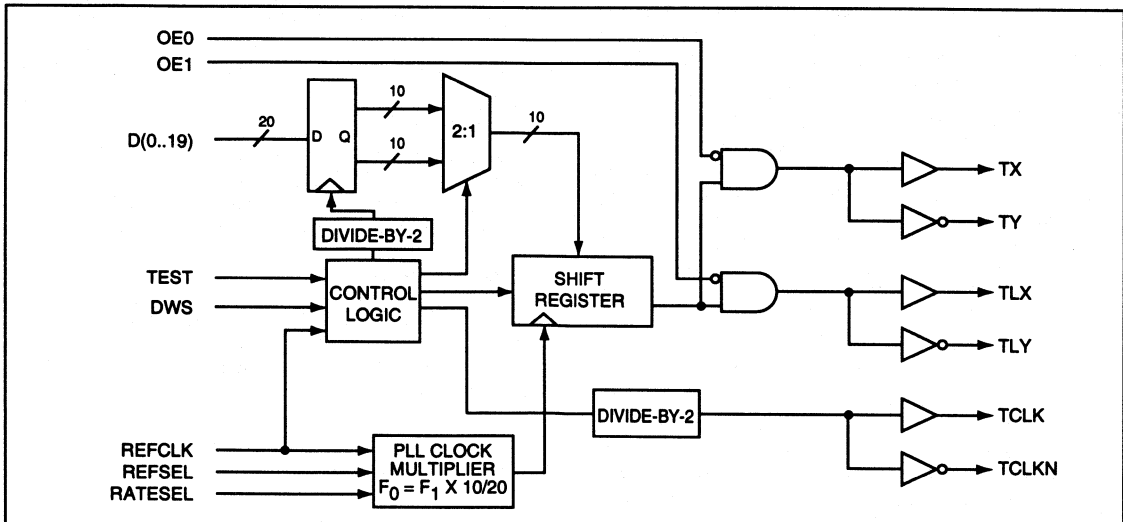


Figure 5. S2043 Block Diagram

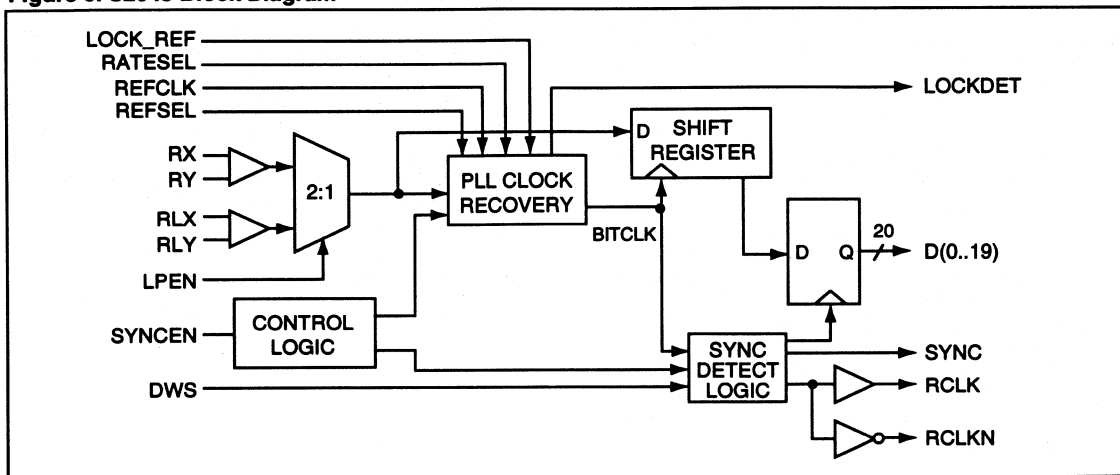


Table 3. Data Mapping to 8b/10b Alphabetic Representation

	First Data Byte										Second Data Byte									
TX[00:19] or RX[00:19]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
8b/10b alphabetic representation	a	b	c	d	e	f	g	h	i	j	a	b	c	d	e	f	g	h	i	j

↑ First bit received in 20-bit mode ↑ First bit received in 10-bit mode

S2043 RECEIVER

Architecture/Functional Description

The S2043 receiver is designed to implement the ANSI X3T11 Fibre Channel specification receiver functions. A block diagram showing the basic chip function is provided in Figure 5.

Whenever a signal is present, the S2043 attempts to achieve synchronization on both bit and transmission-word boundaries of the received encoded bit stream. Received data from the incoming bit stream is provided on the device's parallel data outputs.

The S2043 accepts serial encoded data from a fiber optic or coaxial cable interface. The serial input stream is the result of the serialization of 8B/10B encoded data by an FC compatible transmitter. Clock recovery is performed on-chip, with the output data presented to the Fibre Channel transmission layer as 10- or 20-bit parallel data. The chip is programmable to operate at the Fibre Channel specified operating frequencies of 1062, 531 and 266 Mbit/s.

Serial/Parallel Conversion

Serial data is received on the RX, RY pins. The PLL clock recovery circuit will lock to the data stream if the clock to be recovered is within ± 100 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The data is

then clocked into the serial to parallel output registers on the low going edge of RCLK. In 1062 Mbit/sec, 10-bit mode, data is clocked out on the falling edge of RCLK and RCLKN. The parallel data out can be either 10 or 20 bits wide determined by the state of the DWS pin. The word clock (RCLK) is synchronized to the incoming data stream word boundary by the detection of the fiber channel K28.5 synchronization pattern (0011111010, positive running disparity).

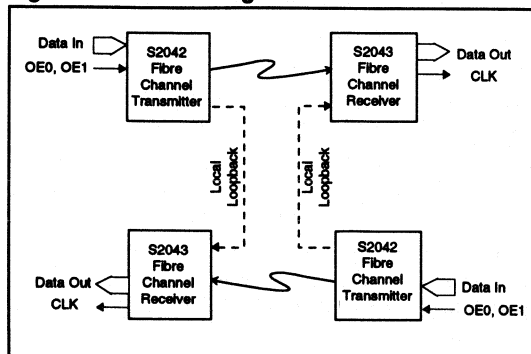
10-Bit/20-Bit Mode

The S2043 will operate with either 10-bit or 20-bit parallel data outputs. This option is selectable via the DWS pin. See Table 4. In 10-bit mode, D10-D19 are used and D0-D9 are driven to the logic high state.

Reference Clock Input

The reference clock input must be supplied with a single-ended AC coupled ECL/PECL crystal clock source at ± 100 PPM tolerance. See Table 4 for reference clock frequencies.

Figure 6. Interface Diagram



Framing

The S2043 provides SYNC character recognition and data word alignment of the TTL level compatible output data bus. In systems where the SYNC detect function is undesired, a LOW on the SYNCEN input disables the SYNC function and the data will be "un-framed".

When framing is disabled by low SYNCEN, the S2043 simply achieves bit synchronization within 250 bit times and begins to deliver parallel output data words whenever it has received full transmission words. No attempt is made to synchronize on any particular incoming character.

The SYNC output signal will go high whenever a K28.5 character (positive disparity) is present on the parallel data outputs. The SYNC output signal will be low at all other times. This is true whether the S2043 is operating in 10-bit mode or in 20-bit mode.

Lock Detect

The S2043 lock detect function indicates the state of the phase-locked loop (PLL) clock recovery unit. The PLL will indicate lock within 250 bit times after the start of receiving serial data inputs. If the serial data inputs have an instantaneous phase jump (from a serial switch, for example) the PLL will not indicate an out-of-lock state, but will recover the correct phase alignment within 250 bit times. If a run length of 64 bits is exceeded, or if the transition density is less than 12%, the loop will be declared out of lock and will attempt to re-acquire bit synchronization. When lock is lost, the PLL will shift from the serial input data to the reference clock, so that correct frequency downstream clocking will be maintained.

In any transfer of PLL control from the serial data to the reference clock, the RCLK/RCLKN output remains phase continuous and glitch free, assuring the integrity of downstream clocking.

Table 4. Receiver Operating Modes

RATESEL	DWS	REFSEL	Data Rate (Mbits/sec)	Word Width (Bits)	Reference Clock Frequency (MHz)	RCLK/RCLKN Frequency (MHz)
0	1	1	1062.5	10	106.25	53.125
0	0	0	1062.5	*20	53.125	53.125
1	1	1	531.25	*10	53.125	53.125
1	0	0	531.25	*20	26.5625	26.5625
Open	1	1	265.625	*10	26.5625	26.5625

* Not available in 44-pin package

Start-Up Procedure

The clock recovery PLL requires an initialization procedure to correctly achieve lock on the serial data inputs. At power-up or loss of lock, the PLL must first acquire frequency lock to the local reference clock. This can be accomplished by guaranteeing that no data is seen at the serial data inputs for a minimum of 10 ms upon power-up. If the serial data inputs cannot be controlled, then the S2043 can be put into the loopback mode and the loopback outputs of the S2042 must be quiescent for a minimum of 10 ms after power-up. In the 52-pin package, the -LOCK_REF pin can be connected to a 10 ms reset signal to initialize the PLL.

OTHER OPERATING MODES

Loopback

Local loopback requires a S2042 and a S2043 as shown in Figure 6. When enabled, serial data from the S2042 transmitter is sent to the S2043 receiver, where the clock is extracted and the data is deserialized. The parallel data is then sent to the subsystem for verification. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium. It also allows system diagnostics.

Operating Frequency Range

The S2042 and S2043 are optimized for operation at the Fibre Channel rates of 266, 531 and 1062 Mbit/s. Operation at other than Fibre channel rates is possible if the rate falls within $\pm 10\%$ of the nominal rate. REFCLK must be selected to be within 100 ppm of the desired byte or word clock rate.

Test Modes

The TEST pin on the S2042 and the SYNCEN pin on the S2043 provide a PLL bypass mode that can be used for operating the digital area of the chip. In this mode, clock signals are input through the reference clock pins. This can be used for testing the device during the manufacturing process or during an off-line self-test. Sync detection is always enabled in test mode.

S2042 Pin Descriptions

44 PQFP Pin #	52 PQFP Pin #	Name	Description
18–21, 24–27, 29–32, 35–38, 40–43	22–25, 28–31, 35–38, 41–44, 47–50	D[0:19]	INPUT—TTL Parallel data on this bus is clocked in on the rising edge of REFCLK. In 20-bit mode, D0 is transmitted first. In 10-bit mode, D10–19 are used, D0–D9 are ignored and D10 is transmitted first.
16	20	TEST	INPUT—Static TTL (Multi-level) This pin is used for factory testing. When not connected, REFCLK replaces the internal bit clock to facilitate factory testing. In normal use this input is wired to ground.
15	19	DWS	INPUT—Static: TTL The level on this pin selects the parallel data bus width. When LOW, a 20-bit parallel bus width is selected, and D[0–19] are active. When HIGH, a 10-bit parallel data bus is selected, D[10–19] are active, and D[0–9] are not used. (See Table 1.) A rising edge will reset the part (used for test).
1	1	OE1	INPUT—Static: TTL Active low output enable control for TLX/TLY outputs. TLX/TLY will go to the logic low state when disabled.
2	2	OE0	INPUT—Static: TTL Active low output enable control for TX/TY outputs. TX/TY will go to the logic low state when disabled.
13	16	REFCLK	INPUT—PECL (Externally capacitively coupled) A crystal controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is set by the REFSEL pin. (See Table 1.)
10 11	11 12	TCLKN TCLK	OUTPUTS—DIFFERENTIAL TTL Word rate clock true and complement. See Table 1 for frequency.
4 5	4 5	TLY TLX	OUTPUTS—DIFFERENTIAL PECL These outputs are functionally equivalent to TX and TY. They are intended to be used for loopback testing. Enabled by OE1.
7 8	8 9	TX TY	OUTPUTS—DIFFERENTIAL PECL These outputs transmit the serial data and drive 75Ω or 50Ω termination to Vcc - 2V. Enabled by OE0. TX is the positive output. TY is the negative output.
—	18	REFSEL	Input—Static: TTL (Multi-level) Used to select the reference clock frequency. (See Table 1.)
—	15	RATESEL	Input—Static: TTL (Multi-level) Used to select the operating speed of the transmitter. (See Table 1.)
17, 33, 39	21, 39, 45	ECLVCC	Core +3.3V
12	14	TTLGND	TTL Ground
14	17	TTLVCC	TTL Power Supply (+5V if TTL)
3, 9	3, 10	ECLIOVCC	PECL I/O Power Supply
17, 33, 39	6, 7	ECLIOVEE	PECL I/O Power Supply
23	27, 32	AVCC	Analog Power Supply
28	26, 33	AVEE	Analog Ground
6, 22, 34, 44	13, 34, 40, 46, 51, 52	ECLVEE	Core Ground

S2043 Pin Description

44 PQFP Pin #	52 PQFP Pin #	Name	Description
13–16, 18–21, 24–27, 29–32, 35–38	14, 15, 17, 18, 21, 22, 24, 25, 28, 29, 31, 32, 34, 35, 37, 38, 40, 42, 43, 45	D[0:19]	OUTPUTS—TTL The width of the parallel data bus is selected by the state of the DWS pin. Parallel data on this bus is clocked out on the falling edge of RCLK in 20-bit mode and on both the falling edges of RCLK and RCLKN in 1062.5 Mbit/sec, 10-bit mode. In 20-bit mode, D0 is the first bit received. In 10-bit mode, D10–D19 are used and D0–D9 are driven to the high state. In 10-bit mode, D10 is the first bit received.
43	52	LOCKDETN	OUTPUT—TTL When LOW, LOCKDETN indicates that the PLL is locked to the incoming data stream. When HIGH, it provides a system flag indicating that the PLL is locked to the local reference clock.
7	8	LPEN	INPUT—TTL When HIGH, LPEN selects the loopback differential serial input pins. When LOW, LPEN selects RX and RY (normal operation).
4	4	DWS	INPUT—Static: TTL The level on this pin selects the parallel data bus width. When LOW, a 20-bit parallel bus width is selected and D[0–19] are active. When HIGH, a 10-bit parallel data bus is selected. D[10–19] are active and D[0–9] will go HIGH. (See Table 4.) A rising edge will reset the internal counters. (Used for test.)
40 41	48 49	RCLKN RCLK	OUTPUTS—DIFFERENTIAL TTL Parallel data is clocked out on the falling edge of RCLK/RCLKN (see Timing Diagrams in Figures 15–18). After a sync word is detected, the period of the current RCLK and RCLKN is stretched to align with the word boundary. (See Table 4 for frequency.)
2	2	REFCLK	INPUT—PECL (Externally capacitively coupled) A free-running, crystal-controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is set by the REFSEL pin. (See Table 4.)
42	51	SYNC	OUTPUT—TTL Upon detection of a valid sync symbol, this output goes high for one RCLK period. When sync is active, the sync symbol shall be present on the parallel data bus bits D0–D9 in 20-bit mode and D10–D19 in 10-bit mode.
10 11	11 12	RLX RLY	INPUT—DIFFERENTIAL PECL (externally capacitively coupled) The serial loopback data inputs. RLX is the positive input, RLY is the negative input.
8 9	9 10	RX RY	INPUT—DIFFERENTIAL PECL (externally capacitively coupled) The received serial data inputs. RX is the positive input, RY is the negative input.
3	3	SYNCEN	INPUT—STATIC TTL (Multi-level) When HIGH, enables sync detection. Detection of the sync pattern (K28.5:0011111010, positive running disparity) will enable the word boundary for the data to follow. When open (not connected), REFCLK replaces internal bit clock to facilitate factory testing. In this mode of operation, sync detection is always enabled. When LOW, data is treated as unframed data.
—	30	REFSEL	INPUT—STATIC TTL (Multi-level) Used to select the reference clock frequency. (See Table 4.)
—	20	RATESEL	INPUT—STATIC TTL (Multi-level) Used to select the operating speed of the receiver. (See Table 4.)
—	50	LOCK_REF	INPUT—TTL When low, forces the PLL to lock to the REFCLK input and ignore the serial data inputs.
12, 34, 44	19, 23, 36, 44	TTLVCC	TTL Power Supply (+5V if TTL)
17, 28, 39	16, 33, 41, 46	TTLGND	TTL Ground
23, 33	13, 27, 39	ECLVCC	Core Power Supply
1, 22	1, 26, 47	ECLVEE	Core Ground
6	7	AVCC	Analog Power Supply
5	5, 6	AVEE	Analog Ground

Figure 7. 44 PQFP Package

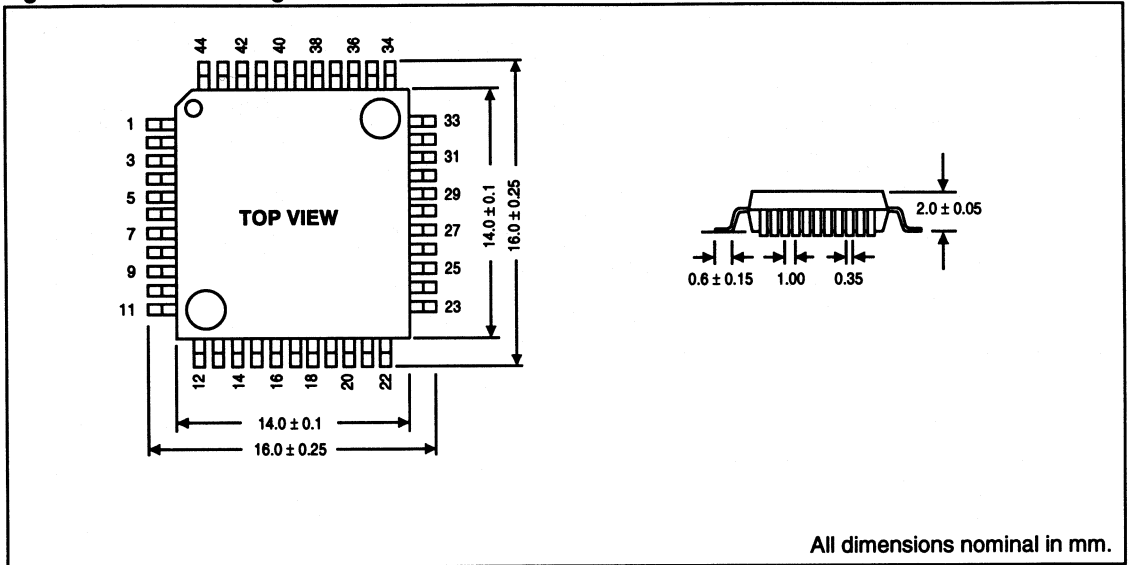
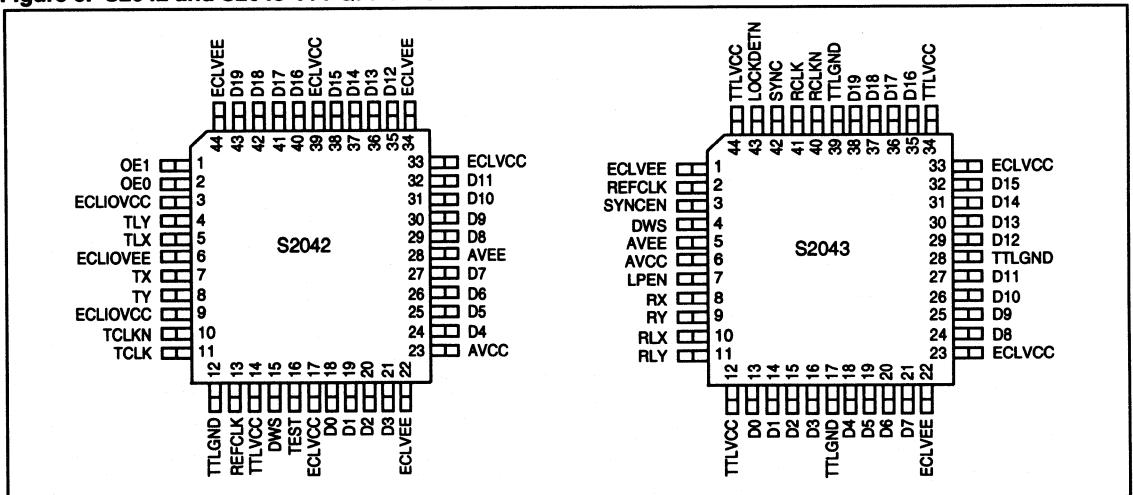
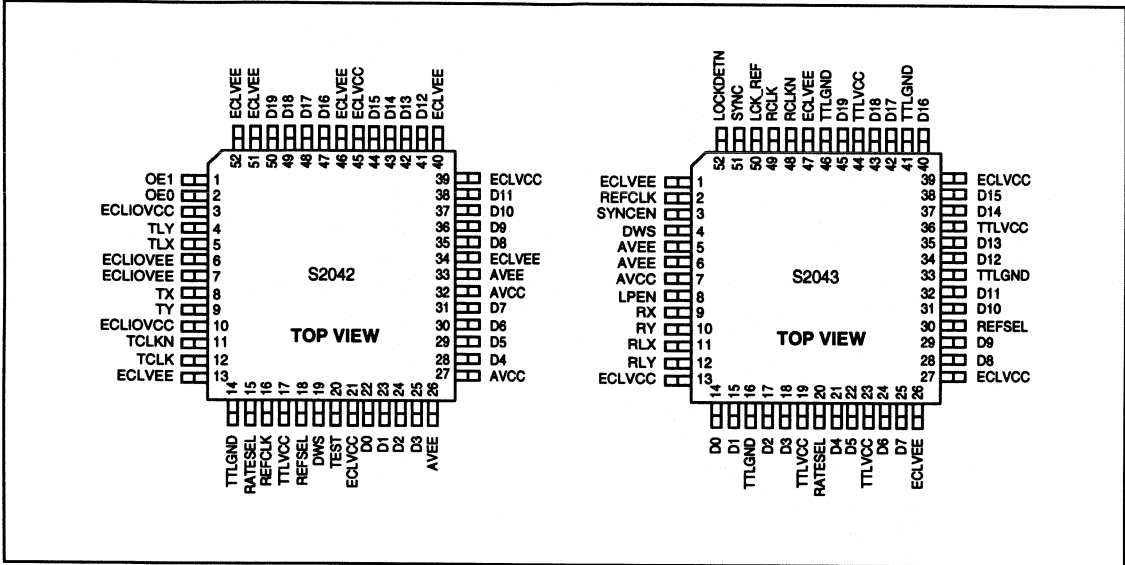


Figure 8. S2042 and S2043 44 PQFP Pinouts



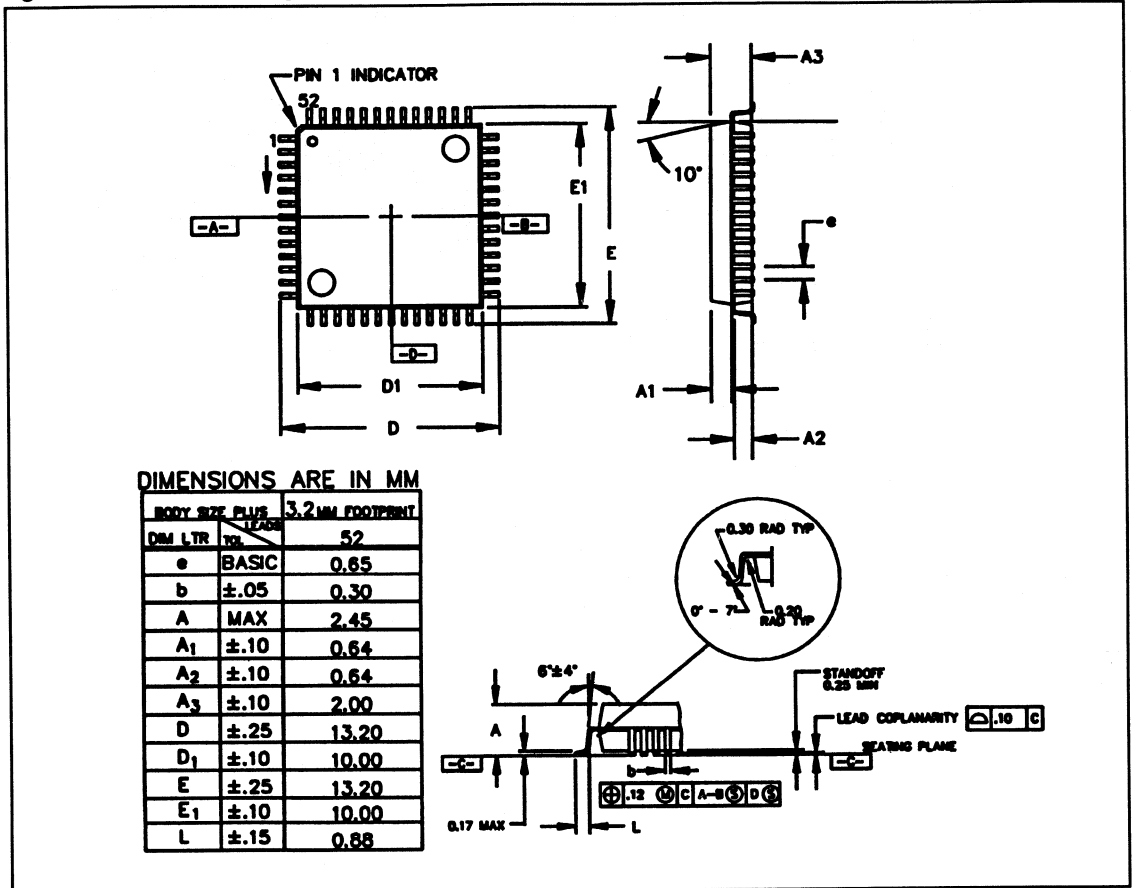
- TTLVCC = +5V or +3.3V
- AVCC = +3.3V
- ECLVCC = +3.3V
- ECLIOVCC = +3.3V
- TTLGND = 0V
- ECLVEE = 0V
- AVEE = 0V
- ECLIOVEE = 0V

Figure 9. S2042 and S2043 52 PQFP Pinouts



TTLVCC= +5V or +3.3V
AVCC= +3.3V
ECLVCC= +3.3V
ECLIOVCC = +3.3V
ECLIOVEE = 0V
TTLGND= 0V
ECLVEE= 0V
AVEE= 0V

Figure 10. 52 PQFP Package



Absolute Maximum Ratings

PARAMETER	MIN	TYP	MAX	UNIT
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Respect to GND	-0.5		+7.0	V
Voltage on any TTL Input Pin	-0.5		+5.5V	V
Voltage on any PECL Input Pin	0		VCC	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage		500		V

4

Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNIT
Ambient Temperature under Bias	0		70	°C
Junction Temperature under Bias			130	°C
Voltage on TTLVCC with Respect to GND				
5V Operation	4.75	5.0	5.25	V
3.3V Operation	3.13	3.3	3.47	V
Voltage on any TTL Input Pin	0		TTLVCC	V
Voltage on ECLVCC with respect to GND	3.13	3.3	3.47	V
Voltage on any PECL Input Pin	ECLVCC -2.0V		ECLVCC	V

Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance S2042	-100	+100	ppm	—
FT	Frequency Tolerance S2043	-100	+100	ppm	—
TD ₁₋₂	Symmetry	40	60	%	Duty Cycle at 50% pt.
T _R CR, T _R CF	REFCLK Rise and Fall Time	—	2	ns	20 – 80%
—	Random Jitter			ps	Peak-to-Peak

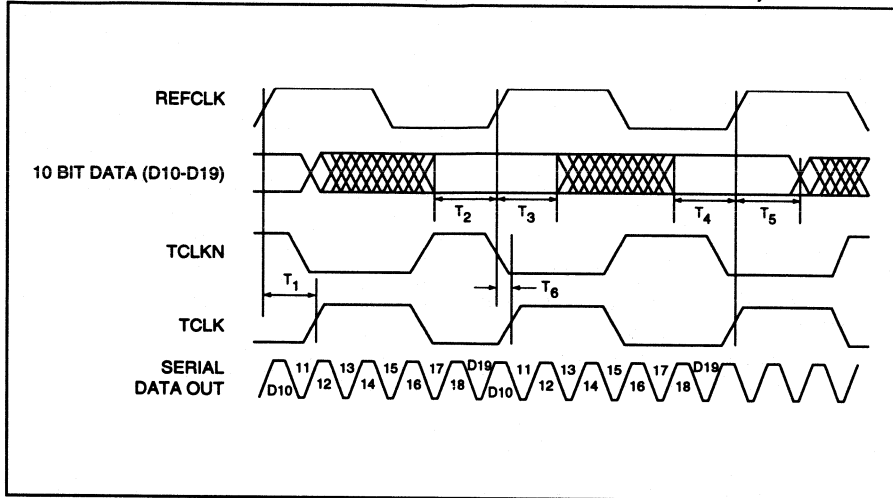
S2042 DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V _{OH}	Output HIGH Voltage (TTL) - 3.3V Power Supply - 3.3V Power Supply - 5V Power Supply	2.1			V	V _{CC} = min, I _{OH} = -2.4mA V _{CC} = min, I _{OH} = -.1mA V _{CC} = min, I _{OH} = -1mA
		2.2			V	
		2.7			V	
V _{OL}	Output LOW Voltage (TTL) - 3.3V Power Supply - 5V Power Supply			.5	V	V _{CC} = min, I _{OL} = 2.4mA V _{CC} = min, I _{OL} = 4mA
				.5	V	
V _{IH}	Input HIGH Voltage (TTL)	2.0	—	5.5	V	I _H ≤ 1mA at V _{IH} = 5.5V
V _{IL}	Input LOW Voltage (TTL)	0	—	0.8	V	—
I _{IH}	Input HIGH Current (TTL)	—	—	50	μA	V _{IN} = 2.4V
I _{IL}	Input LOW Current (TTL)	-500	—	-50	μA	V _{IN} = 0.5V
I _{CC}	Supply Current		123	160	mA	Outputs open, V _{CC} = V _{CC} max
P _D	Power Dissipation		.406	.554	W	Outputs open, V _{CC} = V _{CC} max
ΔV _{INCLK}	Single-ended REFLCK input swing	440	—	1300	mV	AC coupled
ΔV _{OUT}	Serial Output Voltage Swing	600	—	1600	mV	50Ω to V _{CC} -2.0V

S2043 DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V _{OH}	Output HIGH Voltage (TTL) - 3.3V Power Supply - 3.3V Power Supply - 5V Power Supply	2.1			V	V _{CC} = min, I _{OH} = -2.4mA V _{CC} = min, I _{OH} = -.1mA V _{CC} = min, I _{OH} = -1mA
		2.2			V	
		2.7			V	
V _{OL}	Output LOW Voltage (TTL) - 3.3V Power Supply - 5V Power Supply			.5	V	V _{CC} = min, I _{OL} = 2.4mA V _{CC} = min, I _{OL} = 8mA
				.5	V	
V _{IH}	Input HIGH Voltage (TTL)	2.0	—	5.5	V	I _H ≤ 1mA at V _{IH} = 5.5V
V _{IL}	Input LOW Voltage (TTL)	0	—	0.8	V	—
I _{IH}	Input HIGH Current (TTL)	—	—	50	μA	V _{IN} = 2.4V
I _{IL}	Input LOW Current (TTL)	-500	—	-50	μA	V _{IN} = 0.5V
I _{CC}	Supply Current - 10-Bit Mode - 20-Bit Mode		187	256	mA	Outputs open, V _{CC} = V _{CC} max Outputs open, V _{CC} = V _{CC} max
			194	267	mA	
P _D	Power Dissipation - 3.3V Supply, 10-Bit Mode - 3.3V Supply, 20-Bit Mode - 5V Supply, 10-Bit Mode - 5V Supply, 20-Bit Mode		.617	.887	W	Outputs open, V _{CC} = V _{CC} max Outputs open, V _{CC} = V _{CC} max Outputs open, V _{CC} = V _{CC} max Outputs open, V _{CC} = V _{CC} max
			.640	.925	W	
			.728	1.08	W	
			.778	1.142	W	
ΔV _{INCLK}	Single-ended REFLCK input swing	440	—	1300	mV	AC coupled
V _{DIFF}	Min. differential input voltage swing for differential PECL inputs	100		1300	mV	

Figure 11. Transmitter Timing Diagram (531, 266 Mbits/sec, 10-bit mode)



4

Figure 12. Transmitter Timing Diagram (531, 266 Mbits/sec, 20-bit mode)

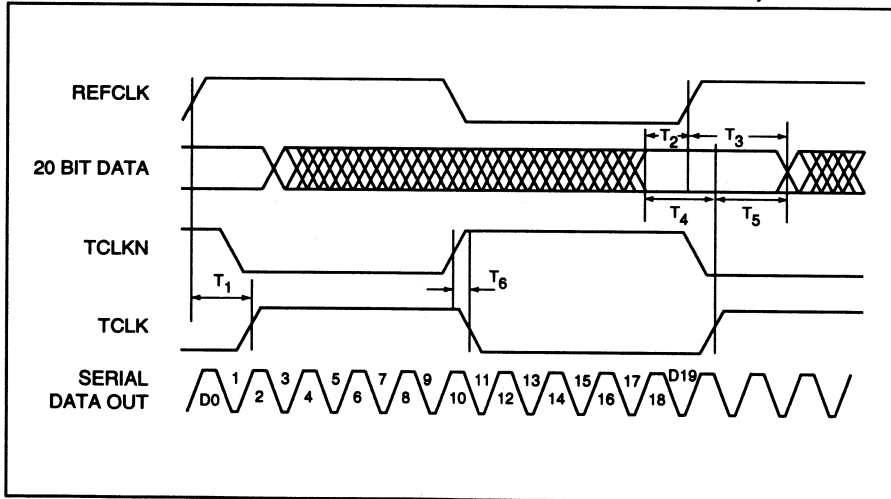


Figure 13. Transmitter Timing Diagram (1062 Mbits/sec, 10-bit mode)

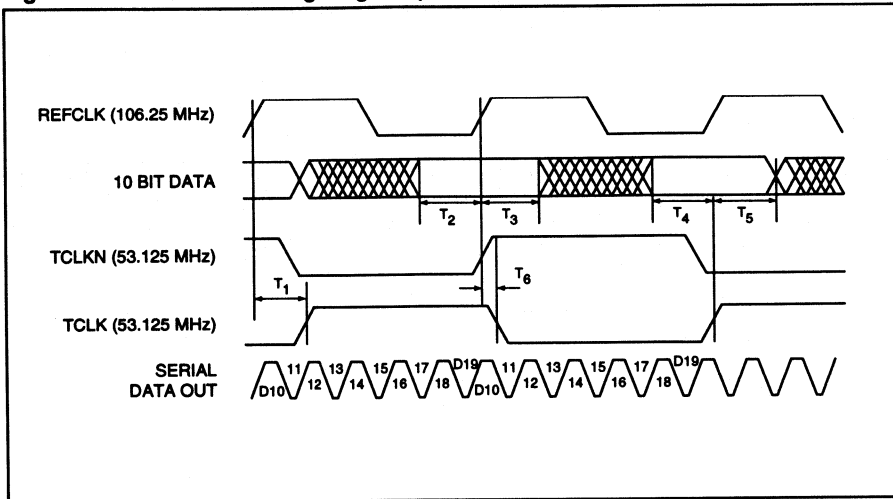


Figure 14. Transmitter Timing Diagram (1062 Mbits/sec, 20-bit mode)

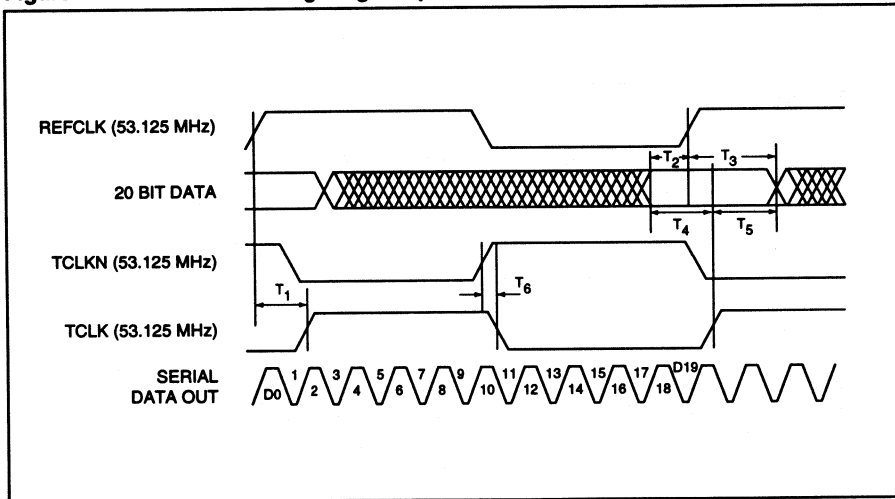


Table 5. AC Characteristics

Parameters	Description	Min	Max	Units	Conditions
T_1	REFCLK to TCLK	1.0	4.0	ns	—
T_2	Data setup w.r.t. REFCLK	1.0	—	ns	—
T_3	Data hold w.r.t. REFCLK	2.0	—	ns	—
T_4	Data setup w.r.t. TCLK	5	—	ns	—
T_5	Data hold w.r.t. TCLK	1	—	ns	—
T_{CR}, T_{CF}	TCLK rise and fall time	—	5.0	ns	10% to 90%, tested on a sample basis.
T_{SDR}, T_{SDF}	Serial data rise and fall	—	300	ps	20% to 80%, tested on a sample basis.
T_6	TCLK to TCLKN Skew	—	1	ns	Tested on a sample basis.
T_{DC}	TCLK, TCLKN Duty Cycle	40	60	%	—
Transmitter Output Jitter Allocation					
T_{jRMS}	Serial data output random jitter (RMS)	—	20	ps	RMS, tested on a sample basis. Measured with 1010 pattern.
T_{DJ}	Serial data output deterministic jitter (p-p)	—	100	ps	Peak-to-peak, tested on a sample basis. Measured with IDLE pattern.

Figure 15. Receiver Timing Diagram (531, 266 Mbits/sec, 10-bit mode)

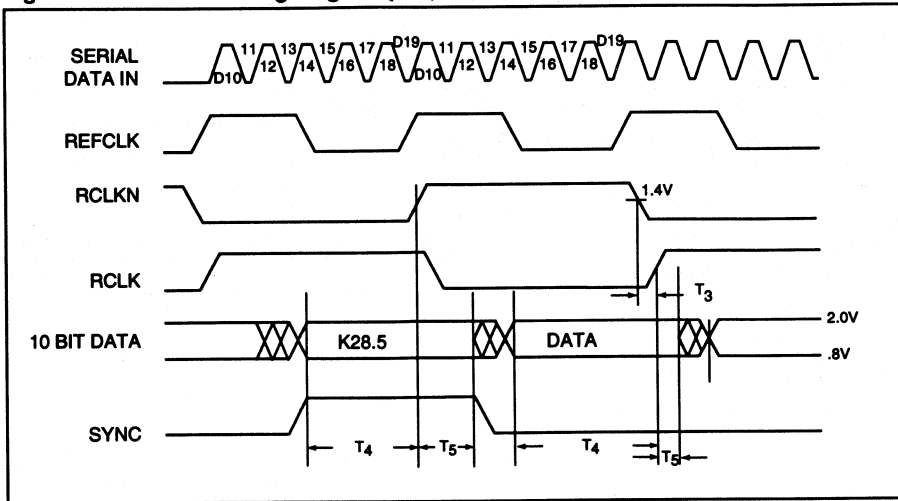
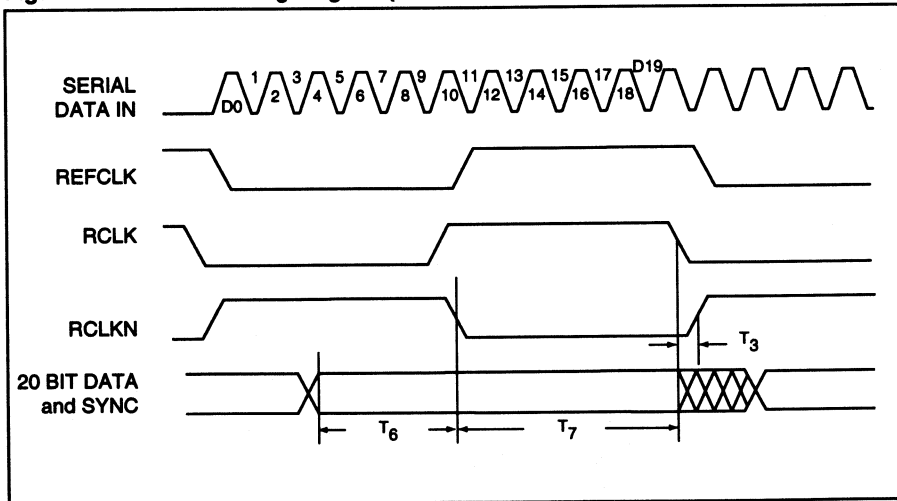
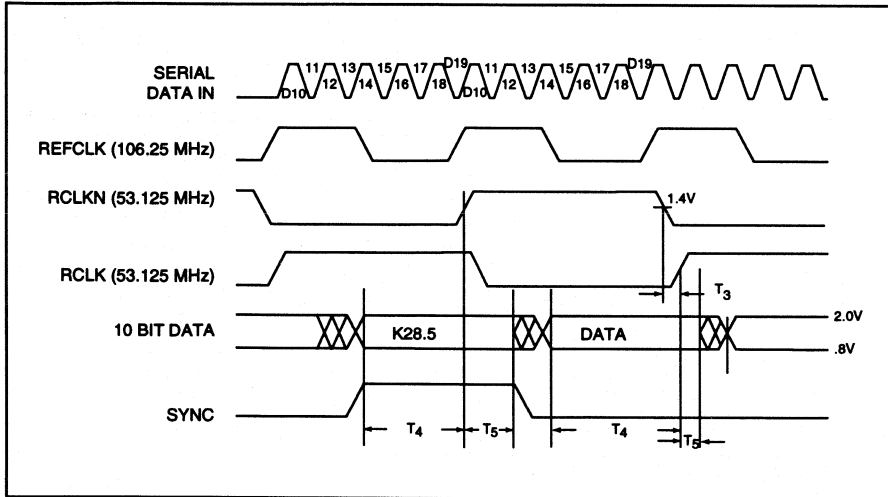


Figure 16. Receiver Timing Diagram (531 Mbits/sec, 20-bit mode)



B

Figure 17. Receiver Timing Diagram (1062 Mbits/sec, 10-bit mode)



4

Figure 18. Receiver Timing Diagram (1062 Mbits/sec, 20-bit mode)

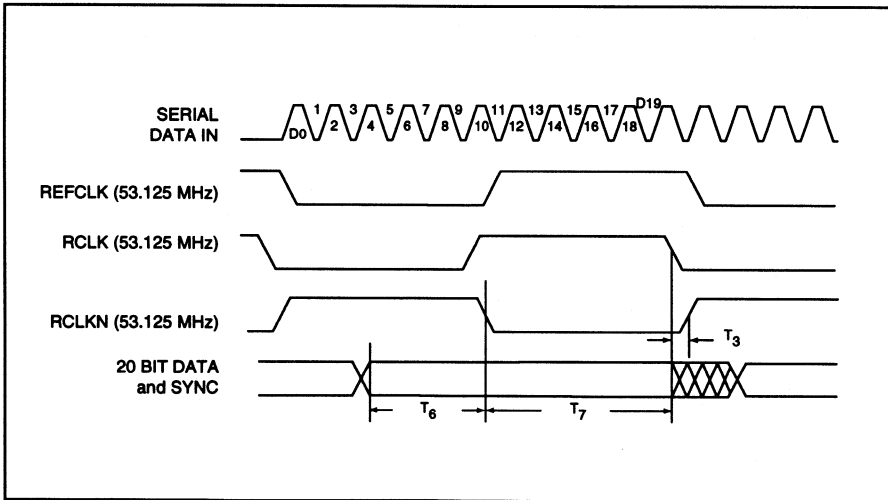


Table 6. S2043 Receiver Timing

Parameters	Description	Min	Max	Units	Conditions
T ₃	RCLK to RCLKN skew	—	1	ns	Tested on a sample basis.
T ₄	Data set-up time	3.0	—	ns	1062 Mbit/sec, 10-bit mode.
T ₅	Data hold time	1.5	—	ns	1062 Mbit/sec, 10-bit mode.
T ₆	Data set-up time	2.5	—	ns	1062, 531 Mbit/sec, 20-bit mode. 531, 266 Mbit/sec, 20-bit mode.
T ₇	Data hold time	7.5	—	ns	1062, 531 Mbit/sec, 20-bit mode. 531, 266 Mbit/sec, 20-bit mode.
T _{RCR} · T _{RCF}	RCLK rise and fall time	—	5.0	ns	10% to 90%, tested on a sample basis.
T _{DR} · T _{DF}	Data Output rise and fall time	—	5.0	ns	10% to 90%, tested on a sample basis.
T _{SDR} · T _{SDF}	Serial data input rise and fall	—	300	ps	20% to 80%.
T _{LOCK}	Data acquisition lock time @ <1.0625Gb/s	—	2.4	μs	8B/10B IDLE pattern sample basis
Duty Cycle	RCLK/RCLKN Duty Cycle	40%	60%		
Input Jitter Tolerance	Input data eye opening allocation at receiver input for BER ≤1E-12	30%	—	bit time	As specified in Fibre Channel FC-PH standard eye diagram jitter mask.

Max. Load = 15 pF.

Figure 19. Serial Input Rise and Fall Time

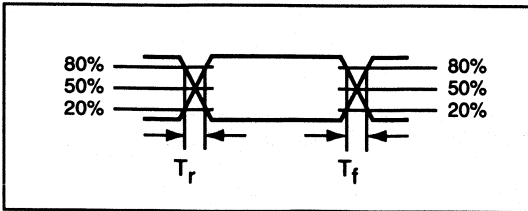


Figure 20. Serial Output Load

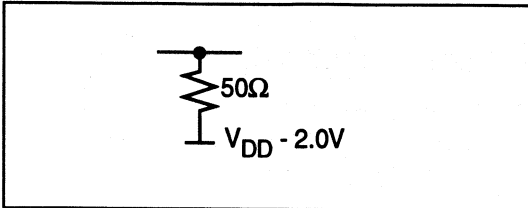


Figure 21. TTL Input and Output Rise and Fall Time

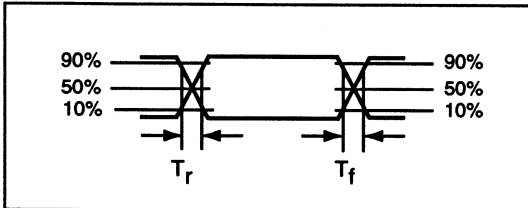
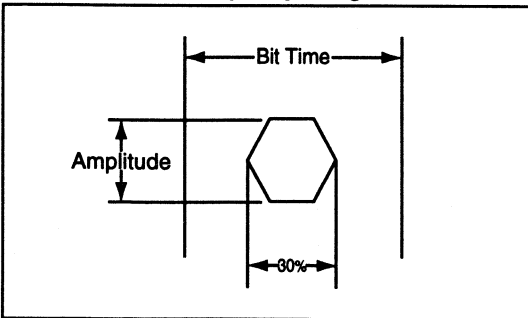


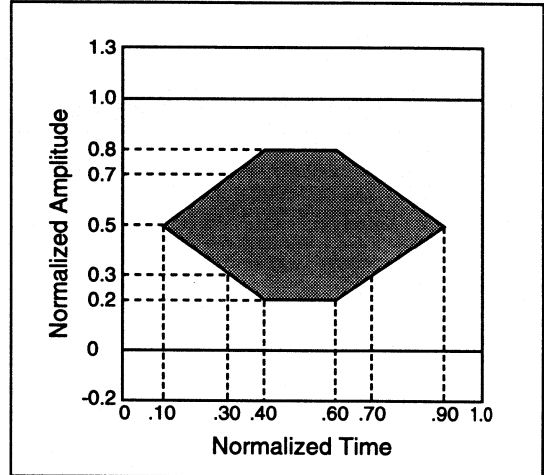
Figure 22. Receiver Input Eye Diagram Jitter Mask



ACQUISITION TIME

With the input eye diagram shown in Figure 23, the S2043 will recover data with a 10^{-9} BER within 50 bit times after an instantaneous phase shift of the incoming data.

Figure 23. Acquisition Time Eye Diagram



Ordering Information

GRADE	TRANSMITTER	PACKAGE	SPEED GRADE
S - commercial	2042	A - 44 PQFP B - 52 PQFP	05 - 531, 266 Mbit/s 10 - 1062, 531, 266 Mbit/s

GRADE	RECEIVER	PACKAGE	SPEED GRADE
S - commercial	2043	A - 44 PQFP B - 52 PQFP	05 - 531, 266 Mbit/s 10 - 1062, 531, 266 Mbit/s

X XXXX X - XX
Grade Part number Package Speed Grade

Example: S2042B-05 — S2042 in a 52 PQFP package operating at 531 or 266 Mbit/sec rates.

FEATURES

- Complies with the electrical and link levels of the Gigabaud Link Module (GLM) specification
- Functionally compliant with ANSI X3T11 Fibre Channel physical and transmission protocol standards
- S2044 transmitter incorporates phase-locked loop (PLL) providing clock synthesis from low-speed reference
- S2045 receiver PLL configured for clock and data recovery
- 1062 Mb/s (GLM), 531 Mb/s (HGLM) and 266 Mb/s (QGLM) operation
- 10- or 20-bit parallel TTL compatible interface
- 1 watt typical power dissipation for chipset
- +3.3/+5V power supply
- Low-jitter serial PECL compatible interface
- Lock detect
- Local loopback
- Compact 52 PQFP package
- Fibre Channel framing performed by receiver
- Continuous downstream clocking from receiver
- TTL compatible outputs possible with +5V I/O power supply

APPLICATIONS

High-speed data communications

- Mainframe
- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes
- RAID drives
- Mass storage devices

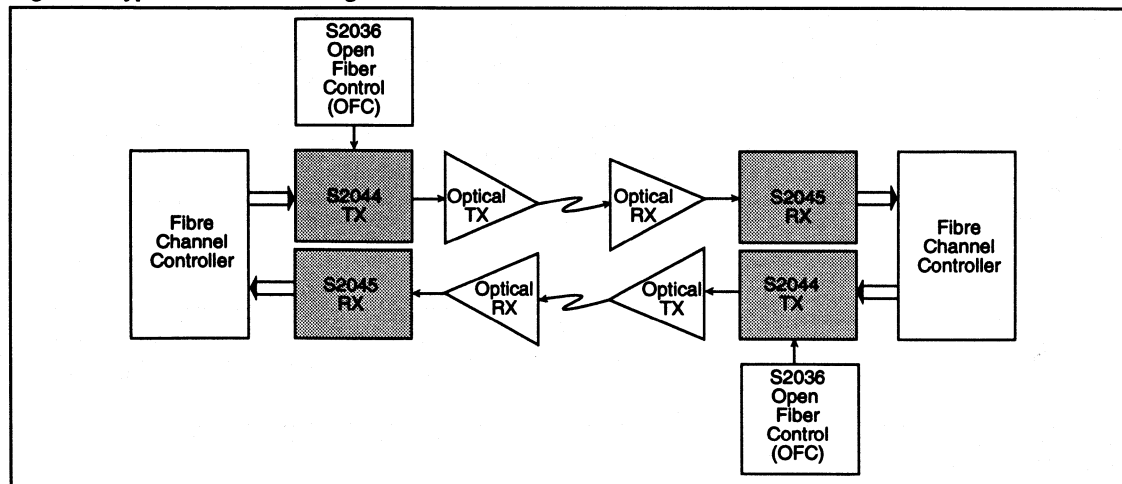
GENERAL DESCRIPTION

The S2044 and S2045 transmitter and receiver pair are designed to perform high-speed serial data transmission over fiber optic or coaxial cable interfaces conforming to the requirements of the ANSI X3T11 Fibre Channel specification. The chipset is Gigabaud Link Module (GLM) compliant and supports 1062 Mb/s (GLM) and 531 Mb/s Half-GLM (HGLM) and 266 Mb/s Quarter-GLM (QGLM) modes with associated 10 or 20-bit data word.

The chipset performs parallel-to-serial and serial-to-parallel conversion and framing for block-encoded data. The S2044 on-chip PLL synthesizes the high-speed clock from a low-speed reference. The S2045 on-chip PLL synchronizes directly to incoming digital signals, to receive the data stream. The transmitter and receiver each support differential PECL-compatible I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local loopback allows for system diagnostics. The I/O section can operate from either a +3.3V or a +5V power supply. With a 3.3V power supply the chipset dissipates only 1 watt typically.

Figure 1 shows a typical network configuration incorporating the chipset. The chipset is compatible with AMCC's S2036 Open Fiber Control (OFC) device.

Figure 1. Typical Network Configuration



S2044/S2045 OVERVIEW

The S2044 transmitter and S2045 receiver provide serialization and deserialization functions for block-encoded data to implement a Fibre Channel interface. Operation of the S2044/S2045 chips is straightforward, as depicted in Figure 2. The sequence of operations is as follows:

Transmitter

1. 10/20-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver

1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10/20-bit parallel output

The 10/20-bit parallel data handled by the S2044 and S2045 devices should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters¹.

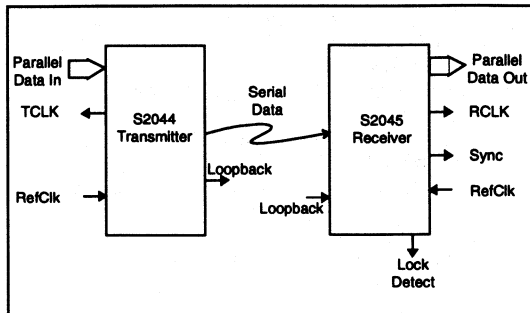
Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figure 3.

A lock detect feature is provided on the receiver, which indicates that the PLL is locked (synchronized) to the data stream.

Loopback

Local loopback is supported by the chipset, and provides a capability for performing offline testing of the interface to ensure the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

Figure 2. Interface Diagram

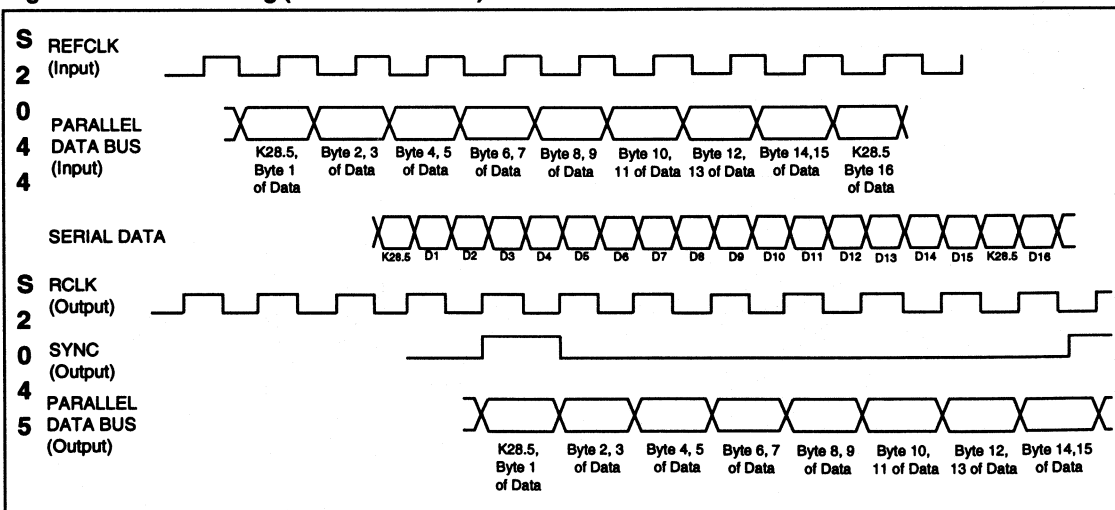


S2044 TRANSMITTER

Architecture/Functional Description

The S2044 transmitter accepts parallel input data and serializes it for transmission over fiber optic or coaxial cable media. The chip is fully compatible with the ANSI X3T11 Fibre Channel standard, and supports the Fibre Channel standard's data rates of 1062, 531 and 266 Mbit/sec.

Figure 3. Interface Timing (20-bit Data Words)



1. A.X. Widmer and P.A. Franaszek, "A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC 9391, May 1982.

The parallel input data word can be either 10 bits or 20 bits wide, depending upon DWS pin selection. A block diagram showing the basic chip function is shown in Figure 4.

Parallel/Serial Conversion

The parallel-to-serial converter takes in 10-bit or 20-bit wide data from the input latch and converts it to a serial data stream. Parallel data is latched into the transmitter on the positive going edge of REFCLK. The data is then clocked synchronous to the clock synthesis unit serial clock into the serial output shift register. The shift register is clocked by the internally generated bit clock which is 10 times the REFCLK input frequency. The state of the serial outputs is controlled by the output enable pins, OE0 and OE1. D10 is transmitted first in 10-bit mode. D0 is transmitted first in 20-bit mode. Table 2 shows the mapping of the parallel data to the 8B/10B codes.

10-Bit/20-Bit Mode

The S2044 operates with either 10-bit or 20-bit parallel data inputs. Word width is selectable via the DWS pin. In 10-bit mode, D10–D19 are used and D0–D9 are ignored.

Reference Clock Input

The reference clock input (REFCLK) must be supplied with a PECL single-ended AC coupled crystal clock source with 100 PPM tolerance to assure that the transmitted data meets the Fibre Channel frequency limits. The internal serial clock is frequency locked to the reference clock. The word rate clock (TCLK, TCLKN) output frequency is determined by the selected operating speed and word width. Refer to Table 1 for TCLK/TCLKN clock frequencies.

Table 1. Transmitter Operating Modes

RATESEL	DWS	REFSEL	Data Rate (Mbits/sec)	Word Width (Bits)	Reference Clock Frequency (MHz)	TCLK/TCLKN Frequency (MHz)
0	1	1	1062.5	10	106.25	53.125
0	0	0	1062.5	*20	53.125	53.125
1	1	1	531.25	*10	53.125	53.125
1	0	0	531.25	*20	26.5625	26.5625
Open	1	1	265.625	*10	26.5625	26.5625

* Not available in 44-pin package

Table 2. Data Mapping to 8b/10b Alphabetic Representation

TX[00:19] or RX[00:19] 8b/10b alphabetic representation	First Data Byte										Second Data Byte									
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	a	b	c	d	e	f	g	h	i	j	a	b	c	d	e	f	g	h	i	j

↑ First bit transmitted in 20-bit mode
↑ First bit transmitted in 10-bit mode

Figure 4. S2044 Block Diagram

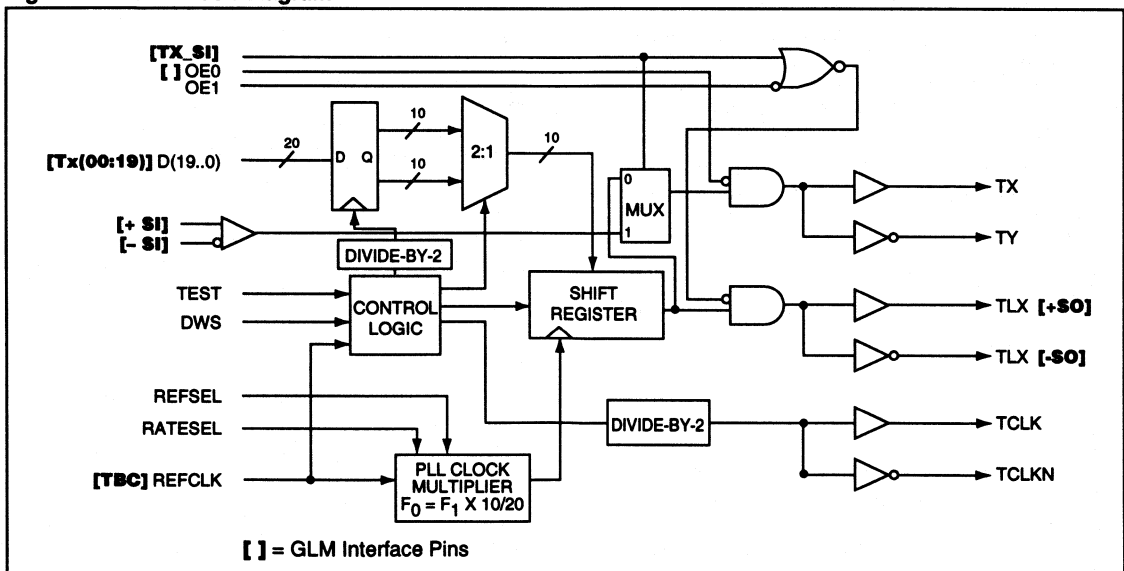


Figure 5. S2045 Block Diagram

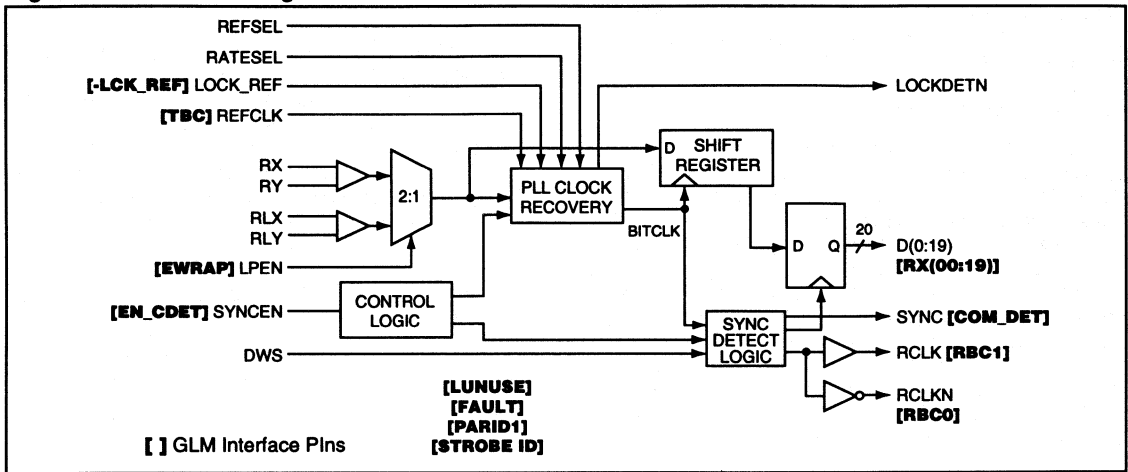


Table 3. Data Mapping to 8b/10b Alphabetic Representation

	First Data Byte										Second Data Byte									
TX(00:19) or RX(00:19)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
8b/10b alphabetic representation	a	b	c	d	e	i	f	g	h	j	a	b	c	d	e	i	f	g	h	j

↑ First bit received in 20-bit mode
↑ First bit received in 10-bit mode

S2045 RECEIVER

Architecture/Functional Description

The S2045 receiver is designed to implement the ANSI X3T11 Fibre Channel specification receiver functions. A block diagram showing the basic chip function is provided in Figure 5.

Whenever a signal is present, the S2045 attempts to achieve synchronization on both bit and transmission-word boundaries of the received encoded bit stream. Received data from the incoming bit stream is provided on the device's parallel data outputs.

The S2045 accepts serial encoded data from a fiber optic or coaxial cable interface. The serial input stream is the result of the serialization of 8B/10B encoded data by an FC compatible transmitter. Clock recovery is performed on-chip, with the output data presented to the Fibre Channel transmission layer as 10- or 20-bit parallel data. The chip is programmable to operate at the Fibre Channel specified operating frequencies of 1062, 531 and 266 Mbit/s.

Serial/Parallel Conversion

Serial data is received on the RX, RY pins. The PLL clock recovery circuit will lock to the data stream if the clock to be recovered is within ±100 PPM of the internally generated bit rate clock. The recovered clock is used to retim the input data stream. The data is

then clocked into the serial to parallel output registers. The parallel data out can be either 10 or 20 bits wide determined by the state of the DWS pin. The word clock (RCLK) is synchronized to the incoming data stream word boundary by the detection of the fiber channel K28.5 synchronization pattern (0011111010, positive running disparity).

10-Bit/20-Bit Mode

The S2045 will operate with either 10-bit or 20-bit parallel data outputs. This option is selectable via the DWS pin. See Tables 3 and 4. In 10-bit mode, D10–D19 are used and D0–D9 are driven to the logic high state.

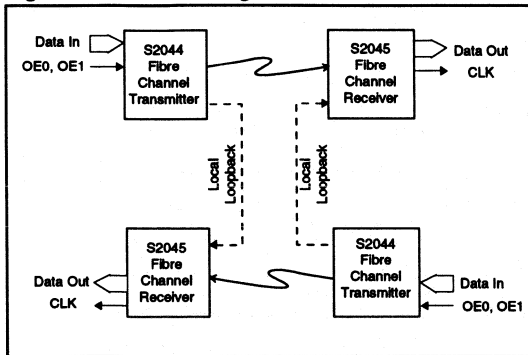
Reference Clock Input

The reference clock input must be supplied with a PECL single-ended AC coupled crystal clock source at ±100 PPM tolerance. See Table 4 for reference clock frequencies.

Framing

The S2045 provides SYNC character recognition and data word alignment of the TTL level compatible output data bus. During the data realignment process, the RCLK phase will be adjusted. No glitches will occur in the RCLK signal due to the realignment. In systems where the SYNC detect function is undesired, a LOW on the SYNCEN input disables the SYNC function and the data will be "un-framed".

Figure 6. Interface Diagram



When framing is disabled by low SYNCEN, the S2045 simply achieves bit synchronization within 250 bit times and begins to deliver parallel output data words whenever it has received full transmission words. No attempt is made to synchronize on any particular incoming character.

The SYNC output signal will go high whenever a K28.5 character (positive disparity) is present on the parallel data outputs. The SYNC output signal will be low at all other times. This is true whether the S2045 is operating in 10-bit mode or in 20-bit mode.

Lock Detect

The S2045 lock detect function indicates the state of the phase-locked loop (PLL) clock recovery unit. The PLL will indicate lock within 250 bit times after the start of receiving serial data inputs. If the serial data inputs have an instantaneous phase jump (from a serial switch, for example) the PLL will not indicate an out-of-lock state, but will recover the correct phase alignment within 250 bit times. If a run length of 64 bits is exceeded, or if the transition density is less than 12%, the loop will be declared out of lock and will attempt to re-acquire bit synchronization. When lock is lost, the PLL will shift from the serial input data to the reference clock, so that correct frequency downstream clocking will be maintained.

In any transfer of PLL control from the serial data to the reference clock, the RCLK/RCLKN output remains phase continuous and glitch free, assuring the integrity of downstream clocking.

Start-Up Procedure

The clock recovery PLL requires an initialization procedure to correctly achieve lock on the serial data inputs. At power-up or loss of lock, the PLL must first acquire frequency lock to the local reference clock. This can be

Table 4. Receiver Operating Modes

RATESEL	DWS	REFSEL	Data Rate (Mbits/sec)	Word Width (Bits)	Reference Clock Frequency (MHz)	RCLK/RCLKN Frequency (MHz)
0	1	0	1062.5	10	106.25	53.125
0	0	1	1062.5	*20	53.125	53.125
1	1	1	531.25	10	53.125	53.125
1	0	0	531.25	*20	26.5625	26.5625
Open	1	1	265.625	*10	26.5625	26.5625

* Not available in 44-pin package

accomplished connecting the -LOCK_REF pin to a 10 ms reset signal. If this is not possible, the PLL can also be initialized by guaranteeing that no data is seen at the serial data inputs for a minimum of 10 ms upon power-up. If the serial data inputs cannot be controlled, then the S2045 can be put into the loopback mode and the loopback outputs of the S2044 must be quiescent for a minimum of 10 ms after power-up.

OTHER OPERATING MODES

Loopback

Local loopback requires a S2044 and a S2045 as shown in Figure 6. When enabled, serial data from the S2044 transmitter is sent to the S2045 receiver, where the clock is extracted and the data is deserialized. The parallel data is then sent to the subsystem for verification. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium. It also allows system diagnostics.

Operating Frequency Range

The S2044 and S2045 are optimized for operation at the Fibre Channel rates of 265.625, 531.25, and 1062.5 Mbit/s. Operation in other than Fibre channel rates is possible if the rate falls within ±10% of the nominal rate. REFCLK must be selected to be within 100 ppm of the desired byte or word clock rate.

Test Modes

The TEST pin on the S2044 and the SYNCEN pin on the S2045 provide a PLL bypass mode that can be used for operating the digital area of the chip. In this mode, clock signals are input through the reference clock pins. This can be used for testing the device during the manufacturing process or during an off-line self-test. Sync detection is always enabled in test mode.

S2044 Pin Descriptions

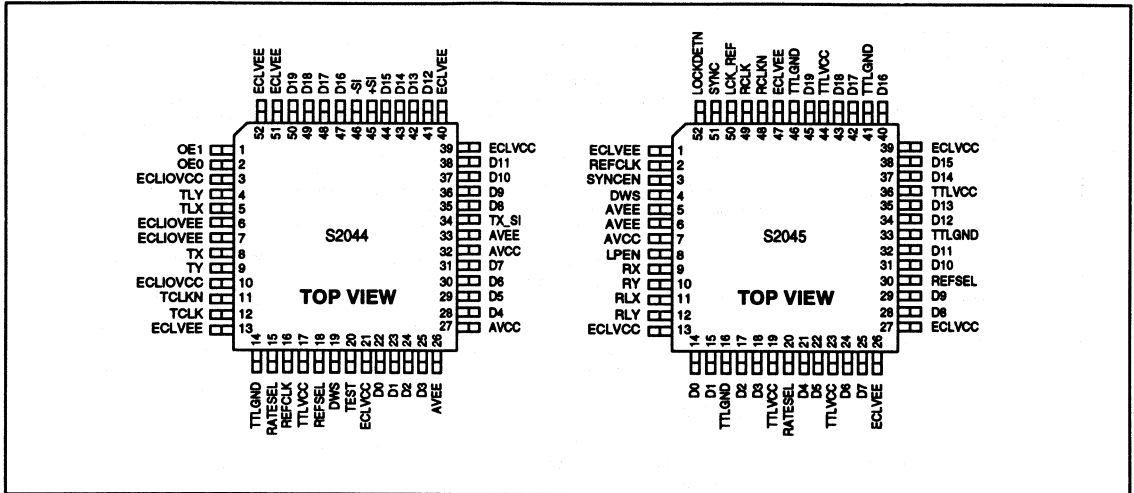
52 PQFP Pin #	Name	Description
22–25, 28–31, 35–38, 41–44, 47–50	D[0:19]	INPUT—TTL Parallel data on this bus is clocked in on the rising edge of REFCLK. In 20-bit mode, D0 is transmitted first. In 10-bit mode, D10-D19 are used, D0-D9 are ignored and D10 is transmitted first.
20	TEST	INPUT—Static TTL (Multi-level) This pin is used for factory testing. When not connected, REFCLK replaces the internal bit clock to facilitate factory testing. In normal use this input is wired to ground.
19	DWS	INPUT—Static: TTL The level on this pin selects the parallel data bus width. When LOW, a 20-bit parallel bus width is selected, and D[0–19] are active. When HIGH, a 10-bit parallel data bus is selected, D[10–19] are active, and D[0–9] are not used. (See Table 1.) A rising edge will reset the part (used for test).
1	OE1	INPUT—Static: TTL Active low output enable control for TLX/TLY outputs. TLX/TLY will go to the logic low state when disabled.
2	OE0	INPUT—Static: TTL Active low output enable control for TX/TY outputs. TX/TY will go to the logic low state when disabled.
16	REFCLK	INPUT—PECL (Externally capacitively coupled) A free running crystal controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is set by the REFSEL pin. (See Table 1.)
11 12	TCLKN TCLK	OUTPUTS—DIFFERENTIAL TTL Word rate clock true and complement. See Table 1 for frequency.
4 5	TLY TLX	OUTPUTS—DIFFERENTIAL PECL These outputs are functionally equivalent to TX and TY. They are intended to be used for loopback testing. Enabled by OE1.
8 9	TX TY	OUTPUTS—DIFFERENTIAL PECL These outputs transmit the serial data and drive 75Ω or 50Ω termination to Vcc - 2V. Enabled by OE0. TX is the positive output. TY is the negative output.
18	REFSEL	Input—Static: TTL (Multi-level) Used to select the reference clock frequency. (See Table 1.)
15	RATESEL	Input—Static: TTL (Multi-level) Used to select the operating speed of the transmitter. (See Table 1.)
21, 39	ECLVCC	Core +3.3V
14	TTLGND	TTL Ground
17	TTLVCC	TTL Power Supply (+5V if TTL)
3, 10	ECLIOVCC	PECL I/O Power Supply
6, 7	ECLIOVEE	PECL I/O Power Supply
27, 32	AVCC	Analog Power Supply
26, 33	AVEE	Analog Ground
13, 40, 51, 52	ECLVEE	Core Ground
34	TX_SI	INPUT—MULTI-LEVEL This signal determines where the data which is presented to the link comes from and whether the ±SO signals are enabled. When this input is low, the TX/TY outputs transmit the serialized data from the parallel transmit data lines. When this input is high the TX/TY outputs transmit the data from the ±SI inputs.
45 46	+SI -SI	INPUTS—DIFFERENTIAL PECL These inputs are a serial data stream (1.0625 Gb/s, 531.25 Mb/s, 265.625) which shall control the link modulation (TX/TY) if the TX_SI input is high.

S2045 Pin Description

52 PQFP Pin #	Name	Description
14, 15, 17, 18, 21, 22, 24, 25, 28, 29, 31, 32, 34, 35, 37, 38, 40, 42, 43, 45	D[0:19]	OUTPUTS—TTL The width of the parallel data bus is selected by the state of the DWS pin. Parallel data on this bus is clocked out on the falling edge of RCLK. In 20-bit mode, D0 is the first bit received. In 10-bit mode, D10–D19 are used and D0–D9 are driven to the high state. In 10-bit mode, D10 is the first bit received.
52	LOCKDETN	OUTPUT—TTL When LOW, LOCKDETN indicates that the PLL is locked to the incoming data stream. When HIGH, it provides a system flag indicating that the PLL is locked to the local reference clock.
8	LPEN	INPUT—TTL When HIGH, LPEN selects the loopback differential serial inputs pins (RLX, RLY). When LOW, LPEN selects RX and RY (normal operation).
4	DWS	INPUT—Static: TTL The level on this pin selects the parallel data bus width. When LOW, a 20-bit parallel bus width is selected and D[0–19] are active. When HIGH, a 10-bit parallel data bus is selected, D[10–19] are active and D[0–9] will go HIGH. (See Table 4.) A rising edge will reset the internal counters. (Used for test.)
48 49	RCLKN RCLK	OUTPUTS—DIFFERENTIAL TTL The falling edge of RCLK outputs a new word on the data bus. After a sync word is detected, the period of the current RCLK and RCLKN is stretched to align with the word boundary. (See Table 4 for frequency.)
2	REFCLK	INPUT—PECL (Externally capacitively coupled) A free-running, crystal-controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is set by the REFSEL pin. (See Table 4.)
51	SYNC	OUTPUT—TTL Upon detection of a valid sync symbol, this output goes high for one RCLK period. When sync is active, the sync symbol shall be present on the parallel data bus bits D0–D9 in 20-bit mode or D10–D19 in 10-bit mode.
11 12	RLX RLY	INPUT—DIFFERENTIAL PECL (externally capacitively coupled) The serial loopback data inputs. RLX is the positive input, RLY is the negative input.
9 10	RX RY	INPUT—DIFFERENTIAL PECL (externally capacitively coupled) The received serial data inputs. RX is the positive input, RY is the negative input.
3	SYNCEN	INPUT—STATIC TTL (Multi-level) When HIGH, enables sync detection. Detection of the sync pattern (K28.5:0011111010, positive running disparity) will determine the word boundary for the data to follow. When open (not connected), REFCLK replaces internal bit clock to facilitate factory testing. In this mode of operation, sync detection is always enabled. When LOW, data is treated as unframed data.
30	REFSEL	INPUT—STATIC TTL (Multi-level) Used to select the reference clock frequency. (See Table 4.)
20	RATESEL	INPUT—STATIC TTL (Multi-level) Used to select the operating speed of the receiver. (See Table 4.)
50	LOCK_REF	INPUT—TTL When low, forces the PLL to lock to the REFCLK input and ignore the serial data inputs.
19, 23, 36, 44	TTLVCC	TTL Power Supply (+5V if TTL)
16, 33, 41, 46	TTLGND	TTL Ground
13, 27, 39	ECLVCC	Core Power Supply
1, 26, 47	ECLVEE	Core Ground
7	AVCC	Analog Power Supply
5, 6	AVEE	Analog Ground

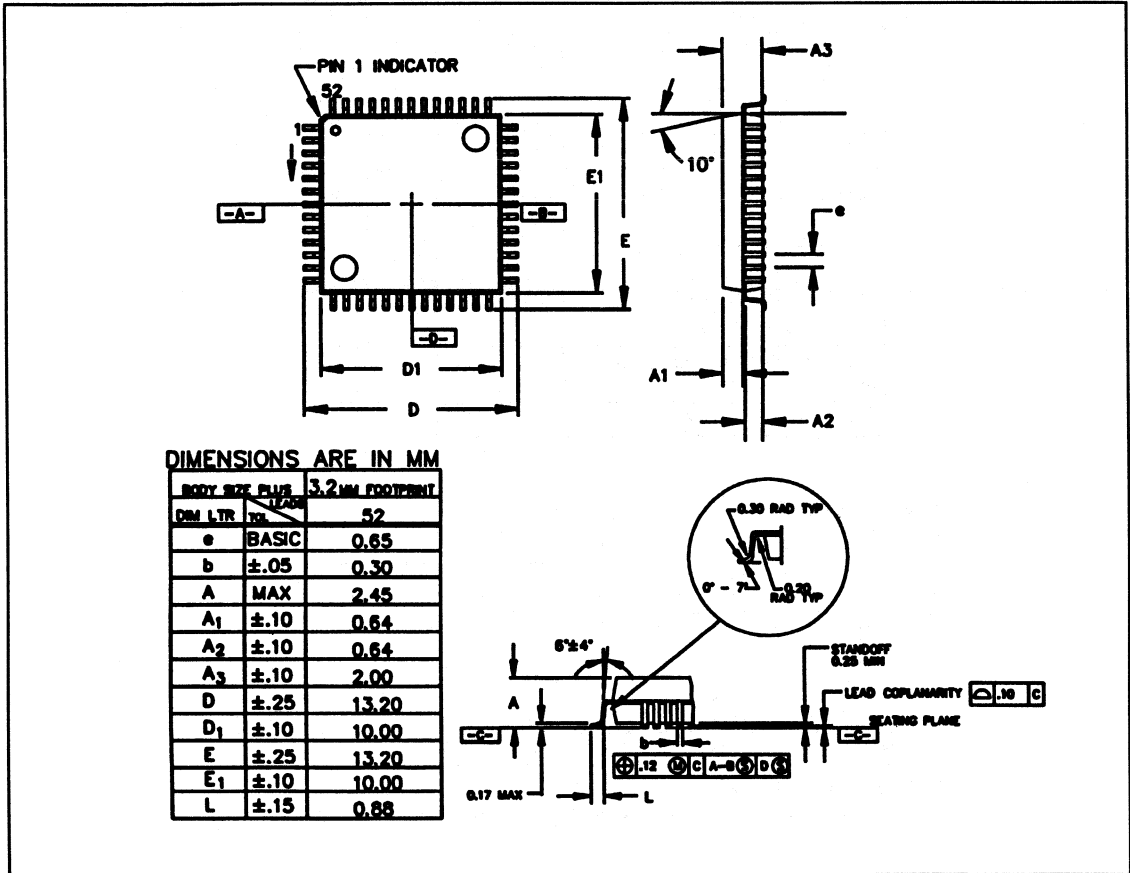
4

Figure 7. S2044 and S2045 52 PQFP Pinouts



- TTLVCC = +5V or +3.3V
- AVCC = +3.3V
- ECLVCC = +3.3V
- ECLIOVCC = +3.3V
- ECLIOVEE = 0V
- TTLGND = 0V
- ECLVEE = 0V
- AVEE = 0V

Figure 8. 52 PQFP — (10mm x 10mm) Plastic Quad Flat Pack



Absolute Maximum Ratings

PARAMETER	MIN	TYP	MAX	UNIT
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Respect to GND	-0.5		+7.0	V
Voltage on any TTL Input Pin	-0.7		VCC +6V	V
Voltage on any PECL Input Pin	0		ECL/ VCC	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage		500		V

Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNIT
Ambient Temperature under Bias	0		70	°C
Junction Temperature under Bias			130	°C
Voltage on TTLVCC with Respect to GND				
5V Operation	4.75	5.0	5.25	V
3.3V Operation	3.13	3.3	3.47	V
Voltage on any TTL Input Pin	0		5.25	V
Voltage on ECLVCC with respect to GND	3.13	3.3	3.47	V
Voltage on any PECL Input Pin	ECL/VCC -2.0		ECL/VCC	V

S2044 DC Characteristics

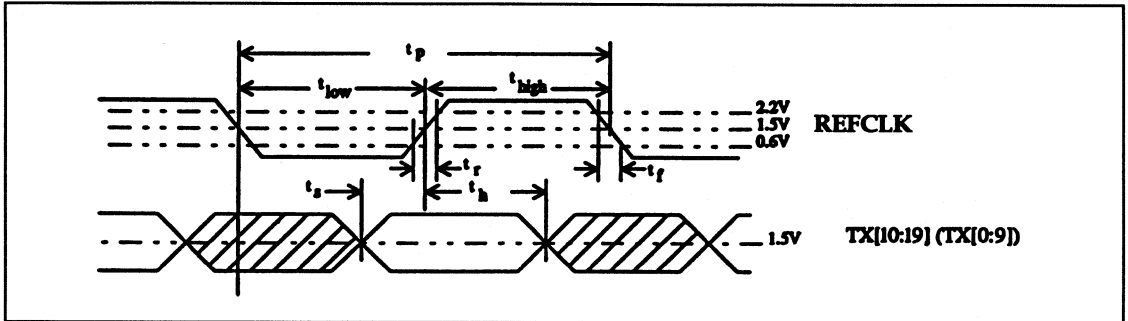
Parameters	Description	Min	Typ	Max	Units	Conditions
V _{OH}	Output HIGH Voltage (TTL) - 3.3V Power Supply - 3.3V Power Supply - 5V Power Supply	2.1			V	V _{CC} = min, I _{OH} = -2.4mA V _{CC} = min, I _{OH} = -.1mA V _{CC} = min, I _{OH} = -1mA
		2.2			V	
		2.7			V	
V _{OL}	Output LOW Voltage (TTL) - 3.3V Power Supply - 5V Power Supply			.5	V	V _{CC} = min, I _{OL} = 2.4mA V _{CC} = min, I _{OL} = 4mA
				.5	V	
V _{IH}	Input HIGH Voltage (TTL)	2.0	—	5.5	V	I _H ≤ 1mA at V _{IH} = 5.5V
V _{IL}	Input LOW Voltage (TTL)	0	—	0.8	V	—
I _{IH}	Input HIGH Current (TTL)	—	—	50	μA	V _{IN} = 2.4V
I _{IL}	Input LOW Current (TTL)	-500	—	-50	μA	V _{IN} = 0.5V
I _{CC}	Supply Current		123	160	mA	Outputs open, V _{CC} = V _{CC} max
P _D	Power Dissipation		.406	.554	W	Outputs open, V _{CC} = V _{CC} max
ΔV _{INCLK}	Single-ended REFCLK input swing	440	—	1300	mV	AC coupled
ΔV _{OUT}	Serial Output Voltage Swing	600	—	1600	mV	50Ω to V _{CC} -2.0V

S2045 DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V _{OH}	Output HIGH Voltage (TTL) - 3.3V Power Supply - 3.3V Power Supply - 5V Power Supply	2.1			V	V _{CC} = min, I _{OH} = -2.4mA V _{CC} = min, I _{OH} = -.1mA V _{CC} = min, I _{OH} = -1mA
		2.2			V	
		2.7			V	
V _{OL}	Output LOW Voltage (TTL) - 3.3V Power Supply - 5V Power Supply			.5	V	V _{CC} = min, I _{OL} = 2.4mA V _{CC} = min, I _{OL} = 8mA
				.5	V	
V _{IH}	Input HIGH Voltage (TTL)	2.0	—	5.5	V	I _H ≤ 1mA at V _{IH} = 5.5V
V _{IL}	Input LOW Voltage (TTL)	0	—	0.8	V	—
I _{IH}	Input HIGH Current (TTL)	—	—	50	μA	V _{IN} = 2.4V
I _{IL}	Input LOW Current (TTL)	-500	—	-50	μA	V _{IN} = 0.5V
I _{CC}	Supply Current - 10-Bit Mode - 20-Bit Mode		187	256	mA	Outputs open, V _{CC} = V _{CC} max Outputs open, V _{CC} = V _{CC} max
			194	267	mA	
P _D	Power Dissipation - 3.3V Supply, 10-Bit Mode - 3.3V Supply, 20-Bit Mode - 5V Supply, 10-Bit Mode - 5V Supply, 20-Bit Mode		.617	.887	W	Outputs open, V _{CC} = V _{CC} max Outputs open, V _{CC} = V _{CC} max Outputs open, V _{CC} = V _{CC} max Outputs open, V _{CC} = V _{CC} max
			.640	.925	W	
			.728	1.08	W	
			.778	1.142	W	
ΔV _{INCLK}	Single-ended REFCLK input swing	440	—	1300	mV	AC coupled
V _{DIFF}	Min. differential input voltage swing for differential PECL inputs	100		1300	mV	

Timing

The data on the TX[00:09] (TX[00:19]) data bus will be sampled on every rising edge of REFCLK. The data will be serialized and transmitted onto the serial link if EWRAP is low and TX_SI is low. The figure below illustrates the timing requirements of REFCLK with respect to the TX[10:19] (TX[0:9]) signals, minimum high and low durations, and the rising and falling slew rate magnitudes. In addition, this system supplied clock must not have more jitter than $\pm 20\%$ of a baud interval.

REFCLK Timing Diagram

REFCLK Timing Table

Parameter	Symbol	Min.	Max.	Units	Comments ¹
Frequency 26.5625 MHz 53.125 MHz	f	25.5598 53.119	26.5652 53.131	MHz	This is dependent on the link rate and the data path width.
Jitter 265.625 MBaud 531.25 MBaud 1062.5 MBaud			753 376 188	ps pk-pk	This is the maximum total jitter allowed by the Fiber Channel standard.
Period (f=26.5625 MHz)	t _p	37.64	37.66	ns	
Period (f=53.125 MHz)	t _p	18.82	18.83	ns	
REFCLK Low Time	t _{low}	6		ns	
REFCLK High Time	t _{high}	6		ns	
TX Setup to REFCLK (GLM, HGLM)	t _s	2		ns	
TX Setup to REFCLK (QGLM, EGLM)	t _s	6		ns	
TX Hold From REFCLK	t _h	3.3		ns	
REFCLK Rise Time	t _r	0.5	3.2	ns	This applies to the REFCLK input.
REFCLK Fall Time	t _f	0.5	3.2	ns	This applies to the REFCLK input.

1. All parameters are for outputs driven into a 35pF lumped capacitive load.

Serial Data Timing Table (TLX, TLY; TX, TY)

Parameters	Description	Min	Max	Units	Conditions
T _{J,RMS}	Serial data output random jitter (RMS)	—	20	ps	RMS, tested on a sample basis. Measured with 1010 pattern.
T _{DJ}	Serial data output deterministic jitter (p-p)	—	100	ps	Peak-to-peak, tested on a sample basis. Measured with IDLE pattern.
T _{SDR} , T _{SDF}	Serial data rise and fall	—	300	ps	20% to 80%, tested on a sample basis.

Tested per Figure 10.

Timing

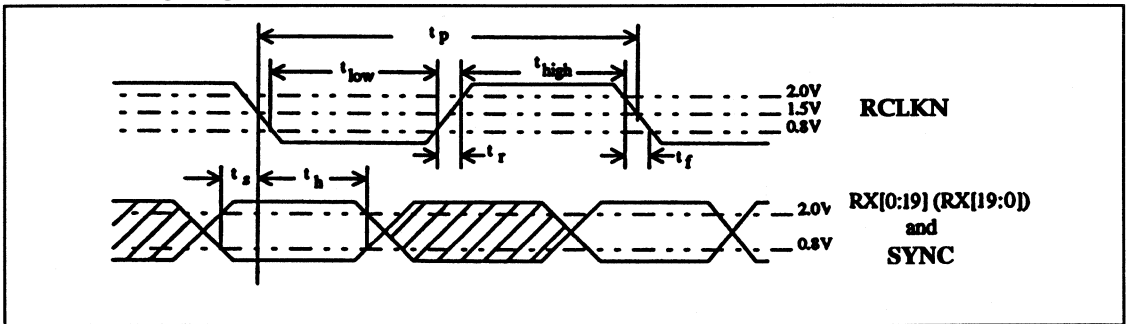
This section will detail the timing requirements of all of the signals on the GLM interface. All timing is measured into a lumped 35pf capacitive load.

RBC[0] Timing

When -LCK_REF is pulled low, RCLKN should be in local phase lock with TBC within 500µs. -LCK_REF, when activated, shall stay low for a duration of at least 500µs if receiver frequency lock is to be expected. After local phase lock has been acquired, and when EWRAP is high, 2500 baud times after -LCK_REF is driven high, RCLKN shall be in phase lock with REFCLK. After local phase lock has been acquired, and when EWRAP is low, 250 baud times after -LCK_REF is driven high, RCLKN shall be in phase lock with the incoming serial data stream.

When a 53 MHz GLM family module is in frequency lock (either with REFCLK or a serial data stream) RCLKN shall never have a high level duration (>2.0v) which is less than 6.5 ns, nor a low level duration (<0.8v) which is less than 5.8 ns (no clock shivering shall occur). At byte realignment, RCLKN clock states are to be extended rather than truncated). When the GLM family module is in frequency lock (either with REFCLK or a serial data stream) and -LCK_REF has been inactive for at least 2500 baud times the minimum instantaneous period shall always be greater than 18.36 ns. When the PLL in the GLM is adjusting to a new phase or a new frequency, where both the old and new frequencies are valid Fibre Channel frequencies, RCLKN shall never have a period less than 18.36 ns. In response to an input data phase jump, the GLM shall meet the requirements of FC-PH clause 5.3 transparent to the host.

RCLKN Timing Diagram



Serial Data Input Timing Table (RLX, RLY; RX, RY)

Parameters	Description	Min	Max	Units	Conditions
R_{SDR}, R_{SDF}	Serial data input rise and fall	—	300	ps	20% to 80%.
T_{LOCK}	Data acquisition lock time @ <1.0625Gb/s	—	2.4	µs	8B/10B IDLE pattern sample basis
Input Jitter Tolerance	Input data eye opening allocation at receiver input for BER $\leq 1E-12$	30%	—	bit time	As specified in Fibre Channel FC-PH standard eye diagram jitter mask. (See Figure 12.) For BER $\leq 1E-9$ see Figure 13.

RCLKN Timing Table

Parameter	Symbol	Min.	Max.	Units	Comments ²
Frequency 26.5625 MHz 53.125 MHz	f	25.5598 53.119	25.5652 53.131	MHz	This is dependent on the link rate and the data path width.
Period in Lock	t _p	18.36		ns	In frequency lock ³ .
Out of Lock Period (f=26.5625 MHz)	t _{oolp}	18.83		ns	Not in frequency lock.
Out of Lock Period (f=53.125 MHz)	t _{oolp}	9.412		ns	Not in frequency lock.
RCLKN Low Time (f=53.125 MHz)	t _{low}	5.8		ns	
RCLKN High Time (f=53.125 MHz)	t _{high}	6.5		ns	
RCLKN Duty Cycle (f=26.5625 MHz)		40%	60%	period	In frequency lock.
RX Setup to RCLKN (f=53.125 MHz)	t _s	2.5		ns	
RX Setup to RCLKN (f=26.5625 MHz)	t _s	6.0		ns	
RX Hold From RCLKN	t _h	7.5		ns	
RCLK/RCLKN Rise Time	t _r	.75	2.4	ns	This applies to the RCLKN output.
RCLKN Fall Time	t _f	0.7	3.0	ns	This applies to the RCLKN output.

2. All parameters are for outputs driven into a 35pf lumped capacitive load.
3. This is the absolute minimum RCLKN period while in frequency lock and must account for any adjustments to the clock to allow for a change in phase or frequency on the received serial link.

Figure 9. Serial Input Rise and Fall Time

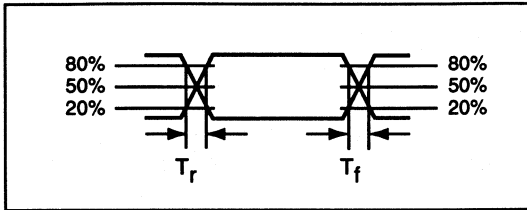


Figure 10. Serial Output Load

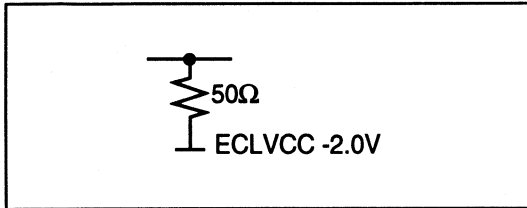


Figure 11. TTL Input Rise and Fall Time

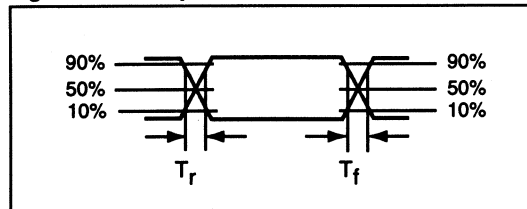
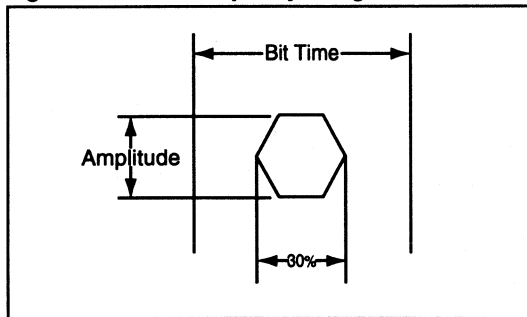


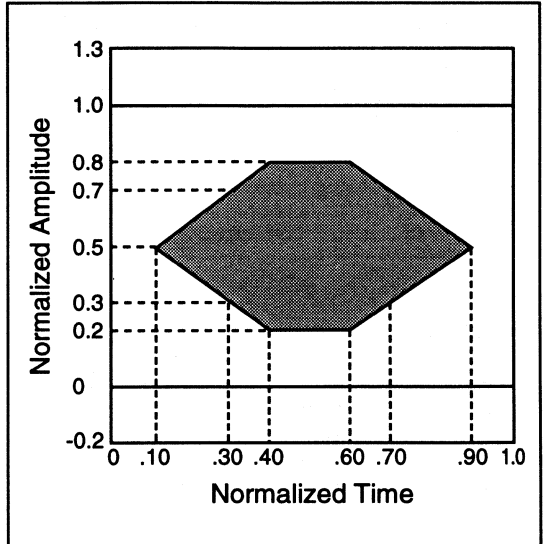
Figure 12. Receiver Input Eye Diagram Jitter Mask



ACQUISITION TIME

With the input eye diagram shown in Figure 13, the S2045 will recover data with a 10^{-9} BER within 50 bit times after an instantaneous phase shift of the incoming data. Note: This is only valid after a 10 ms initial reset has been applied on power up.

Figure 13. Acquisition Time Eye Diagram

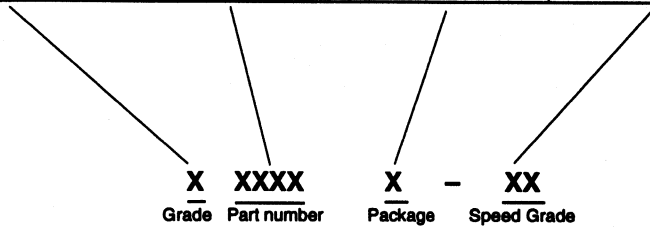


Ordering Information

GRADE	TRANSMITTER	PACKAGE	SPEED GRADE
S – commercial	2044	B – 52 PQFP	5 – 531, 266 Mbit/s 10 – 1062, 531 and 266 Mbit/s

GRADE	RECEIVER	PACKAGE	SPEED GRADE
S – commercial	2045	B – 52 PQFP	5 – 531, 266 Mbit/s 10 – 1062, 531 and 266 Mbit/s

4



Example: S2044B-5—S2044 in a 52 PQFP package operating at 531 or 266 Mbits/sec rates.

FEATURES

- Functionally compliant with ANSI X3T11 Fibre Channel physical and transmission protocol standards
- Transmitter incorporates phase-locked loop (PLL) providing clock synthesis from low-speed reference
- Receiver PLL configured for clock and data recovery
- 1062, 531 and 266 Mb/s operation
- 10-bit parallel TTL compatible interface
- 1 watt typical power at 3.3V
- +3.3 power supply
- Low-jitter serial PECL compatible interface
- Lock detect
- Local loopback
- Compact 52 PQFP package
- Fibre Channel framing performed by receiver
- Continuous downstream clocking from receiver
- TTL compatible outputs possible with +5V I/O power supply

APPLICATIONS

High-speed data communications

- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes
- RAID drives
- Mass storage devices

GENERAL DESCRIPTION

The S2052 transmitter and receiver chip is designed to perform high-speed serial data transmission over fiber optic or coaxial cable interfaces conforming to the requirements of the ANSI X3T11 Fibre Channel specification. The chip runs at 1062.5, 531.25 and 266 Mbit/s data rates with associated 10-bit data word.

The chip performs parallel-to-serial and serial-to-parallel conversion and framing for block-encoded data. The transmitter's on-chip PLL synthesizes the high-speed clock from a low-speed reference. The receiver's on-chip PLL synchronizes directly to incoming digital signal to receive the data stream. The transmitter and receiver each support differential PECL-compatible I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local loopback mode is provided for system diagnostics. The I/O section can operate from either a +3.3V or a +5V power supply. With a 3.3V power supply the chip dissipates only 1 watt typically.

Figure 1 shows a typical configuration incorporating the chip, which is compatible with AMCC's S2036 Open Fiber Control (OFC) device.

Figure 1. Typical Network Configuration

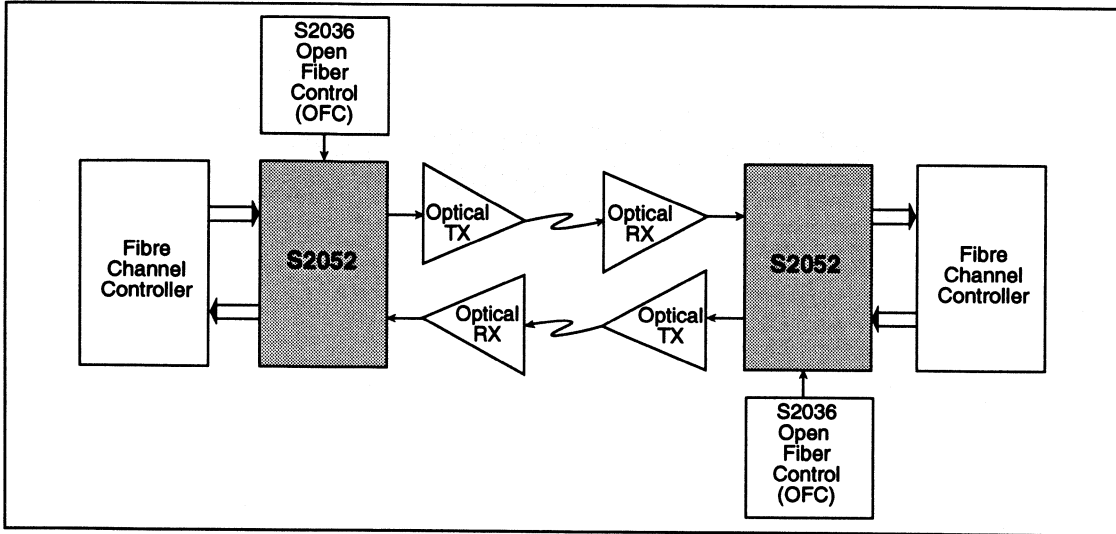
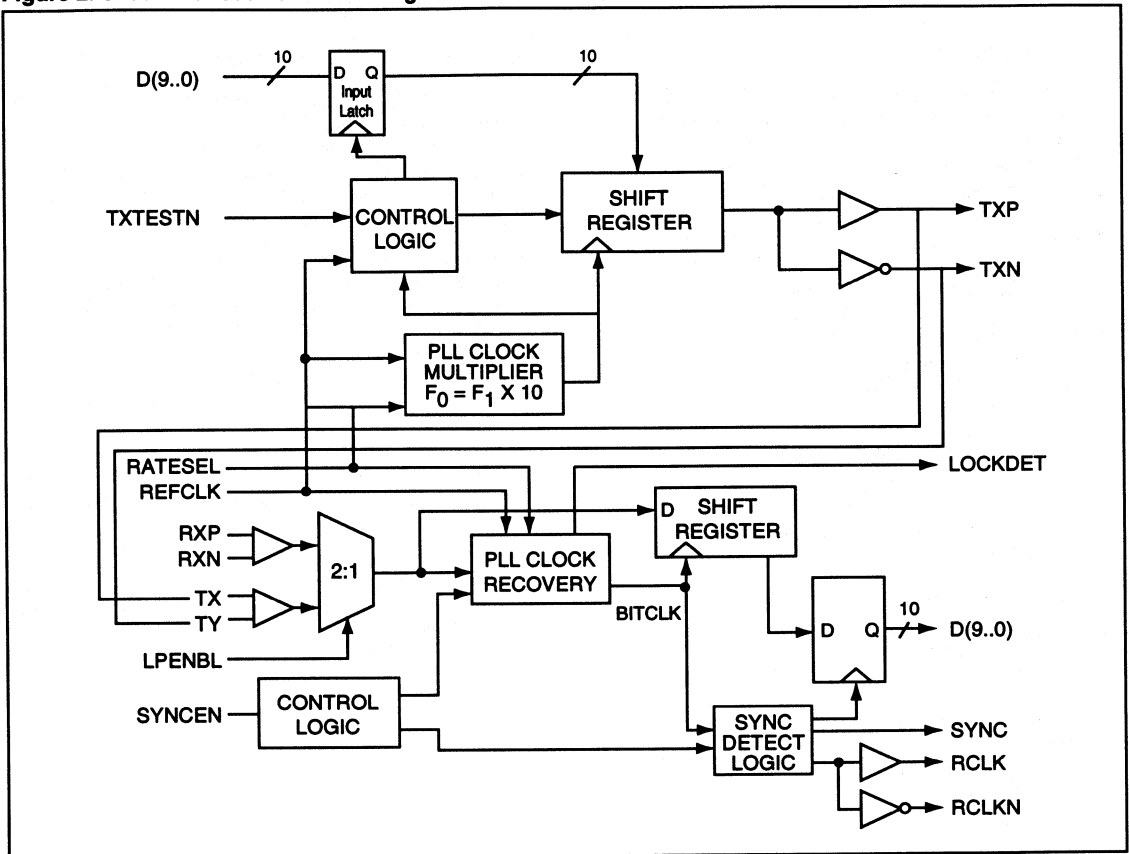


Figure 2. S2052 Transceiver Block Diagram



Contact AMCC for Product Availability.

This product is not released
and the specifications herein
are subject to change.

FEATURES

- Compliant with ANSI X3T11 Fibre Channel FC-1 layer functionality
- Supports Fibre Channel data transmission rates of 1062.5, 531.25, and 265.625 Mbit/s
- Full duplex operation
- Low-power technology
- 16-bit system interface, 20-bit physical layer interface
- Connects directly to AMCC's S2042/S2043 and S2044/S2045 serializer/deserializer devices
- 120 PQFP package

APPLICATIONS

- High-speed data communications
- Supercomputer
- Mainframe
- Workstation
- Adapter cards
- Frame buffer
- Switches
- Data broadcast environments

GENERAL DESCRIPTION

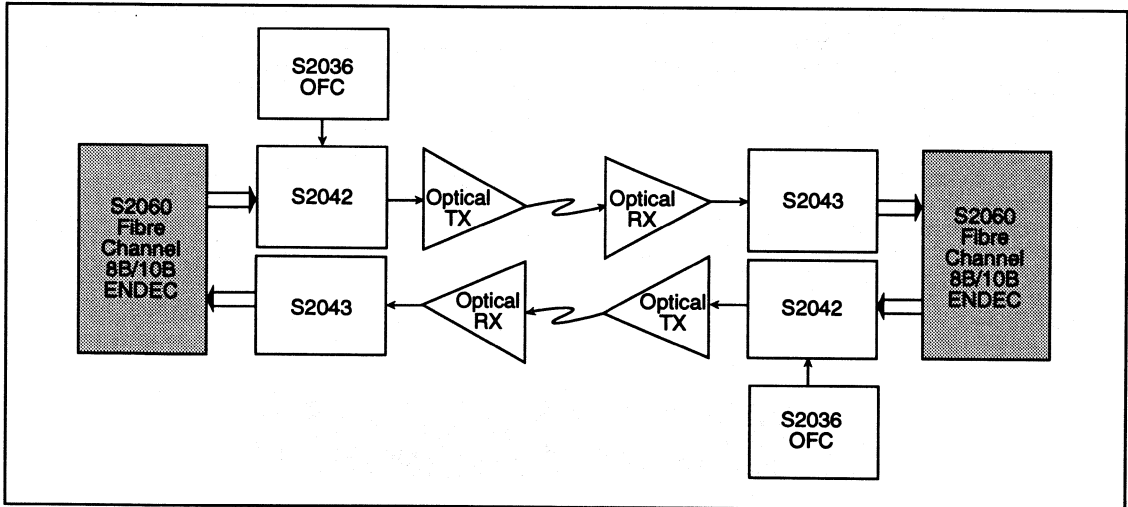
The S2060 is a physical layer Fibre Channel compatible 8B10B Encoder/Decoder conforming to the requirements of the ANSI X3T11 FC-PH standard. The S2060 implements the 8B/10B encoding and decoding functions of the transmission protocol (FC-1) layer of the Fibre Channel standard. The chip is designed to connect directly to AMCC's S2042/43 and S2044/45 serializer/deserializer chipset.

The S2060 supports full duplex operation with simultaneous encoding and decoding. The encoder takes in 16 bit NRZ data from the system interface and outputs 20 bit 8B/10B coded data to the physical layer serializer interface. The decoder takes in 20 bit 8B/10B coded data from the physical layer deserializer interface and puts out 16 bit NRZ data to the system interface.

The S2060 will operate at the 53.125 Mbyte/sec rate required for 1062.5 Mbit/sec full speed Fibre Channel operation. The part will also support the lower data rates of 26.5625 Mbytes/sec and 13.28125 Mbytes/sec.

Figure 1 shows a typical configuration incorporating the S2060 to implement a Fibre Channel Link.

Figure 1. Typical S2060 Link Configuration



FIBRE CHANNEL OVERVIEW

Fibre Channel is a high-performance serial link supporting its own as well as higher-level protocols associated with networking standards such as the High-Performance Parallel Interface (HIPPI), Intelligent Peripheral Interface (IPI), Small Computer System Interface (SCSI), and others. Fibre Channel is capable of replacing the HIPPI, IPI, and SCSI physical interfaces with a protocol-efficient alternative that provides performance improvements in both distance and speed. Fibre Channel standards are organized in layers, as seen in Figure 2.

The Fibre Channel is optimized for movement of large blocks of data such as those used in file transfers between processors (supercomputer, mainframe, etc.), storage systems (disk and tape), communications, and output-only devices such as laser printers and frame buffers.

Basics of the Fibre Channel specification are covered in the following sections. For details on Fibre Channel transmission and signaling protocol, refer to the ANSI X3T11 Fibre Channel standard document.

ENDEC Overview

The Fibre Channel transmission protocol includes serial encoding and decoding rules, special characters, and error control. It uses the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into a 10-bit transmission character (see Figure 3). Information received is recovered 10 bits at a time and those transmission characters used for data ("D"-type) are decoded into one of the correct 256 8-bit combinations.

Refer to the Fibre Channel standard for the complete listing of valid data characters. Some of the remaining transmission characters ("K"-type) are used for functions associated with control signals related to protocol management. Table 1 specifies the valid special characters. Codes detected at the receiver that are not D- or K-type are flagged as errors.

The characters defined by this transmission code ensure that short run lengths and enough transitions are present in the serial bit stream to make clock recovery possible at the receiver. The encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of data.

Figure 2. Fibre Channel Organization

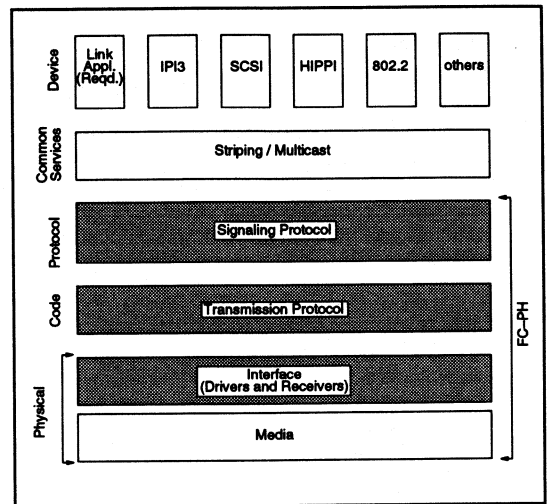
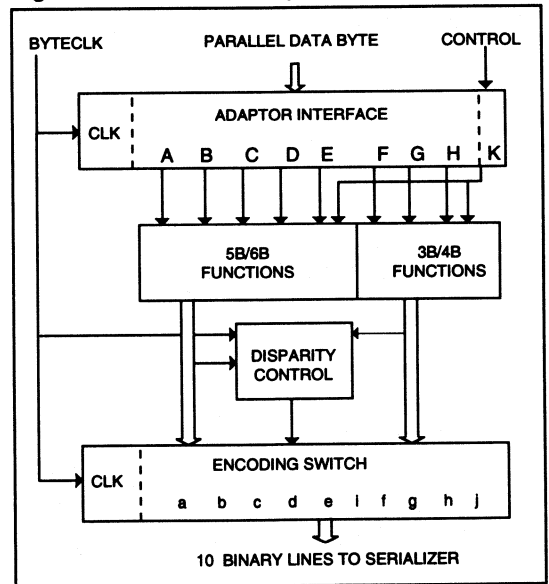


Figure 3. 8B/10B Encoding



Contact AMCC for Product Availability.

CONTENTS

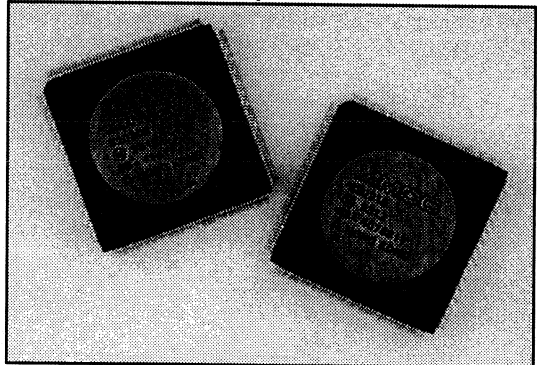
HIPPI PRODUCTS

S2020/S2021—HIPPI Source/Destination Interface Circuits.....	5-3
HIPPI Application Note	5-25

FEATURES

- Functionally compliant with the ANSI HIPPI standard
- 32-Bit data channel
- Equivalent single channel rate of 800 Mbits/sec
- Host-side interface single-ended TTL designed for use with external FIFO
- Channel-side interface differential ECL 10K
- Four rank data and control signal synchronization
- Byte parity checking
- Length/Longitudinal Redundancy Checkword (LLRC) generation and checking
- Automatic division of data into HIPPI bursts
- 16-Bit READY counter for flow control
- Maximum latency through both ICs
Connection: 600ns, Data: 400ns
- Diagnostic modes for self test
- Standard +5V, 0V(gnd), and -5.2V power requirements
- 225-pin ceramic PGA package
- 208-pin Thermally Enhanced Plastic (TEP)

S2020/S2021 HIPPI Chipset

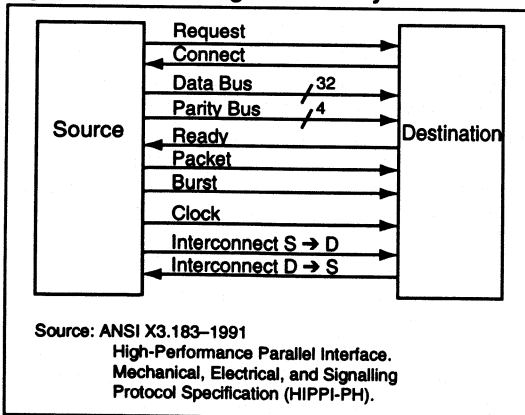


GENERAL DESCRIPTION

The S2020 and the S2021 are Source and Destination interface circuits, respectively, for the High-Performance Parallel Interface (HIPPI) standard. These circuits are designed to completely meet the signalling protocol of the proposed ANSI HIPPI specification: current document number X3.183-1991. They include both LLRC generation and checking as well as byte parity checking. The S2021 also incorporates a sophisticated four rank synchronization scheme to ensure that the incoming data and control signals are coupled to the local clock. Data flow control is provided by a 16-bit ready counter in both the Source and the Destination circuits. HIPPI data BURST partitioning is also provided in the Source circuit.

Architected and designed by Network Systems Corporation, the S2020 and S2021 utilize AMCC's 1.5-micron BiCMOS technology. AMCC's BiCMOS technology is especially optimized for high performance mixed mode ECL/TTL applications such as the HIPPI Source and Destination interfaces. AMCC pioneered ECL/TTL mixed mode BiCMOS capability and continues to be the leading U.S. supplier of BiCMOS VLSI circuits.

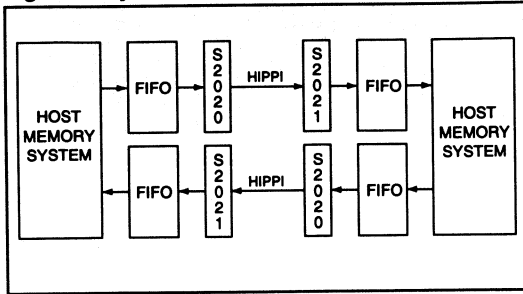
Figure 1. Interface Signal Summary



HIPPI OVERVIEW

The individual HIPPI channel is a simplex interface, meaning that data moves in one direction from the HIPPI Source (S2020) to the HIPPI Destination (S2021). Thus a fully bidirectional interface requires the use of two HIPPI channels as indicated in the System Block Diagram.

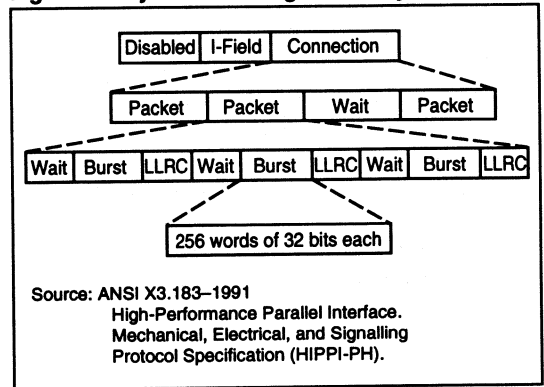
Figure 2. System Block Diagram



The transfer of data from the Source to the Destination depends on the physical connection of the two endpoints and the exchange of requesting, acknowledging, and data delimiting signals. The Source and Destination circuits both observe the state of the INTERCONNECT signals to verify a physically intact channel. If both Source and Destination are interconnected, the Source may initiate a data transfer by asserting the REQUEST signal. At the same time the Source places a 32 bit word also known as the I-Field on the data lines together with the appropriate Byte parity. The Upper Level Protocols (ULPs) controlling the Source and Destination may use this information for routing. The Destination responds to the REQUEST by asserting the CONNECT signal either for a short period while leaving the READY signal inactive to actively reject the REQUEST, or by asserting CONNECT and then asserting the READY signal to accept the REQUEST and indicate the availability of an input data buffer. The Destination can also accept the REQUEST by asserting CONNECT for a longer period without sending a READY, thus indicating a temporary delay in the availability of an input data buffer. The Source may remove the I-Field data after detecting the CONNECT signal.

Once the connection is established, data transfer can proceed according to the Physical Framing Hierarchy (see Figure 3). The basic data block is the Burst consisting of from 1 to 256 words of 32 data bits and 4 bits of odd byte parity. Each Burst is delimited by the assertion and deassertion of the BURST signal by the data Source. Every burst is followed immediately by Length/Longitudinal Redundancy Checkword (LLRC) which is the even parity for each bit for the entire length of the Burst together with the modulo 256 count of the number of words in the Burst. The count is included in the parity calculation for the least significant 8 bits of the LLRC word. For the normal full burst of 256 words, the count is all zeros (256 base 2 truncated to 8 bits).

Figure 3. Physical Framing Hierarchy



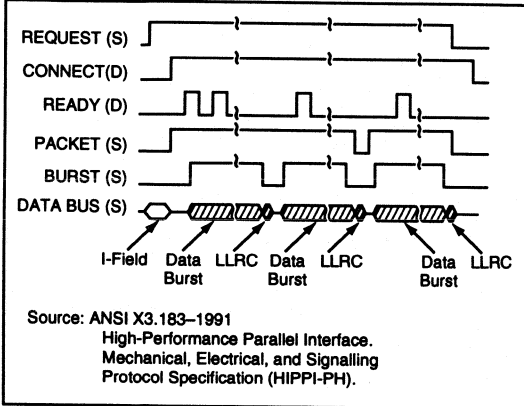
One or more Bursts are grouped as a Packet delimited by the assertion and deassertion of the PACKET signal by the Source. Wait periods are placed between Bursts and between Packets to allow synchronization adjustments between the Source and Destination circuits. A connection may contain one or more Packets. The details of the data transfer handshake are shown in Figure 4.

S2020 AND S2021 DESCRIPTION

The S2020 Source and the S2021 Destination circuits generate all of the required control and handshaking signals described above in the correct timing relationships, as well as providing Burst and Packet control, READY to BURST coordination, and LLRC generation and checking.

HIPPI FUNCTIONAL DESCRIPTION

Figure 4. Typical HIPPI-PH Waveforms



The Host systems are the actual originator and the ultimate destination of the data sent over the HIPPI channel. The purpose of the S2020 and S2021 is to decouple the Host hardware and software from the timing and formatting details of the interface. Each circuit can be considered as having a "Host-side" and a "HIPPI-side." The Host-side of the Source circuit accepts data from the Host FIFO and passes it to the HIPPI-side. The HIPPI-side controls the forward signals (REQUEST, PACKET, BURST and CLOCK) and receives the reverse signals (CONNECT and READY) of the HIPPI channel. The HIPPI-side of the Destination circuit receives the forward signals and controls the reverse signals of the HIPPI channel. The Host-side of the Destination delivers the received data to the Host FIFO.

The Host-side of both circuits can be thought of as consisting of four sections:

- Connect Control (for connecting/disconnecting to/from the HIPPI channel)
- Data/FIFO Control (for moving data to/from the Host logic)
- Data + Parity (for presenting data to/from the Host logic)
- Status/Control (for general control of the circuit and to obtain status from the circuit)

The purpose of these circuits is to reduce the complexity of the circuitry required to mate a Host memory system to the HIPPI channel. The Host-side is primarily single-ended TTL while the HIPPI-side is primarily differential ECL. Beside meeting the signalling protocol requirements of the HIPPI standard, the circuits provide a reduction of the signal lines to the host interface.

The circuits provide diagnostic modes for testing the devices themselves plus the circuitry that interfaces to the device. In the self-test modes, the INTERCONNECT signal can be deasserted. This effectively "unplugs" the device undergoing self-test from the HIPPI channel making it unavailable for connection and thus unable to generate spurious data or control information while in the diagnostic mode.

S2020 HIPPI SOURCE DEVICE

This device meets the signalling protocol requirements for a HIPPI-Source; i.e., it controls the forward signals and receives and acts on the reverse signals.

The Host-side consists of 45 single-ended TTL inputs used for data, control and the 50 MHz clock as well as 9 single-ended TTL outputs used for control of the external FIFO and to obtain device status.

The HIPPI-side consists of 40 differential ECL outputs (forward signals), 2 differential ECL inputs (reverse signals), 1 single-ended TTL output (Source-to-Destination INTERCONNECT signal) and 1 single-ended ECL input (Destination-to-Source INTERCONNECT signal).

ELECTRICAL REQUIREMENTS

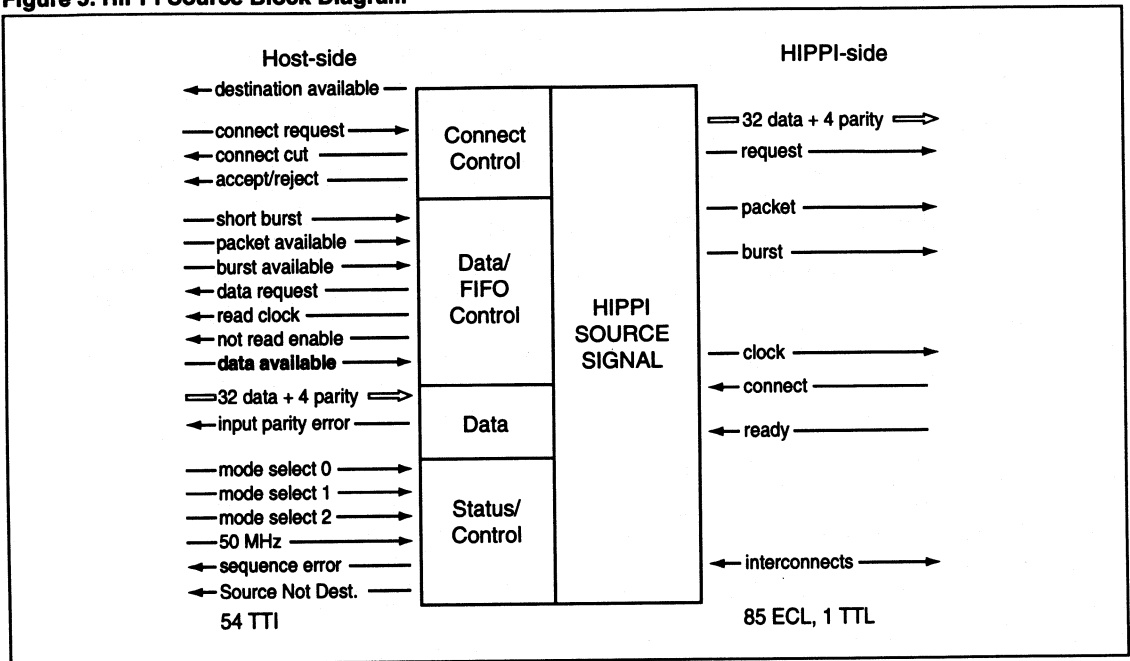
The differential ECL outputs require eighty 330 Ohm 2% resistors, one per pin. The differential ECL inputs require two 110 Ohm 2% resistors, one per input pair.

The two INTERCONNECT signals require external transmit and receive networks to reliably implement the signal swing required by the HIPPI Specification. For the Source-to-Destination INTERCONNECT (output signal), the required network is shown in Figure 10.

It should be noted that this network is only required if switching control of the INTERCONNECT signal by the Source device is desired. The network may be omitted and a simple pull-down of the Source-to-Destination INTERCONNECT via a 220 Ohm resistor to Vee may be used as indicated in the ANSI standard. For the Destination-to-Source INTERCONNECT (input signal), the required network is shown in Figure 11.

The network is strongly recommended for use on the received INTERCONNECT signal to avoid risk of saturation when operated with a switchable INTERCONNECT Destination device such as the S2021. It is also recommended for use in the non-switched passive pull-down applications to avoid damage to the ECL input due to transients caused by mechanical connection/disconnection cycles of the allowed cabling while Source and Destination are under power.

Figure 5. HIPPI Source Block Diagram



CONNECTION LATENCY

The Connection latency through the Source device consists of two parts: 1) The delay from the rising edge of the TTL input CONNECT_REQUEST to the assertion of the REQUEST signal in parallel with the placement of the I-Field data on the Host data bus and its availability on the HIPPI channel data bus (4 clock cycles), and 2) the delay from the detection of the CONNECT signal for the 17th clock cycle and the assertion of the TTL outputs CONNECT_OUT and ACCEPT/REJECT to the Host (3 to 4 clock cycles). The total connection latency in the Source device ranges from 7 to 8 clock cycles. This does not include cable delay or Destination processing.

DATA LATENCY

The data latency through the Source device is defined as the delay from the rising edge of the BURST_AVAILABLE signal and the assertion of the BURST signal on the HIPPI channel. The data latency is 4 clock cycles. This does not include cable delay or Destination processing.

SOURCE CONNECT CONTROL

Connection control is provided by four control signals and two error flags on the Host-side of the Source device. Using the signals the Host can "request" a connection to a Destination and monitor the results (whether the Destination has accepted or rejected the connection request). Timeout mechanisms, if required, must be provided by the Host hardware or software.

DESTINATION_AVAILABLE (output) [DSTAV]*

A high level on this signal indicates an active Destination-to-Source INTERCONNECT signal. Low indicates inactive INTERCONNECT.

CONNECT_REQUEST (input) [CNREQ]

This signal when high directs the Source device to read the I-Field from the Host System (see HIPPI Data Control, page). When a valid I-Field is read, it is placed on the HIPPI channel and the HIPPI REQUEST signal is asserted. The information in the I-Field can be used by intermediate HIPPI nodes (nodes that are not end-points) to control the routing of the associated connection. The Host would then monitor the CONNECT_OUT and ACCEPT/REJECT signals to determine the state of the connection.

*Bracketed signal name refers to pin matrix on pages 20–23 (all signals).

CONNECT_OUT (output) [CNOUT]

This signal, along with the CONNECT_REQUEST and ACCEPT/REJECT signals defines the current state of the HIPPI connection. A high level indicates active acceptance or rejection of a requested connection.

ACCEPT/REJECT (output) [ACREJ]

This signal along with the CONNECT_REQUEST and CONNECT_OUT signals defines the current state of the HIPPI connection. A high level indicates active acceptance of a requested connection.

SEQUENCE_ERROR (output) [SQERR]

This signal when high indicates the presence of either a Source error state (PACKET_AVAILABLE dropped before the first word of Burst transmitted or CONNECT_REQUEST is reasserted before Destination has deasserted CONNECT) or Destination error state (CONNECT is detected before REQUEST has been asserted).

SOURCE_NOT_DESTINATION (output) [SRNDS]

This signal is used to distinguish between a Source error (logic 1 state) and a Destination error (logic 0 state).

DATA/FIFO CONTROL

This interface provides control to the Source Host system, of the flow and organization of the data to be transferred over the HIPPI channel. It is intended for this interface to attach to an external synchronous FIFO, which is in turn attached to the Source Host memory system. Recommended FIFO's capable of buffering 4 or more Bursts are:

IDT P/N 72225LB20 1K x 18 bits

IDT P/N 72235LB20 2K x 18 bits

IDT P/N 72245LB20 4K x 18 bits

The signals of this interface can be divided into three groups; Source FLOW control, Source FIFO control, and HIPPI data control.

SOURCE FLOW CONTROL

After a HIPPI connection is established, data transfer from the Source Host to the Destination Host is enabled by the presence of data from the Source Host and the current ability of the Destination Host to accept data. The presence of data from the Source Host is indicated to the Source device on the Source FLOW control lines. The ability of the Destination Host to receive data is determined by the Source device's FLOW control circuit.

The Source device FLOW control circuit consists of a set of 16-bit counters that automatically maintain the number of READYs received from the HIPPI Destination and the number of BURSTs sent to the HIPPI Destination. In the Source device, these counters are reset when the HIPPI channel is disconnected, and then enabled when the HIPPI channel is reconnected. When the BURST counter and the READY counter are equal, data transfer will be disabled and both counters are enabled. When the BURST counter and the READY counter are not equal and their difference is not 65535 $[(2 \times 16) - 1]$, data transfer will be enabled and both counters are enabled. When the difference between the BURST counter and the READY counter is 65535, data transfer is enabled and the READY counter is disabled. Disabling the READY counter results in a limit of 65535 pending READYs for the HIPPI connection.

The Source FLOW control signals are:

BURST_AVAILABLE (input) [BSTAV]

This signal when held high enables the initiation of a data transfer from the FIFO, through the Source device, to the HIPPI channel. When held low this signal prevents the initiation of a data transfer. A transition from high to low after a data transfer has been initiated has no effect on that transfer (i.e., the current Burst will terminate normally).

DATA_AVAILABLE (input) [DATAV]

This signal when high indicates the current presence of at least one more word from the Source Host FIFO and enables the synchronous load of the data bus into the Source device. When low this signal disables the data loading. It is intended that this signal be driven by the Not Empty flag of the FIFO. In this configuration any interruption of the data flow due to the FIFO not being refilled by the host will result in a Short Burst with normal LLRC and Burst termination. This signal must be reasserted and the BURST_AVAILABLE signal reasserted to start a subsequent Burst.

DATA_REQUEST (output) [DTREQ]

This signal indicates the current ability of the HIPPI Destination to accept data. When high the signal indicates a current connection on the HIPPI channel and the inequality of the BURST and READY counters in the Source device FLOW control circuit. When low, (and during a HIPPI channel connection) the signal indicates the equality of the BURST and READY counters in the Source device FLOW control circuit, i.e., the Source has sent one BURST to the HIPPI Destination for each READY received from that Destination.

SOURCE FIFO CONTROL

When a data transfer is enabled, the Source device will initiate read operations of the Source Host FIFO by activating the Source FIFO control lines.

The Source FIFO control signals are:

READ_CLOCK (output) [RDCLK]

This signal is a continuous 25 MHz clock synchronous with the internal clocks of the Source device and the HIPPI channel differential ECL CLOCK signal. The signal is intended to be used together with NREN to control the read function of the FIFO and as a reference for timing critical Host-side control signals such as SHORT_BURST and PACKET_AVAILABLE. This signal is intended to drive the 'read clock' input of the Source Host FIFO system.

NOT_READ_ENABLE (output) [NRDEN]

This signal when held low, is used to strobe data from the FIFO to the Source device. This signal is used as a gate of the 25 MHz TTL RDCLK for the synchronous operation of the FIFO. This signal is intended to drive the 'read enable' input of the Source Host FIFO system.

HIPPI DATA CONTROL

PACKET_AVAILABLE (input) [PKTAV]

This signal when high causes the Source device to start a Packet if Bursts are available. When brought low, this signal will end the Packet.

SHORT_BURST (input) [SHBST]

This signal when high while PACKET_AVAILABLE is low indicates presence of I-Field data at the Source device input data lines. During a Burst, a high level indicates that the current data word is the last word of a Short Burst.

Each read operation performed by the Source device reads a Data/Parity word, and an associated HIPPI data control field consisting of the PACKET_AVAILABLE and SHORT_BURST signals. Because the HIPPI data control field is to be read in parallel with the associated DATA and PARITY, these (two) bits can be written by the Source Host into the Source Host FIFO as the DATA and PARITY are transferred into it. As the Source device reads each word from the Source Host FIFO, the HIPPI data control field specifies what type of HIPPI data operation is to be performed.

The three basic types of HIPPI data operations are: I-Field, HIPPI PACKET control, and HIPPI BURST control. The HIPPI data control signals defining these data types are shown on the HIPPI Data Control Table.

HIPPI DATA CONTROL SIGNALS		
	SHORT_BURST (input) [SHBST]	PACKET_AVAILABLE (input) [PKTAV]
IDLE. No PACKET or BURST onto HIPPI channel	0	0
Assert PACKET onto the HIPPI channel*	0	1
Associated data is a HIPPI I-Field	1	0
Associated data is last word of HIPPI Burst	1	1

When the Source Host initiates a HIPPI CONNECT_REQUEST, the Source device performs read operations until a HIPPI I-Field is read. The Source device recognizes a HIPPI I-Field by decoding the HIPPI data control lines. Once a HIPPI I-Field is presented to the Source device, the REQUEST line will be asserted on the HIPPI channel and the I-Field will be put on the HIPPI channel data bus. By identifying the HIPPI I-Field in this way, the Source Host can effectively queue several connections in the FIFO and also enter primary and secondary I-Fields for single connections to support alternate paths for connect reject retries.

When data transfers are enabled, as described above, the HIPPI data control field specifies what partitioning operations are to be performed by the Source device on the associated data word. The main partitioning operations are: begin HIPPI Packet, maintain HIPPI Packet, terminate HIPPI Packet, auto-burst termination, and explicit (short) burst termination.

The three HIPPI Packet functions control the organization of data into HIPPI Packets. The auto-burst termination allows the Source device to automatically delimit the unbounded data from the Source Host FIFO into HIPPI Bursts of 256 (max) words each. The Short Burst termination allows the Source Host to specify BURST boundaries for HIPPI data bursts. In addition to the explicit Short Burst and auto-burst terminations, the Source device will terminate a HIPPI Burst if the HIPPI Packet is terminated at a non-256 word boundary or if the Source Host supply of data expires on a non-256 word boundary.

*The Source device will not assert Packet onto the HIPPI channel until the first data Burst of the Packet is sent. This prevents the possible generation of a zero-Burst Packet (illegal) onto the HIPPI channel.

The sequence of control signals and data presented to the HIPPI channel by the Source device meet all the requirements of the HIPPI specification. There is no need for the Source Host to insert wait intervals (dummy words) in the FIFO stream to provide the required wait intervals between PACKET and BURST (the FIFO can be 100% utilized for HIPPI I-Field and data). The Source device will automatically generate LLRC and append it to the end of each terminated HIPPI Burst regardless of how the Burst was terminated. It is the responsibility of the Source Host to prevent multiple Short Bursts in one Packet.

The Source device automatically formats the transferred data into packets and bursts with LLRC. The Source device counts the number of data words received from the FIFO and uses this number as the "seed" for the LLRC calculation.

DATA AND PARITY

The Source Host presents the HIPPI I-Field and Data to the HIPPI Source device on the TTL DATA AND PARITY interface.

32_DATA_+_4_PARITY (inputs) [DATxx,PARxx]

These lines are used for the I-Field during the connection sequence and for data during Burst transfers.

INPUT_PARITY_ERROR (output) [INPRR]

Parity is checked just before the data leaves the Source device (i.e. at the inputs to the differential drivers of the HIPPI channel). Parity errors are reported on a word by word basis. Upon detecting a parity error for a given word, this signal is set high for the duration of the next word's clock cycle (approximately 40 nsec).

Note: All parity errors are indicated but no recovery action is taken by the Source device. If there is a parity error detected, then the data and the bad parity are passed through the Source.

CHIP STATUS/CONTROL

Overall control of the HIPPI Source device is provided to the Source Host by the STATUS/CONTROL interface, which allows the Source Host to control the device clock frequency and phase (if necessary), and to select the operating mode of the Source device.

50_MHZ (input) [50MHZ]

This 50 MHz TTL clock is divided by 2 to generate a 50% duty cycle 25 MHz clock for all internal timing functions of the Source device and as the generated and transmitted HIPPI channel CLOCK signal. This

input also latches the MODE_SELECT inputs on its rising edge. The phase of the resulting 25 MHz clock is controllable by the phase of the asserted RESET mode described below.

SOURCE DEVICE OPERATING MODES

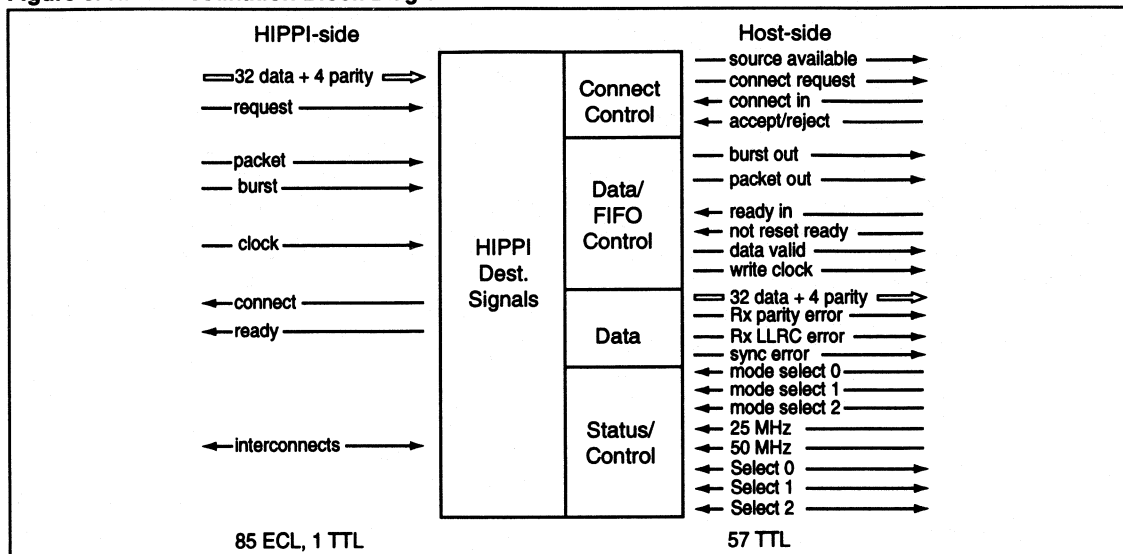
The Source device has several operating modes, which require external selection by the Source Host. Also provided is a 'board test' mode that may be used by the Source Host as a part of a system diagnostic routine. The Source Host selects the operating mode with the two lines, MODE_SELECT_0 and MODE_SELECT_1 [MSELx]. For numerical reference, MODE_SELECT_1 is the most significant bit. MODE_SELECT_2 should be held at a TTL logic zero (ground) for in-board operation of the Source device.*

Mode 0 (00 on mode select bus) is device reset. In the reset mode, all internal registers are initialized, and all device outputs are forced inactive including the HIPPI Source-to-Destination INTERCONNECT [SDIC] output. The ability to control the phase of the 25MHz clock (and the READ_CLOCK output) which is generated by dividing the 50_MHZ input by 2 is also provided by this mode.

Mode 1 (01) is the board test mode. In this mode, the Source device provides a means to verify connection and operation of the interface between the Source Host and the Source device completely independent of the HIPPI channel. In this mode, the Source-to-Destination INTERCONNECT [SDIC] signal is forced inactive. When the Source Host initiates a Connection Request by asserting CONNECT_REQUEST, the Source device advances the FIFO to the first I-Field, reads the I-Field, and then simulates a Connect Accept on the HIPPI channel, asserting the CONNECT_OUT and ACCEPT/ REJECT signals to the Source Host. The Source Host will then provide 'test' data bursts to the Source device through the FIFO, as it would for a functional data transfer, and the Source device will pass the 'test' data through the LLRC and parity check functions. The data will also appear at the HIPPI-side data outputs, but since the Source device is not in the functional or wait Modes the Source-to-Destination INTERCONNECT signal is inactive. The only difference to the Source Host between a functional transfer and a 'test' transfer is that the first data word of each 'test' burst must be the expected LLRC of the previous 'test' burst. By providing the expected LLRC, the Source device can compare its generated LLRC with the Host's expected LLRC,

*The active state of MODE_SELECT_2 is used for manufacturing test of the Source device.

Figure 6. HIPPI Destination Block Diagram



and thus verify the integrity of the DATA, PARITY, and DATA/FIFO CONTROL busses. This test routine continues until the Mode is changed or until a miscompare is detected between the Host's expected LLRC and the device's generated LLRC. When a miscompare is detected, the simulated connection is terminated and CONNECT_OUT is deactivated. Mode 0 (reset) clears the board test mode.

Mode 2 (10) is the WAIT mode. This mode provides an interlock device between the Source Host and the HIPPI channel that requires the Source Host to acknowledge an inactive Destination-to-Source INTERCONNECT [DSIC] before an active DSIC signal is processed. In this mode the Source-to-Destination INTERCONNECT [SDIC] is active. The requirement upon the Source Host is that if DESTINATION_AVAILABLE is inactive and the Source Host is waiting for it to become active, the Source device must be put into Mode 2. Once DESTINATION_AVAILABLE is active, the Source device must be put into Mode 3 to initiate further operations.

Mode 3 (11) is the operational mode. This mode activates the Source-to-Destination INTERCONNECT signal and enables the functional operation of all the Source device interfaces.

NOTE: The only time DESTINATION_AVAILABLE will go from inactive to active is if Destination-to-Source INTERCONNECT is active while the Source device is brought from Mode 0 (reset) to Mode 3 (operational) or if the Source device is in Mode 2 (wait).

S2021 HIPPI DESTINATION DEVICE

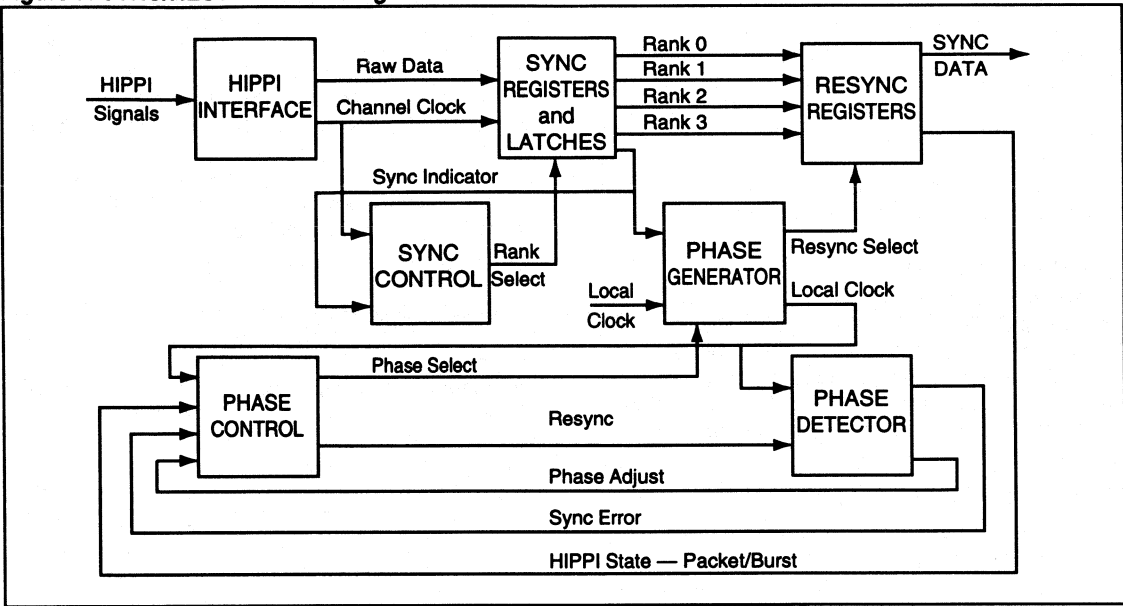
This chip meets the signalling protocol requirements for a HIPPI-Destination, i.e., it controls the reverse signals and receives the forward signals.

The HIPPI-side consists of 40 differential ECL inputs (forward going signals), 2 differential ECL outputs (reverse signals), 1 single-ended ECL input (Source-to-Destination INTERCONNECT signal), and 1 single-ended TTL output (Destination-to-Source INTERCONNECT signal).

The Host side consists of 45 single-ended TTL outputs used for data, FIFO control and status, 9 single-ended TTL inputs used for chip control, a 25 MHz clock and a 50 MHz clock and 3 TTL Bidirectional I/O.

In addition to the signal translation and control handshake functions, the Destination device provides a four stage "elastic store" for the buffering of the data, parity, and control information received from the HIPPI channel. This internal FIFO (not to be confused with the external multi-Burst size FIFO) together with a digital phase locked loop structure allow the HIPPI channel clocked information to be synchronized to the local (Host-side) 25 MHz clock. The use of the combined 50 MHz and 25 MHz clocks allow tracking of the synchronizer through more than 1200 degrees of phase "slip" or error between received HIPPI clock and the local clock. In a normally operating HIPPI channel, the accumulated

Figure 7. SYNC/RESYNC Block Diagram



phase error is re-zeroed during the inter-burst/packet Wait period by resynchronization. Since multiple nodes could be in the channel between the originating Source and the final Destination, the inter-burst Wait states may have been “consumed” before the data is received. The large phase tolerance of the sync/resynch circuitry (shown in Figure 7) in the Destination device allows 48 consecutive Bursts with missing Wait states to be received before synchronization is lost. A maximum rate transfer through a chain of 30 nodes, all with worst-case jitter, operating at progressively worse frequency margins, and all requiring a ‘dropped’ cycle at the same time would be required between the originating Source and the final Destination to produce 48 consecutive missing Wait cycles.

ELECTRICAL REQUIREMENTS

The resistors needed to complete the electrical requirements of the HIPPI-Destination interface are four 330 Ohm 2% resistors, one per pin of differential ECL outputs, and forty 110 Ohm 2% resistors, one per pair of differential ECL inputs

The two INTERCONNECT signals require external transmit and receive networks to reliably implement the signal swing required by the ANSI standard. For the Destination-to-Source INTERCONNECT (output signal), the required network is shown in Figure 10.

This network is only required if switching control of the INTERCONNECT signal by the Destination device is desired. The network may be omitted and a simple pull-down of the Destination-to-Source INTERCONNECT via a 220 Ohm resistor to Vee may be used as indicated in the ANSI standard. For the Source-to-Destination INTERCONNECT (input signal), the required network is shown in Figure 11.

CONNECTION LATENCY

The connection latency through the Destination device consists of two parts:

- 1) the time between the arrival of the REQUEST signal on the HIPPI channel from the Source device, to the presentation by the Destination device of the l-field to the TTL data lines and assertion of CONNECT_REQUEST ranges from 4 to 5 clock cycles;
- 2) the time between assertion of CONNECT_IN signal by the host (to accept the connection request), to the assertion of the CONNECT signal by the Destination device on the HIPPI channel is 2 clock cycles.

The Destination device connection latency therefore ranges from 6 to 7 clock cycles. This does not include local host connection processing (the time it takes the host to decide whether or not to accept a particular connection request).

DATA LATENCY

The data latency through the Destination device is defined as the time between detection of the BURST signal by the Destination device from the HIPPI, to the presentation of the data to the FIFO on the TTL data lines and the assertion of the DATA_VALID line. The data latency ranges from 2 to 6 clock cycles. There is no response by the Destination device on the HIPPI channel to data reception.

CONNECT CONTROL

Connection control is provided via the four signals in the "Connect Control" area on the Host-side of the Destination device. With this interface, the Host can monitor when a Connect Request or Disconnect Request comes in from the HIPPI Source, and then initiate the appropriate action in response to the request.

SOURCE_AVAILABLE (output) [SRCAV]

High indicates an active Source-to-Destination INTERCONNECT signal while the Destination device is in the on-line mode. Low indicates an inactive Source-to-Destination INTERCONNECT signal or the Destination device commanded to the off-line or disabled mode.

CONNECT_REQUEST (output) [CONRQ]

This signal indicates the state of the REQUEST signal on the HIPPI channel. High indicates a Connect Request function from the HIPPI channel, resulting from an asserted REQUEST signal while the Destination device is in a functional operating mode with Connect Requests enabled. Low indicates either a false REQUEST signal on the HIPPI channel, a disabled Connect Request at this device, or that the Destination device is in a non-functional mode.

CONNECT_IN (input) [CONIN]

This signal controls the Connect Request and Response functions of the Destination device on the HIPPI channel. A low on this input will hold the CONNECT signal on the HIPPI channel inactive, and will enable the REQUEST signal from the HIPPI channel to control the CONNECT_REQUEST output of this Destination device.

During a Connect Request, asserting this input initiates one of two responses to the Request; Accept or Reject the Request. The desired response is selected with the ACCEPT_REJECT input, described next. If a Connect Request is accepted,

holding this input high will maintain an asserted CONNECT signal on the HIPPI channel, while dropping this input will deassert the CONNECT signal (Disconnect Function). If a Connect Request is rejected, holding this input high will maintain a deasserted CONNECT signal on the HIPPI channel (after the four cycle reject sequence) and disable further Connect Requests, while dropping this input will also maintain a deasserted CONNECT signal but will enable further Connect Requests.

ACCEPT_REJECT (input) [ACCRJ]

This input specifies the response to generate when CONNECT_IN is asserted during a Connect Request. A high on this input when CONNECT_IN is asserted will generate an Accept response, i.e., the CONNECT signal on the HIPPI channel will be asserted and will remain asserted until a Disconnect Function is initiated (CONNECT_IN is deasserted). A low on this input when CONNECT_IN is asserted will generate a Reject response, i.e., the CONNECT signal on the HIPPI channel will be asserted for four cycles then fall and remain deasserted until the response for the next Connect Request is initiated. The ACCEPT_REJECT signal needs to be valid only for the first cycle of the asserted CONNECT_IN input.

Note: The host can have the Destination device automatically respond to connection requests by tying the CONNECT_REQUEST output to the CONNECT_IN input. In this case, the ACCEPT/REJECT signal would be used as an "available/busy" signal. While ACCEPT/REJECT was held low all connection requests would be rejected.

DATA/FIFO CONTROL

This interface provides control to the Destination Host system over the flow of data transfers on the HIPPI channel, and provides control of data transfer from the Destination device into the Destination Host system. It is intended for this interface to attach to an external synchronous FIFO or DMA mechanism which, in turn, attaches to the Destination Host memory system. Recommended FIFO's capable of buffering 4 or more full Bursts are:

IDT P/N 72225LB20 1K x 18 bits
IDT P/N 72235LB20 2K x 18 bits
IDT P/N 72245LB20 4K x 18 bits

The signals of this interface can be divided into three groups: Destination FLOW control, Destination FIFO control, and HIPPI data control.

DESTINATION FLOW CONTROL

After a HIPPI connection is established, data transfer from the Source Host to the Destination Host is enabled by the presence of data from the Source Host and the current ability of the Destination Host to accept that data. Although this function is performed at the HIPPI Source, the HIPPI Destination signals its current buffer capacity to the Source via the READY signal on the HIPPI channel.

The Destination FLOW control circuit consists of a set of modulo 64K counters that maintains the current Buffer capacity, the number of READYs sent to the HIPPI Source, and the number of Bursts received from the HIPPI Source. At initialization (Destination device reset) all of these counters are reset. When the Source-to-Destination INTERCONNECT [SDIC] signal is true and the Destination device is in a functional mode, the Destination Host may initialize the Buffer counter to the number of HIPPI Bursts that it can accept. When a Connect Request is accepted, the Destination device will automatically generate legal READY pulses and increment the READY counter for each pulse until the READY counter equals the Buffer counter. If the Buffer counter was not initialized before the Connect Request, then no READY pulses will be generated. If the Buffer counter is incremented after the Connection is made, then READY pulses will automatically be generated until the READY and Buffer counters are equal. The Buffer counter will be disabled when it equals Burst count -1, thereby putting a limit of 64K on the number of pending READY pulses.

If the Burst counter is not equal to the READY counter as a data Burst is received, then the Burst counter is incremented and the data is automatically transferred to the Destination Host. If the Burst counter is equal to the READY counter as a data Burst is received, then the data is not transferred to the Destination Host and an Overflow error is reported.

When the HIPPI connection is terminated, one of two operations may be performed by the Destination Host: the Destination FLOW control counters may be reset (and initialized), or the current buffer capacity may be automatically saved for the next HIPPI connection. To reset and initialize, the Destination Host must maintain a set of buffer counters, or empty the buffers before the next connection. To automatically save the current buffer capacity, the Destination device will initialize the READY counter to the Burst counter: at the end of a HIPPI connection, the number of remaining available buffers at the Destination Host is the difference between the Burst counter and the Buffer counter. Therefore, initializing the READY counter to the

Burst counter contents will result in that same difference between the READY and Buffer counters. When a subsequent HIPPI connection is accepted, the Destination FLOW control circuit will automatically send the correct number (equal to the number of currently available buffers in the Destination Host) of READY pulses.

The Destination FLOW control signals are:

READY_IN (input) [RDYIN]

This input controls the Destination FLOW control circuit's Buffer and READY counters. A rising edge on this input will increment the Buffer counter and, if a Connect Request has been accepted, generate a READY pulse on the HIPPI channel as well as increment the READY counter by one. This input can be driven by a free-running 12.5 MHz clock for maximum throughput on the HIPPI channel (representing infinite Host buffer capacity), or it can be controlled by the Host memory system. If controlled by the Destination Host system, after initialization with one edge for each available buffer, the Host may generate one rising edge on this input after it processes and releases each used 256 word buffer.

NOT_RESET_READY (input) [NRRDY]

This signal is an active low TTL input that erases the stored count of available Host system buffers by resetting the Buffer, Ready and Burst counters to their initial states.

DESTINATION FIFO CONTROL

When a data Burst is received over the HIPPI channel, the Destination FIFO Control provides the signals necessary to transfer the received data from the Destination device to the Destination Host FIFO system. In addition to transferring received data Bursts, the Destination device will also transfer the HIPPI I-Field, and the channel and device status words as specified in the FIFO Control Signal Table. To provide flexibility at this interface, the Destination device identifies each type of information presented to the Destination Host, so that each implementation may customize its use of the information.

The Destination FIFO Control signals are:

WRITE_CLOCK (output) [WRCLK]

This signal is a buffered 25 MHz TTL clock synchronized to the internal local clock. It is intended for use with the VALID signal to transfer data to the write port of the FIFO and to serve as the timing reference for critical input and output control signals of the Host-side of the Destination device.

SELECT_0, 1, 2 (bi-directional) [SELBx]

These signals are used in conjunction with the MODE_SELECT inputs during manufacturing testing to confirm the function of the internal counters and state machines. In the functional mode [Mode value 5 (101)] the value of the SELECT (SELECT_2 is MSB) bus indicates the type of data available on the DOUT_0,31 signals. Select value 0 (000) indicates burst data on the outputs. Select value 1 (001) indicates I-Field data on the outputs. Select value 2 (010) indicates the LLRC word, and Select value 3 (011) indicates internal status data during inter-BURST wait states. When there is no connection on the HIPPI channel, the select value will sequence and repeat 5,6,7 (101, 110, 111) until connection is requested. Select value 4 is reserved to indicate sequence error status for advanced link diagnostics. For most applications these latter values can be ignored.

DATA_VALID (output) [DTVAL]

This signal is intended to be used together with the SELECT_0,1,2 outputs to gate the clocking of received data into the FIFO or register set selected by the select lines. All received data will be presented to the data outputs of the Destination device and will be accompanied by a DATA_VALID signal.

HIPPI DATA CONTROL

The data and control signals, received on the HIPPI channel, are resynchronized to the 25_MHz local clock, converted to TTL, and then presented to the data and control interface used by the host.

The HIPPI data control signals are:

BURST_OUT (output) [BROUT]

This signal indicates the state of the BURST line on the HIPPI channel. High indicates an active BURST and is presented with each word of the received burst. Low indicates an inactive BURST and is presented when there is no received data.

PACKET_OUT (output) [PKOUT]

This signal indicates the state of the PACKET line on the HIPPI channel. High indicates an active PACKET and is presented as long as PACKET is active on the HIPPI channel. Low indicates an inactive PACKET and is presented as long as PACKET is inactive on the HIPPI channel.

Note: The BURST_OUT and PACKET_OUT signals are provided to delimit the data into the FIFO the same way it is delimited on the HIPPI channel. These signals may not be needed by the Host.

FIFO Control Signal Table

SELB(2:0)	HOST data	DATA_VALID	Comment
000	HIPPI Burst	1 (high)	for duration of data received Burst
001	HIPPI I-Field	1 (high)	for duration of HIPPI Connect Request
010	HIPPI LLRC	1 (high)	one word, after last word of each Burst
011	gen. op. status	1 (high)	one word, beginning each Packet received on channel (accomp. start of PACKET_OUT)
		1 (high)	one word, end of each Burst, after LLRC*
		1 (high)	one word, end of each Packet (accompanies deactivation of PACKET_OUT)*
011	gen. op. status	0 (low)	multiple words, while connection is estab. across channel, but channel has no data
100	SEQUENCE ERROR	1 (high)	one word, when a HIPPI sequence error is detected, or when an illegal signal sequence disrupts the devices's state machines
101	idle/disab. status	1 (high)	one word, in sequence with FLOW status words (below), continuously while channel is disconnected
110	FLOW status word 1	1 (high)	one word, in sequence with FLOW status word 2 and idle/disab. status, continuously while channel is disconnected
111	FLOW status word 2	1 (high)	one word, in sequence with FLOW status word 1 and idle/disab. status, continuously while channel is disconnected

*Only one general operational status word (Select code 011) will be presented if the BURST and PACKET terminations coincide, i.e., BURST deasserted, followed by PACKET deasserted.

DATA AND PARITY

32_DATA_+_4_PARITY (outputs) [DToxx, PAROx]

These signals reflect what was received on the data and parity lines of the HIPPI channel, resynchronized to local clock. During a connection request (CONNECT_REQUEST going high and remaining high) the I-field is presented on these signals. The LLRC is also presented to this interface after the last word of each burst.

Note: All parity errors are indicated but no recovery action is taken by the Destination device. If there is a parity error detected, then the data and bad parity are passed through the Destination device.

RX_PARITY_ERROR (output) [RPERR]

High indicates a detected parity error on a data word received over the HIPPI channel. This is valid for each word received; however, there may be a time skew between this indication and the presentation of data. See Figure 9 for details. The bad parity bit(s) is presented with its associated data word.

During a connection request the data lines contain the I-field. RX_PARITY_ERROR indication presented to the host logic when a connection has not been established tells the host that an I-field parity error has been detected. The RX_PARITY_ERROR signal is valid for every clock that I-field is presented. Bad parity on the I-field will result in the chip raising RX_PARITY_ERROR until one of the following things happen:

- The I-field changes (stabilizes) so that the parity is good
- The host logic accepts or rejects the connection request based on I-field content and the state of RX_PARITY_ERROR
- The HIPPI channel source drops REQUEST

RX_LLRC_ERROR (output) [RLLER]

This signal high means that an LLRC error was detected on a received burst. This signal is presented to the host along with the LLRC following the last word of the burst.

The Destination device counts the number of data words it receives from the HIPPI channel and uses this number as the "seed" for the LLRC it computes and checks against the received LLRC word.

SYNC_ERROR (output) [SYNER]

This signal high indicates the loss of synchronization with the HIPPI channel (overrun or underrun).

CHIP STATUS/CONTROL

MODE_SELECT_0, 1, and 2 (inputs) [MSELx]

There are several operating modes in which the Destination device can be placed. Operational and diagnostic modes are controlled by the data placed on the MODE_SELECT bus. MODE_SELECT_2 is the MSB and MODE_SELECT_0 is the LSB of this bus. Mode value 0 (000) is to be used as the master reset mode for all internal counters and state machines and should be used for power-up initialization. Mode value 4 (100) is the board test or diagnostic mode. In this mode an internal "walking zero" pattern generator will exercise all Host-side TTL outputs and the parity error circuitry. The SELECT_0, 1, 2 outputs will count through all eight states allowing exercise of any external I-Field or status registers driven by the Destination device. Mode value 5 (101) is the normal functional mode for the Destination device.

25_MHz (INPUT) [25MHZ]

This signal provides the Destination device with a 25MHz TTL clock (also called local clock) and is used to resynchronize the HIPPI channel clock and data.

50_MHz (INPUT) [50MHZ]

This signal provides the Destination device with a 50 MHz TTL clock and is used for internal state machine control, and for resynchronization. The phase requirements between this clock and 25_MHz are shown in Figure 9.

ABSOLUTE MAXIMUM RATINGS

ECL Supply Voltage V_{EE} ($V_{CC} = 0$)	-8.0VDC
ECL Input Voltage ($V_{CC} = 0$)	GND to VEE
ECL Output Source Current (continuous)	-50mA DC
TTL Supply Voltage V_{CC} ($V_{EE} = 0$)	7.0V
TTL Input Voltage ($V_{EE} = 0$)	5.5V
Operating Temperature	0°C to 70°C Ambient
Operating Junction Temperature T_J	+130°C
Storage Temperature	-65° to +150°C

ECL 10K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -5.2V1$

	T _{ambient}			UNIT
	0°C	25°C	75°C	
V_{OHmax}	-770	-730	-650	mV
V_{IHmax}	-720	-680	-600	mV
V_{OHmin}	-1000	-980	-920	mV
V_{IHmin}	-1145	-1105	-1045	mV
V_{ILmax}	-1490	-1475	-1450	mV
V_{OLmax}	-1625	-1620	-1585	mV
V_{OLmin}	-1980	-1980	-1980	mV
V_{ILmin}	-2000	-2000	-2000	mV
I_{inHmax}	-0	30	30	μA
I_{inLmax}	-5	-5	-5	μA

RECOMMENDED OPERATING CONDITIONS

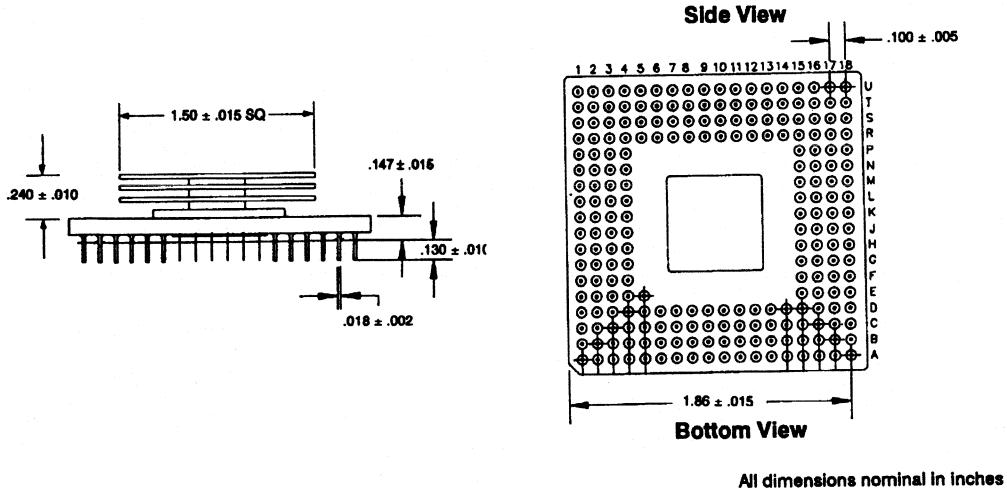
PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE})	-4.94	-5.2	-5.46	V
TTL Supply Voltage (V_{CC})	4.75	5.0	5.25	V
TTL Output Current Low (I_{OL})			20	mA
Ambient Temperature	0		70	°C
Junction Temperature			<130	°C
S2020 — I_{CC}		65	91	mA
— I_{EE}		421	589	mA
— P_{OEF}		1530		mW
S2021 — I_{CC}		125	174	mA
— I_{EE}		307	429	mA
— P_{OEF}		90		mW

TTL INPUT/OUTPUT DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL 0°/+70°C			UNIT
			MIN	TYP ²	MAX	
V_{IH}^3	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			V
V_{IL}^3	Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8	V
V_{IK}	Input clamp diode voltage	$V_{CC} = \text{Min}$, $I_{IN} = -18\text{mA}$		-8	-1.2	V
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min}$, $I_{OH} = -1\text{mA}$	2.7	3.4		V
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min}$			0.5	V
		$I_{OL} = 8\text{mA}$			0.5	V
		$I_{OI} = 20\text{mA}$				V
I_{IH}	Input HIGH current	$V_{CC} = \text{Max}$, $V_{IN} = 2.7\text{V}$			110	μA
I_I	Input HIGH current at Max.	$V_{CC} = \text{Max}$, $V_{IN} = 5.25\text{V}$			1	mA
I_{IL}	Input LOW current	$V_{CC} = \text{Max}$, $V_{IN} = 0.5\text{V}$			110	μA
I_{OS}	Output short circuit current	$V_{CC} = \text{Max}$, $V_{IN} = 0.5\text{V}$	-25		-100	mA

1. Data measured with $V_{EE} = -5.2 \pm .1\text{V}$ assuming a +50°C rise between ambient (t_a) and junction temperature (T_J) for 0°C, +25°C, and +70°C. Specification will vary based upon T_J . These conditions will be met with an ambient 70°C airflow of 200 LFM.
2. Typical limits are at 25°C, $V_{CC} = 5.0\text{V}$.
3. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

225 PGA



5

208 Thermally Enhanced Plastic (TEP)

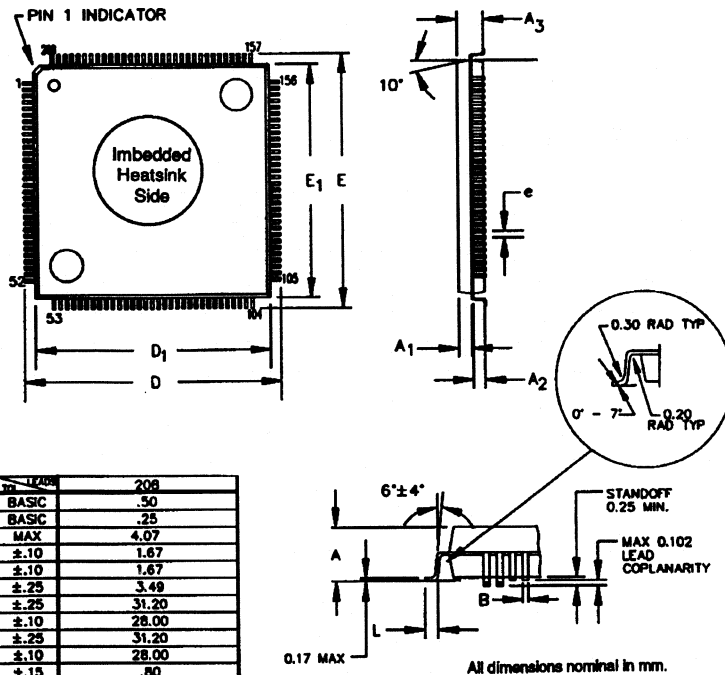
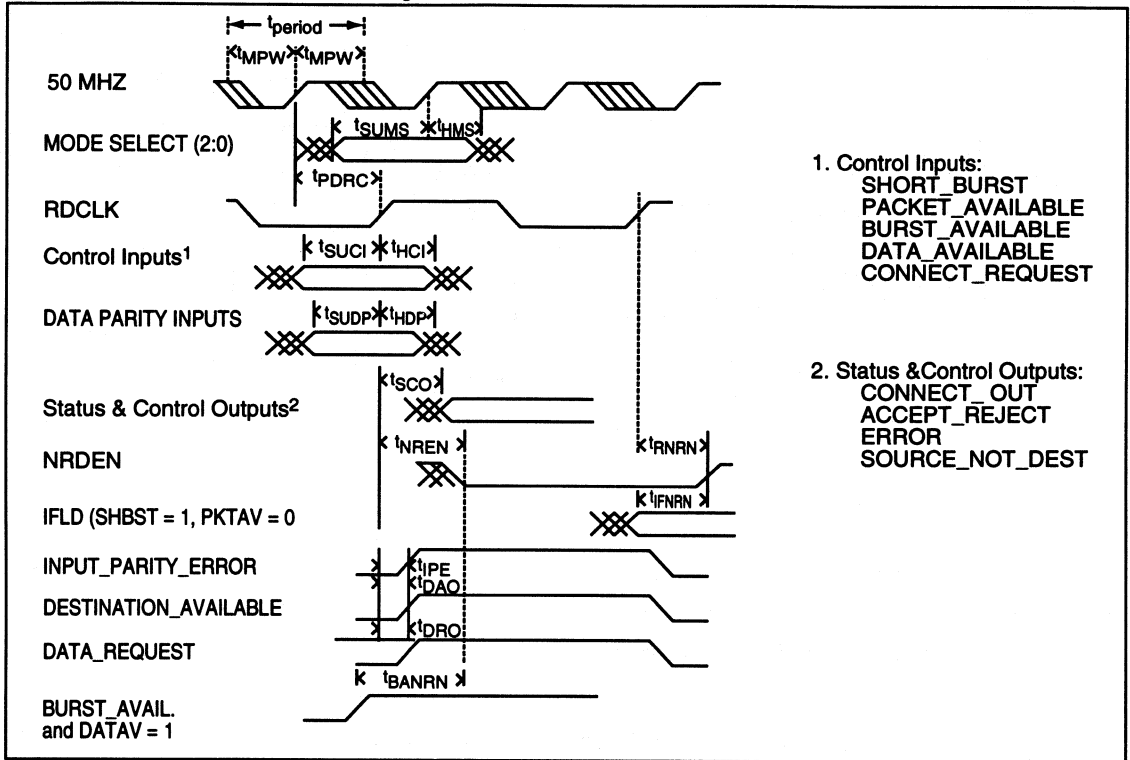


Figure 8. S2020 Source Device Timing

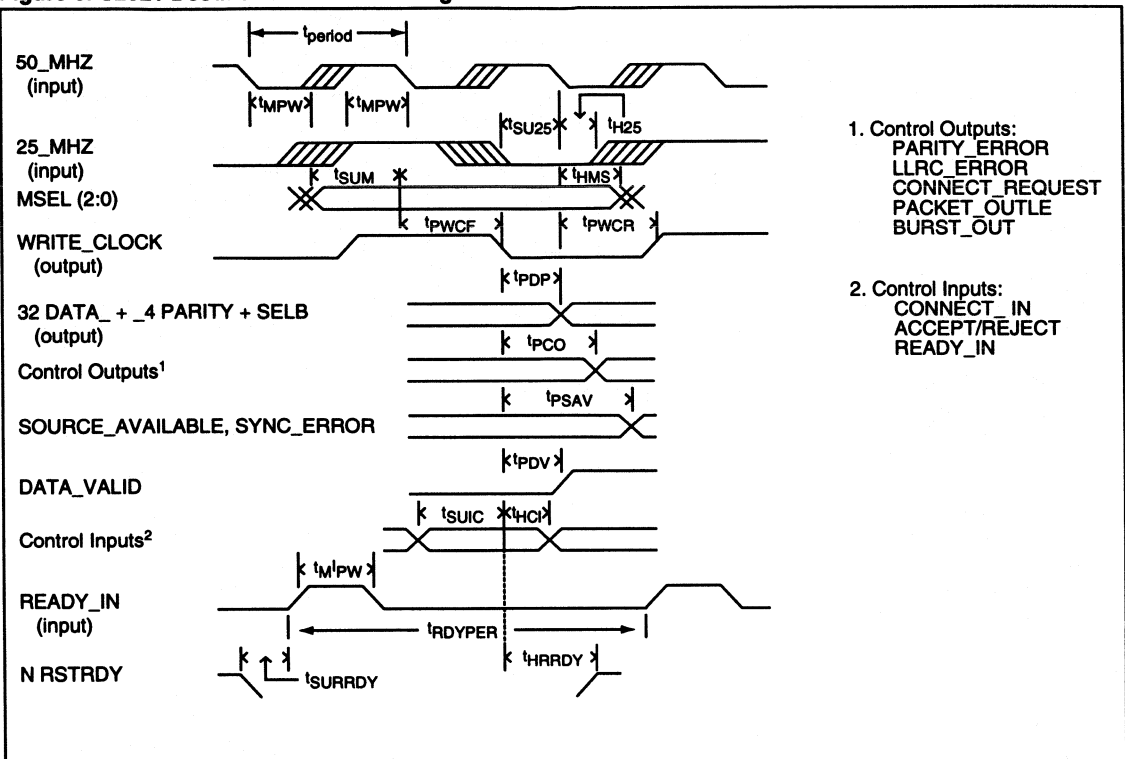


S2020 Source Timing Table

	Min nsec	Typ nsec	Max nsec	Notes
t_{PERIOD} ³	—	20	—	
t_{MPW} ³	5.55	—	—	
t_{SUMS}	7	—	—	Relative to 50MHz INPUT
t_{HMS}	0	—	—	
t_{PDRC}	5	11	17	For Reference Only
t_{SUCI}	21	—	—	Relative to RDCLK Rising Edge
t_{HCI}	0	—	—	
t_{SUDP}	14	—	—	
t_{HDP}	0	—	—	
t_{SCO}	—	—	17	
t_{NREN} ⁴	—	—	14	
t_{IPE} ⁴	—	—	10	
t_{DAO} ⁴	—	—	17	
t_{DRO} ⁴	—	—	10	
t_{IFNRN} ⁴	—	—	19	
t_{NRRN} ⁴	—	—	19	
t_{BANRN} ⁴	—	—	17	

3. Guaranteed but not tested

Figure 9. S2021 Destination Device Timing



5

S2021 Destination Timing Table

	Min nsec	Typ nsec	Max nsec	Notes
tPERIOD ³	—	20	—	
tMPW ³	5.55	—	—	
tPWCF ⁴	5	—	14	Relative to 50MHz Falling Edge
tPWCR ⁴	5	—	15	
tSU25	2	—	—	
tH25	25	—	—	
tPDP ⁴	—	—	13	
tPCO ⁴	—	—	13	Relative to WRCLK Falling Edge
tPSAV ⁴	—	—	18	
tPDV ⁴	—	—	16	
tSUCI	9	—	—	
tHCI	0	—	—	
tRDYPER ³	40	—	—	
tSURRDY ³	8	—	—	Relative to WRCLK falling edge or RDYIN rising edge
tHRRDY ³	8	—	—	
tSUM	5	—	—	
tHMS	5	—	—	

3. Guaranteed but not tested

4. Assumes 5pf load for ECL and 15pf for TTL

SOURCE

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
	NC	ND27	D28	D29	ND31	NP0	P1	P2	P3	TPWR	TGND	PAR02	DAT31	DAT28	DAT25	DAT22	DAT19	NC	U
	D26	NC	ND28	ND29	D30	EGND	P0	NP2	NP3	TSTO*	PAR03	PAR00	DAT30	DAT27	DAT24	DAT21	NC	DAT18	T
	ND25	D25	NC	D27	EGND	ND30	D31	NP1	-5.2V	-5.2V	PAR01	DAT29	DAT26	DAT23	DAT20	NC	DAT16	DAT15	S
	ND24	D24	ND26	+5V	+5V	GND	GND	GND	-5.2V	-5.2V	GND	GND	GND	+5V	+5V	DAT17	DAT13	DAT12	R
	D22	ND23	EGND	+5V	BOTTOM VIEW										+5V	DAT14	DAT10	DAT09	P
	ND21	D21	D23	GND											GND	DAT11	DTREQ	NRDEN	N
	EGND	D20	ND22	GND											GND	DAT00	RDCLK	DSTAV	M
	ND19	D19	ND20	GND											GND	INPRR	CNOUT	ACREJ	L
	ND18	D18	-5.2V	-5.2V											-5.2V	-5.2V	SDIC	SRNDS	K
	D17	ND17	-5.2V	-5.2V											-5.2V	-5.2V	TGND	SQERR	J
	D16	ND16	ND15	GND											GND	DAT04	DAT06	DAT07	H
	D15	D14	D13	GND											GND	DAT00	DAT03	DAT05	G
	ND14	GTR0*	ND12	GND											GND	SHBST	DAT01	DAT02	F
	ND13	D12	EGND	+5V											NC	+5V	MSEL2	BSTAV	PKTAV
	D11	ND11	D09	+5V	+5V	GND	GND	GND	-5.2V	-5.2V	GND	GND	GND	+5V	+5V	EGND	CNREQ	DATAV	D
	D10	ND10	NC	ND08	EGND	D05	ND04	ND02	-5.2V	-5.2V	NPKT	THDI*	VBB	RDY	CON	NC	MSEL0	MSEL1	C
	ND09	NC	D07	D06	ND05	D03	D02	D01	D00	NCLK	REQ	PKT	BRST	EGND	EGND	EGND	NC	50MHZ	B
	NC	D06	ND07	ND06	D04	ND03	EGND	ND01	ND00	CLK	NREQ	EGND	NBRST	THDO*	DSIC	NRDY	NCON	NC	A

*Indicates signal used for component testing—make no connection

HIPPI INTERCONNECT PAIR

DSIC = Destination to Source Interconnect
 SDIC = Source to Destination Interconnect

EGND = TGND = GND = 0V

TPWR = +5V

HIPPI DESTINATION PIN GRID

S2020/S2021

DESTINATION

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
NC	CON	NREQ	BRST	CLK	NP3	P2	P1	P0	ACCRJ	D31	D30	ND28	D27	ND25	ND24	D23	NC	U
NRDY	NC	THDI*	NBRST	PKT	CONIN	P3	NP1	NP0	ND31	ND30	D29	D28	ND26	D25	D24	NC	NRRDY	T
TGND	THDO*	NC	NCON	REQ	NPKT	NCLK	NP2	-5.2V	-5.2V	ND29	ND27	D26	RDYIN	ND23	NC	D22	ND21	S
SELB1	SELB0	RDY	+5V	+5V	GND	GND	GND	-5.2V	-5.2V	GND	GND	GND	+5V	+5V	ND22	ND20	D20	R
25MHZ	50MHZ	TPWR	+5V	BOTTOM VIEW										+5V	D21	D19	ND18	P
DT000	DSIC	SELB2	GND											GND	ND19	MSEL2	ND17	N
DT003	DT001	DTVAL	GND											GND	D18	D17	D16	M
DT005	DT004	DT002	GND											GND	ND16	ND15	D15	L
DT007	DT006	-5.2V	-5.2V											-5.2V	-5.2V	ND14	D14	K
DT008	DT009	-5.2V	-5.2V											-5.2V	-5.2V	ND13	MSEL1	J
TPWR	TGND	DT011	GND											GND	ND11	ND12	D13	H
DT010	DT012	DT015	GND											GND	ND09	D11	D12	G
DT013	DT014	DT018	GND											GND	D08	D10	ND10	F
DT016	DT017	DT021	+5V											NC	+5V	MSEL0	ND08	D09
DT019	DT020	DT022	+5V	+5V	GND	GND	GND	-5.2V	-5.2V	GND	GND	GND	+5V	+5V	ND05	D07	ND07	D
TPWR	TGND	NC	DT025	DT028	TGND	PAR00	RPERR	-5.2V	-5.2V	SSO1*	D00	ND01	SDIC	D04	NC	D06	ND06	C
DT023	NC	DT026	DT029	DT030	PAR01	PAR03	SRCV	CONRQ	PKOUT	TGND	SSO2*	VBB	D01	ND02	ND03	NC	D05	B
NC	DT024	DT027	TPWR	DT031	PAR02	SYNER	BROUT	WRCLK	RLER	TPWR	SSO0*	SSEN*	ND00	D02	D03	ND04	NC	A

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*Indicates signal used for component testing only
 — Connect SSEN to GROUND (0V)
 — Make no connection to other pins mark with asterisk (*)

HIPPI INTERCONNECT PAIR
 DSIC = Destination to Source Interconnect
 SDIC = Source to Destination Interconnect

EGND = TGND = GND = 0V
 TPWR = +5V

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	GND	53	GND	105	GND	157	GND
2	GND	54	+5V	106	GND	158	+5V
3	DAT18	55	NCON	107	ND09	159	ND27
4	DAT17	56	CON	108	D09	160	D27
5	DAT16	57	EGND	109	ND10	161	ND28
6	DAT15	58	NRDY	110	D10	162	D28
7	DAT14	59	RDY	111	EGND	163	EGND
8	DAT13	60	EGND	112	ND11	164	ND29
9	DAT12	61	DSIC	113	D11	165	D29
10	DAT11	62	VBB	114	ND12	166	ND30
11	DAT10	63	EGND	115	D12	167	D30
12	DAT09	64	-5.2V	116	ND13	168	ND31
13	DAT08	65	-5.2V	117	D13	169	D31
14	-5.2V	66	GND	118	-5.2V	170	-5.2V
15	-5.2V	67	GND	119	-5.2V	171	-5.2V
16	GND	68	BRST	120	GND	172	GND
17	GND	69	NBRST	121	GND	173	GND
18	DTREQ	70	PKT	122	ND14	174	NP0
19	NRDEN	71	NPKT	123	D14	175	P0
20	RDCLK	72	EGND	124	ND15	176	NP1
21	INPRR	73	REQ	125	D15	177	P1
22	DSTAV	74	NREQ	126	ND16	178	NP2
23	CNOUT	75	NCLK	127	D16	179	P2
24	ACREJ	76	CLK	128	ND17	180	NP3
25	SDIC	77	GND	129	D17	181	P3
26	SRNDS	78	GND	130	GND	182	GND
27	GND	79	+5V	131	GND	183	GND
28	GND	80	ND00	132	+5V	184	+5V
29	+5V	81	D00	133	ND18	185	TST0
30	SQERR	82	ND01	134	D18	186	TGND
31	DAT07	83	D01	135	ND19	187	PAR03
32	DAT06	84	GND	136	D19	188	PAR02
33	DAT05	85	ND02	137	EGND	189	PAR01
34	DAT04	86	D02	138	ND20	190	PAR00
35	DAT03	87	ND03	139	D20	191	DAT31
36	DAT02	88	D03	140	ND21	192	DAT30
37	DAT01	89	GND	141	D21	193	GND
38	-5.2V	90	GND	142	-5.2V	194	GND
39	-5.2V	91	-5.2V	143	-5.2V	195	-5.2V
40	GND	92	-5.2V	144	GND	196	-5.2V
41	GND	93	ND04	145	GND	197	DAT29
42	DAT00	94	D04	146	ND22	198	DAT28
43	PKTAV	95	ND05	147	D22	199	DAT27
44	BSTAV	96	D05	148	ND23	200	DAT26
45	SHBST	97	ND06	149	D23	201	DAT25
46	DATAV	98	D06	150	ND24	202	DAT24
47	CNREQ	99	EGND	151	D24	203	DAT23
48	MSEL2	100	ND07	152	ND25	204	DAT22
49	MSEL1	101	D07	153	D25	205	DAT21
50	MSEL0	102	ND08	154	ND26	206	DAT20
51	50MHZ	103	D08	155	D26	207	DAT19
52	GND	104	+5V	156	GND	208	+5V

EGND = TGND = GND = 0V;
TPWR = +5V

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	NRRDY	53	GND	105	GND	157	NCON
2	ND22	54	+5V	106	DTO23	158	NREQ
3	D22	55	ND04	107	DTO22	159	REQ
4	ND21	56	D04	108	DTO21	160	NBRST
5	D21	57	ND03	109	DTO20	161	BRST
6	ND20	58	D03	110	DTO19	162	NPKT
7	D20	59	SDIC	111	DTO18	163	PKT
8	ND19	60	ND02	112	DTO17	164	CLK
9	D19	61	D02	113	DTO16	165	NCLK
10	ND18	62	ND01	114	DTO15	166	-5.2V
11	D18	63	D01	115	-5.2V	167	-5.2V
12	-5.2V	64	ND00	116	-5.2V	168	GND
13	-5.2V	65	D00	117	GND	169	GND
14	GND	66	-5.2V	118	GND	170	CONIN
15	GND	67	-5.2V	119	DTO14	171	NP3
16	MSEL2	68	GND	120	DTO13	172	P3
17	ND17	69	GND	121	DTO12	173	NP2
18	D17	70	VBB	122	DTO11	174	P2
19	ND16	71	SSEN	123	DTO10	175	NP1
20	D16	72	SSO2	124	TGND	176	P1
21	ND15	73	SSO1	125	DTO09	177	NP0
22	D15	74	SSO0	126	DTO08	178	P0
23	ND14	75	PKOUT	127	GND	179	GND
24	D14	76	RLLER	128	GND	180	GND
25	GND	77	GND	129	+5V	181	+5V
26	GND	78	GND	130	DTO07	182	ACCRJ
27	+5V	79	+5V	131	DTO06	183	ND31
28	MSEL1	80	WRCLK	132	DTO05	184	D31
29	ND13	81	CONRQ	133	DTO04	185	ND30
30	D13	82	BROUT	134	DTO03	186	D30
31	ND12	83	SRCAV	135	DTO02	187	ND29
32	D12	84	SYNER	136	DTO01	188	D29
33	ND11	85	RPERR	137	DTO00	189	ND28
34	D11	86	PARO3	138	DSIC	190	D28
35	ND10	87	PARO2	139	-5.2V	191	GND
36	D10	88	PARO1	140	-5.2V	192	GND
37	-5.2V	89	GND	141	GND	193	-5.2V
38	-5.2V	90	GND	142	GND	194	-5.2V
39	GND	91	-5.2V	143	DTVAL	195	ND27
40	GND	92	-5.2V	144	25MHZ	196	D27
41	ND09	93	PARO0	145	50MHZ	197	ND26
42	D09	94	DTO31	146	SELB2	198	D26
43	ND08	95	DTO30	147	SELB1	199	ND25
44	D08	96	TGND	148	SELB0	200	D25
45	ND07	97	DTO29	149	TPWR	201	RDYIN
46	D07	98	DTO28	150	TGND	202	ND24
47	MSEL0	99	DTO27	151	RDY	203	D24
48	ND06	100	DTO26	152	NRDY	204	ND23
49	D06	101	DTO25	153	GND	205	D23
50	ND05	102	DTO24	154	GND	206	+5V
51	D05	103	+5V	155	+5V	207	GND
52	GND	104	GND	156	CON	208	GND

EGND = TGND = GND = 0V;
TPWR = +5V

Figure 10. Interconnect (output) Network

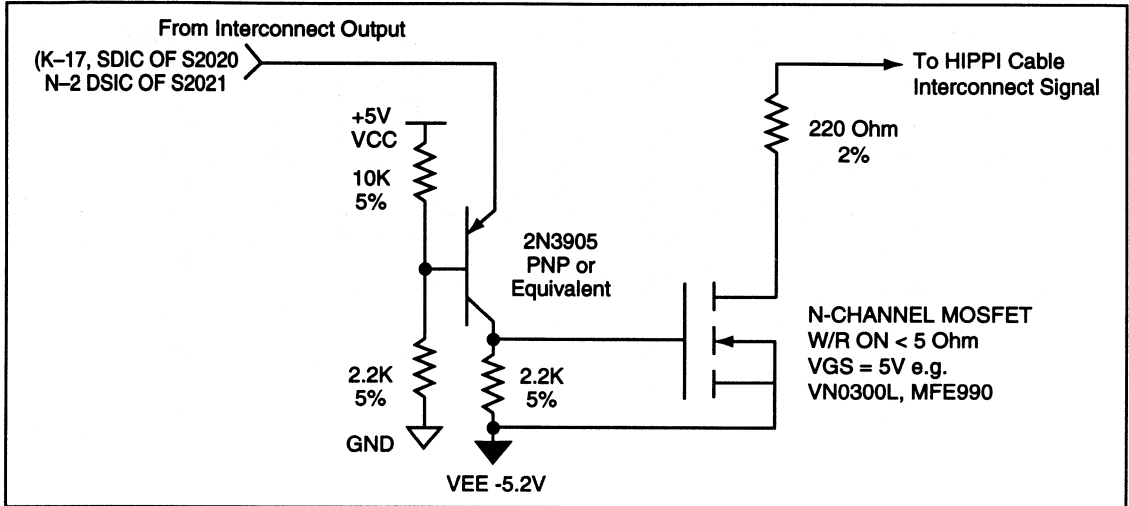
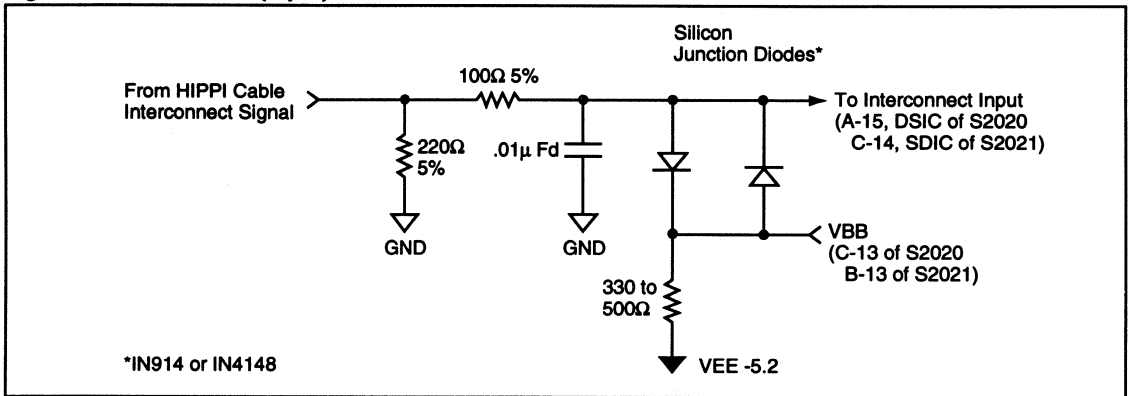


Figure 11. Interconnect (input) Network



ORDERING INFORMATION		
GRADE	FUNCTION	PACKAGE
S-Commercial	2020 — Hippi Source 2021 — Hippi Destination 2022 — Hippi Evaluation Kit (contains 2 source and 2 destination parts)	A = 225 PGA B = 208 TEP

X XXXX X

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1.0 S2020 HIPPI SOURCE CONNECT CONTROL

The S2020 Source Device meets the signalling protocol for the Hippi-Source as determined by ANSI X3.183-1991 HipPI-PH Mechanical Electrical and Signalling Protocol Specification. As the Source, the S2020 functions as the initiator and controller of all data transfers on the Hippi channel.

The RESET Command (Mode 0) initializes all internal state machines in the S2020 and clears all data and parity bit registers to zero. The only function that is not cleared or held at an initialized state is the clock control which generates the internal 25 MHz and the external RDCLK signal. The RESET Command provides phase control of the internal and external clocks.

If the RESET Command is placed on the MODE(2:0) inputs while the RDCLK output is in the logic high state, there will be no change in the continuous 25 MHz signal observed at the RDCLK output. If, however, the RESET Command is placed on the MODE(2:0) inputs while the RDCLK output is in the logic low state, the RDCLK output will go high after the next rising edge of the 50 MHz input, remain high for two cycles of the 50 MHz input and then produce a rising edge on the third 50 MHz falling edge applied to the S2020. From that point until the next application of the RESET Command the RDCLK (and the internal clocks) will be a continuous 25 MHz signal synchronized to the 50MHz input rising edge.

This "phase slip on low" function can be used to unambiguously set the phase relation between the 50 MHz input and the RDCLK output. Since most of the Host interface control inputs are required to be synchronous with the 25 Mhz RDCLK output, this phase slip control gives the user the capability of aligning the S2020's timing to the 50 MHz and 25 MHz used in the external Host circuitry.

It should be noted that while the RESET Command clears the Parity Error bit (INPRR output), the internal data and parity registers have also been cleared. This "zero data/zero parity" condition is a Parity Error with respect to the HIPPI odd byte parity convention. If a parity correct word is present at the inputs of the S2020 at the time the RESET state is exited, there will be a two clock period parity error bit on the INPRR output. If the attached FIFO has also been cleared during the RESET Command, the INPRR bit will remain high until three clocks after the first read cycle of the FIFO.

While there are some differences in FIFO or "FIFO equivalent" memory structures that have been successfully used with the S2020, the available or an-

nounced synchronous clocked FIFOs from IDT, Cypress and Sharp all share this feature. Even if the external data source memory had "correct" parity available at the inputs of the S2020, the two clock period parity error would be observed.

The first function that must be performed after the power-up initialization of the S2020 (RESET Mode 0) is to determine the status of the Destination to Source Interconnect [DSIC] signal. That signal, generated by the remote HIPPI Destination, is an input signal from the HIPPI Channel to the S2020 and must be in the logic low (active) state for any control or data transfer functions to be valid on the HIPPI Channel.

The filtered and inverted state of the DSIC input is available at the Destination Available [DSTAV] output. Since the S2020 has the capability of switching its own Source to Destination output signal to the inactive state during Reset and Board Test modes, the Device must be placed in the Wait for Destination mode (Mode 2) immediately after RESET to allow the filter to recognize either the static low (active) DSIC input or the high to low transition of the DSIC input.

If the S2020 is placed directly from the RESET Mode into the Operational Mode (Mode 3), the DSTAV output will not correctly respond to the DSIC input state, even if the DSIC input is already in the active low condition when the RESET to Operational mode change is made. The Wait for Destination mode avoids possible control ambiguities in systems where both Source and Destination have active control of their respective Interconnect signals.

With the S2020 in the Wait for Destination mode (Mode 2), the observation of an active high state on the DSTAV output indicates that the internal reset and initialization cycle of the entire HIPPI Channel (both Source and Destination) is complete. The S2020 may now be legally placed in the Operational mode, and the internal Connect State Machine of the S2020 will be placed in the {IDLE} state.

If there is any interruption of the DSIC input greater than the filter integration time (four clock cycles), the Connect State Machine will be forced to the {LOSTDEST} state. This will immediately stop any current data transfer, and cause the REQUEST, PACKET and BURST signals on the HIPPI Channel to go to the inactive state. The DSTAV signal will go low to indicate this condition to the Source Host System. The only recovery from this condition is the RESET and WAIT sequence described above. It is the responsibility of the Source Host System to exercise a reasonable "time-out" if the remote Destination does not generate a stable active low state on the DSIC signal.

Once the DSTAV signal is observed at an active high state and the Operational Mode (Mode 3) is commanded, the S2020 is ready to initiate a Connection Request sequence. The design of the S2020 is optimized to use the external synchronous FIFO as the source of the I-Field Word as well as the PKTAV and SHBST signals used to flag the I-Field Word. If the I-Field and/or the two control signals are not placed in the FIFO, care must be taken that their timing is controlled to meet the specification of the Data Sheet. Failure to honor that timing will cause erroneous and unpredictable operation of the FIFO with resultant data loss.

The S2020 acts as a continuously running, two register deep pipeline. In the HIPPI application, the only point at which a data word is held static for multiple clock cycles is the output register of the FIFO. The NREN output of the S2020 is applied to the Not Read Enable input of the FIFO to control this register.

It should be also noted that for the recommended FIFO and most equivalents, the operation of writing into the FIFO from the Host System does not directly write any data into the FIFO's output register. The data in the output register is indeterminate (it may be zero if the entire system including the FIFO was initialized, otherwise it is usually the last transmitted data word.)

Placing the I-Field and the two signals defining the I-Field in the FIFO eliminates any ambiguity as to the previous contents or state of the FIFO. If the FIFO has been filled with data, and the Not Empty output of the FIFO is connected to the DATAV input of the S2020, then a high signal on the CNREQ input and the high signal already at the DATAV input will cause an active low on the NREN output. The NREN signal will remain low for at least one cycle of the 25 MHz RDCLK until the 01 condition is observed on the PKTAV and SHBST inputs respectively.

The detection of the 01 condition will asynchronously raise the NREN signal to the inactive state, locking the current data word (assumed by its PKTAV/SHBST label to be the I-Field) in the output register of the FIFO. Two clock cycles later, this data is available at the HIPPI Channel outputs and the REQUEST signal is asserted on the HIPPI Channel.

The REQUEST signal will remain active on the HIPPI Channel until the CNREQ input is returned to the logic low state. The S2020 will make no more read requests of the FIFO until the Destination has responded with a Connect Accept or a Connect Reject. This status is indicated by the CNOUT and ACREJ signals. If both of these outputs are at logic high, the Connection has been accepted and recognized at both Source and Destination.

The S2020 distinguishes between Connect Accept and Connect Reject conditions in accordance with the HIPPI Specification. If the CONNECT signal from the HIPPI Channel is detected for less than four clock cycles (160 nsec) it is ignored and the S2020 remains in the {REQ} state.

If the CONNECT signal is detected for more than three and less than twenty clock cycles with no activity detected on the READY signal, The Destination is judged to have issued an active Connect Rejection. In that case the S2020 will place a logic high on the CNOUT output and a logic low on the ACREJ output. This condition will persist until the Host returns the CNREQ signal to the low state or the Host executes the Mode 0 Reset sequence.

The READY signal is also monitored to determine the Connect Accept or Connect Reject status. If the READY signal is detected two or more clock cycles after the detection of CONNECT signal, the Connection is considered as accepted and the 11 pattern is posted to the CNOUT and ACREJ outputs. If the Destination drops the CONNECT signal at this point while the CONREQ input remains high, the {DESTERR} state is entered.

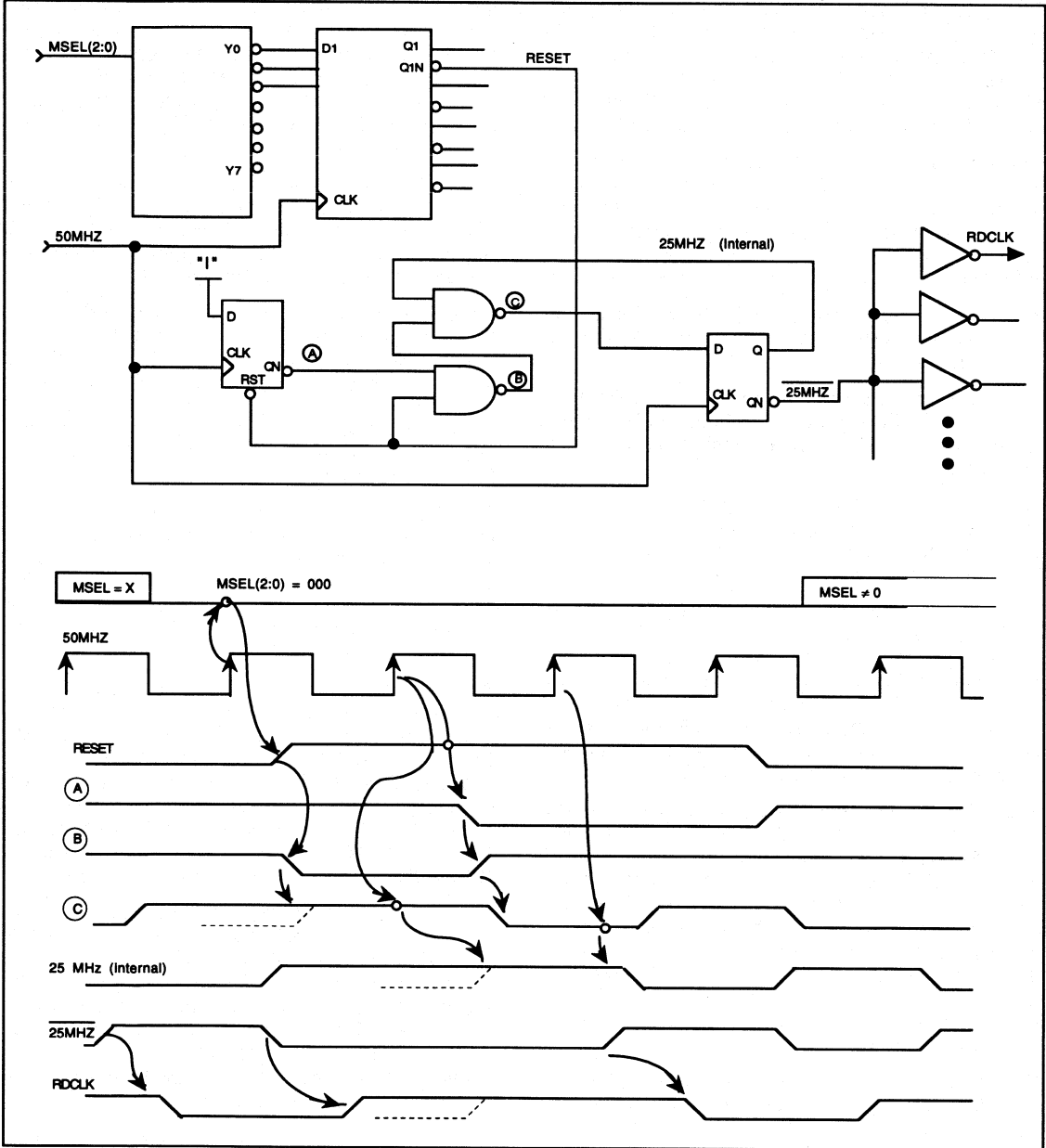
If a READY signal is detected during the Connect Request cycle or later at any time while in the {CONNECTED} state, the Ready counter in the S2020 will be incremented by one. This counter and a similar Burst counter (incremented at the last word of every Burst) are compared to generate, when not equal, the external DTREQ signal. This inequality is also used internally by the S2020 to automatically control the flow of Bursts in response to received READYs. Both counters are cleared to zero at Reset Mode or at the termination of the current {CONNECTED} state.

If the I-Field is to be sourced from a register separate from the FIFO, the NREN signal must be blocked to avoid erroneously advancing the FIFO.

Care must also be taken to control the FIFO in order to recognize the beginning of the Burst data if the PKTAV and SHBST are not used to delimit the data.

Once the Connection is established, the S2020 waits in the {IDLE} state until both BSTAV and DATAV input signals are asserted before starting any further data transfers. The BSTAV is used to initiate the search of the FIFO for the first word of the Burst and Packet. It should be noted that the BSTAV signal must be set high before the S2020 can attempt to read in the PKTAV signal.

Figure 0. S2020 50 MHz / RDCLK RESYNCH at MODE = 0 RESET (Corrected Version)



The S2020 sets the PACKET signal on the HIPPI Channel prior to setting the BURST signal as required by the HIPPI Standard. If the external DTREQ signal is low (Burst and Ready counters are equal), there are no "unanswered" READYs. In this case the S2020 will pause in the {PENDBST} state until a READY signal is detected and the Ready counter is incremented.

This function allows the Destination to "meter" the transmission of HIPPI Bursts on a one-by-one basis. A logic high on the DTREQ signal indicates that the S2020 is allowed to proceed, setting the BURST signal active and reading the next word of the Burst from the FIFO.

While this process when started proceeds automatically, the Host system can observe its progress via the DTREQ output.

The BSTAV should not be placed in the FIFO as a data bit, since it is used along with the DATAV signal to start and stop transmission gracefully at even Burst boundaries.

In all cases the BSTAV must be synchronized with the 25 MHz RDCLK for reliable operation of the S2020. The rising edge of BSTAV asynchronously controls the leading edge of the low active NREN signal.

Once the Connection is established and the first Packet and Burst are started, the S2020 Source Device will generate properly formatted Bursts with the appropriate LLRC word and inter-burst idle cycles as long as the FIFO has data and the PKTAV and BSTAV signals remain high. The BSTAV signal is used to pause at the even 256 word Burst boundaries while the Host System "refills" the FIFO.

The BSTAV signal must be set for at least the first word of the Burst. Once started the Burst will continue until 256 words are transmitted unless the SHBST signal is set active, the PKTAV signal is set inactive, or the DATAV signal is set low inactive. The word being read from the FIFO at the time that any one of these three events occurs becomes the last word of the Burst. The last word is transmitted, followed immediately by the LLRC for that Burst, and the S2020 pauses and waits for both the DATAV and BSTAV to be true (active high).

If the Burst was terminated due to an inactive PKTAV, the S2020 will wait for DATAV and BSTAV in the internal inter-packet (IDLE) state. Inter Burst pauses within a Packet cause the S2020 to wait in the {LLRC} state.

Each time a Burst reaches the last word condition, the Burst Counter is incremented and the previous value of the Burst Counter is saved in an internal Last Burst Register. In addition to the comparison between the Ready Counter and the Burst Counter used to control

the FLOWON and DTREQ signals, a second comparison between the Ready Counter and the Last Burst Register is used to prevent the Ready Counter from being incremented to a value greater than the old Burst Count. Thus the Ready Counter is prevented from "wrapping around" after receiving more than 65,535 unanswered READY signals from the Destination.

The 65,536th and subsequent READY signals will be disregarded until at least one more Burst is completed, the Burst Counter incremented, the Last Burst Register updated, and the comparator conditions re-enable the incrementing of the Ready Counter.

If the Host decides to terminate the Packet while in the inter-Burst state, a single word must be loaded in the FIFO with the accompanying PKTAV bit set to 0. While the data at the inputs of the S2020 will appear at the HIPPI Channel outputs, the inactive BURST signal will cause the Destination to ignore that data. The low PKTAV read from the FIFO will again vector the S2020 to the inter-packet (IDLE) state.

After the last Packet of the transmission is completed, the Source Host may terminate the connection by placing a logic low on the CNREQ input. The S2020 will deassert the REQUEST signal on the HIPPI Channel, enter the {TERMCON} state and remain there until the Destination deasserts the CONNECT signal. At that point the {IDLE} state will be re-entered.

As an alternative, the Host may issue a Mode 0 Reset command to terminate the Connection. The REQUEST signal will similarly be deasserted and the {INIT} state will be entered until the Destination deasserts CONNECT and the Host System deasserts CNREQ. It is recommended that the first method be used for graceful termination since the path through the {TERMCON} state allows the Host to monitor the CONNECT signal status via the CNOUT output.

The HIPPI Source device connect control State Machine (SM) controls the Connection state of the HIPPI channel to which it is attached. The Connect Control SM has inputs from the Source Host and from the HIPPI channel (remote Destination). Based on the current set of inputs and the last state of this circuit, the next Connect state is entered and a related set of outputs is generated to the Source Host and to the HIPPI channel (remote Destination).

For this discussion all external device signal names shall be CAPITALIZED and underlined, the SM input 'alphabet' or decode names shall be in double quotes (""), and all internal state names shall be enclosed in curly brackets '{}'.
'

1.1 CONNECT SM EXTERNAL INPUTS

MSEL2-0 Mode SElect lines 2-0 from the Source Host. Although there are eight possible modes for the Source device selected by these signals, only modes 0 (RESET), 2 (WAIT), and 3 (OPERATIONAL) are part of this discussion.

CNREQ CoNnect REQuest signal from the Source Host. A '1' on this signal indicates the Source Host's request to either initiate a connection or maintain the current connection on the HIPPI channel.

A '0' on this signal indicates the Source Host's request to either terminate the current connection or maintain a disconnected state on the HIPPI channel.

DSIC Destination to Source InterConnect signal from the HIPPI channel. A '0' on this signal indicates the presence of a functioning Destination on the HIPPI channel. A '1' on this signal indicates the absence of a functioning Destination on the HIPPI channel.

CON CONnect signal from the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

RDY ReaDY signal from the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

NOTE: The input signals from the HIPPI channel go through a digital 'filter' in the Source device. This filter circuit resolves metastability (of the asynchronous signals) and filters out any signal state changes which are less than two cycles in duration.

1.2 CONNECT SM INTERNAL STATES

The defined states and brief descriptions of each state follow.

{INIT} The INITIALization state is the state from which the rest of the functional connect states are entered. The main entrance to this state is when the inputs specify "RST", i.e., modes 0 or 2 with DSIC = 0 (active). The "RST" input indicates that the HIPPI Destination is present and that the Source Host is holding this device in a RESET or WAIT mode. It is intended that the Source Host enter the OPERATIONAL mode (3) when DSIC becomes active and when the Source Host is ready to enter the operational* states of this CONNECT SM (for HIPPI connections).

{IDLE} The IDLE state: This is the first operational state entered from {INIT} (above). The main entrance to this state is when this circuit is in the {INIT} state and the inputs specify "1". While in this state, both Source and Destination are ready and waiting for a connection to be established.

{REQ} The REQuest state is entered from the {IDLE} state when the Source Host initiates a HIPPI connection by asserting CNREQ. This state is exited when the Source Host drops CNREQ (abort) or when CON goes active, indicating a Destination response to the connect request.

{CON1} The CONnect1 state is entered from the {REQ} state for one cycle when CON first goes active, indicating a Destination response to the connect request. From this state, the request may be aborted, or the response will continue to be processed.

{CONn, 1<n<16} These 14 states differentiate between a CONNECT ACCEPT and a CONNECT REJECT response from the Destination. Being in one of these states implies that CON has been active (from the Destination) for 2 to 15 consecutive cycles. Receiving "CR" (inactive CON) in one of these states is a CONNECT REJECT. Receiving a "RDY" in one of these states indicates a CONNECT ACCEPT. Receiving "DR" in one of these states indicates that the Source Host wishes to abort the request.

{CON16} CONnect 16 state is entered for one cycle when the sixteenth consecutive cycle of an active CON from the Destination is received. Receiving "C" or "RDY" in this state constitutes a CONNECT ACCEPT. Receiving a "CR" in this state indicates a CONNECT REJECT response from the Destination. **NOTE:** The 'filter' circuit that the CON signal goes through effectively truncates the end of an active CONNECT signal, thereby allowing this state machine to wait 16 cycles (rather than 17) to determine if the Destination response is ACCEPT or REJECT. Receiving "DR" in this state indicates that the Source Host wishes to abort the connect requests operation.

{CONNECTED} CONNECTED state is entered when a valid connection is established across the HIPPI channel between the Source and Destination. Receiving a "CR" in this state indicates an illegal termination, initiated by the Destination. Receiving a "DR" in this state results in a connection termination, initiated by the Source Host.

* The operational states of this CONNECT SM are all but {INIT}, {LOSTDEST}, and {NODEST}.

Figure 1. S2020 Connect SM Input Decode Alphabet

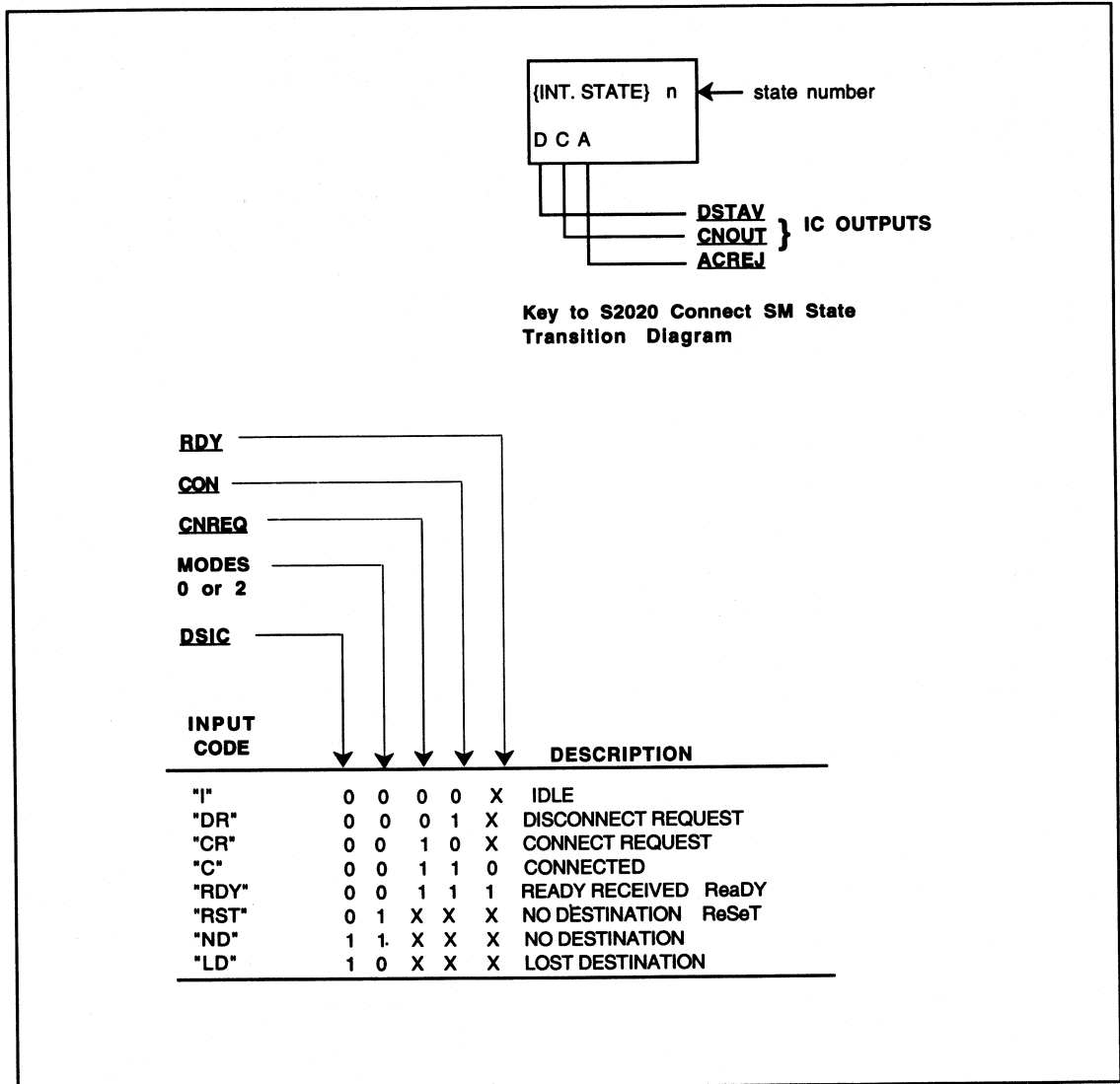
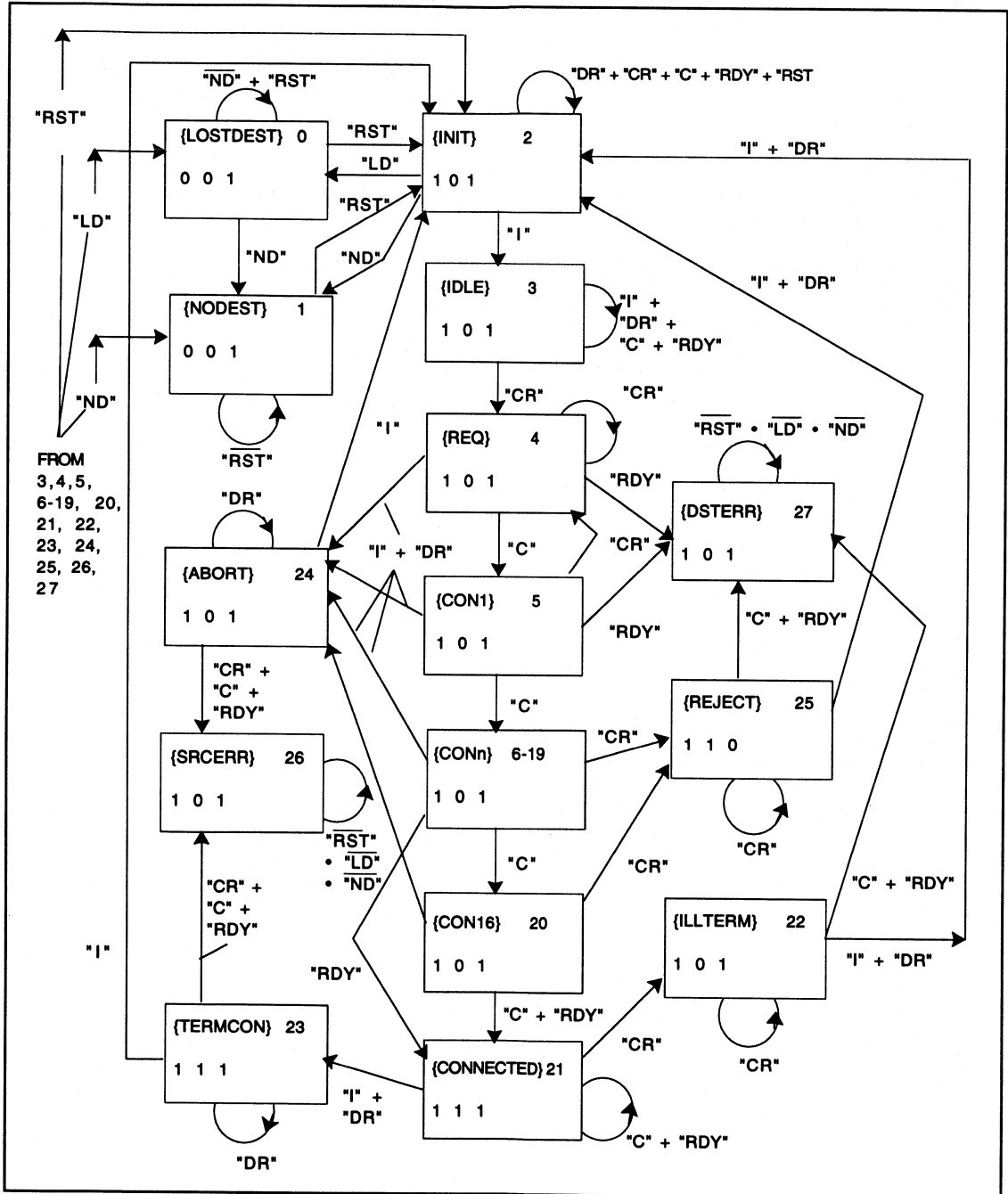


Figure 2. S2020 Connect SM State Transition Diagram



{ILLTERM} ILlegal TERMination state is entered when "CR" is received while in the {CONNECTED} state (i.e., the Destination drops CONNECT while a valid HIPPI connection exists). This state is exited when the Source Host drops CNREQ.

{TERMCON} TERMinate CONNecTion state is entered when "DR" is received while in the {CONNECTED} state (i.e., the Source Host drops CNREQ while a valid HIPPI connection exists). This circuit remains in this state until the Destination drops CONNECT.

{ABORT} The ABORT state is entered when "I" or "DR" are received while a connection is being requested (Source Host drops CNREQ before the HIPPI connection is established). This state is exited when the Destination drops CONNECT (if it was active).

{REJECT} The REJECT state is entered when the Destination's response to a connect request results in more than two (2) but less than 17 consecutive cycles of "C" (active CON). This state is exited when the Source Host drops CNREQ.

{LOSTDEST} The LOST DESTination state is non-operational, and is entered when the HIPPI Interconnect Destination-to-Source signal goes inactive during any of the operational states. This circuit remains in this state until the Source Host system forces a RESET or a WAIT mode (MSEL2-0 inputs).

{NODEST} The NO DESTination state is non-operational, and is entered anytime there is no Destination-to-Source Interconnect signal while the Source Host is forcing a RESET or WAIT mode via the MSEL2-0 inputs. This state is exited only by "RST" (the HIPPI Interconnect Destination-to-Source signal going active while still in the RESET or WAIT mode).

{SRCERR} The SouRcE ERRor state is entered when CNREQ goes active illegally. This is possible during the {ABORT} and {TERMCON} states, where this circuit is waiting for the channel to go idle after a Source initiated termination. While in this state, the Source device will report the error by asserting the SQERR output. The SeQuence ERRor will be further identified as a SouRcE ERRor by setting SRNDS to a '1'.

{DSTERR} The DeSTination ERRor state is entered when CON or RDY go active illegally; RDY should not be active during the {REQ} or {CON1} states, and neither CON or RDY should be active during the {ILLTERM} state. While in the {DSTERR} state, the Source device will report the error by asserting the SQERR output. The SeQuence ERRor will be further identified as a DeSTination ERRor by clearing SRNDS to a '0'.

1.3 CONNECT SM EXTERNAL OUTPUTS

In addition showing the state transitions resulting from external inputs to the Source chip, Figure 2 also shows the external output signals for each defined state.

DSTAV DeSTination AVailable signal to the Source Host. A '1' on this signal indicates the presence of a functioning Destination on the HIPPI channel. A '0' on this signal indicates the absence of a functioning Destination on the HIPPI channel.

CNOUT CoNnect OUT signal to the Source Host. This signal, along with the ACREJ signal (below), indicates the current connection state on the HIPPI Channel. During a Connect Request, a '1' on this signal indicates the receipt of a valid response to the Source (from the Destination) for the Connect Request. A '0' on this signal, during a Connect Request, indicates no response (yet) from the Destination.

After a connection is accepted, this signal shall be the same state as CONNECT on the HIPPI channel, and therefore will indicate to the Source Host an illegal termination (termination initiated by the Destination), or the acknowledgment by the Destination of a normal termination.

ACREJ ACcept/REject signal to the Source Host. This signal, along with the CNOUT signal (above), indicates the Destination's response to the Source's Connect Request. A '1' on this signal when CNOUT goes active during a Connect Request indicates an ACCEPTEd connection. A '0' on this signal when CNOUT goes active during a Connect Request indicates a REJECTEd connection.

2.0 S2020 HIPPI DATA/FIFO CONTROL

The HIPPI Source device Host Data/FIFO State Machine (SM) is part of the Host Data/FIFO Control Block. The State Machine controls the flow of data and status from the Source Host FIFO to the S2020 Source device. The Data/FIFO SM also controls the generation of the HIPPI channel control signals to properly delimit the data and respond to the data transfer commands of the Source Host system.

The Host Data/FIFO SM has inputs from the Source Host system, the Connect Control State Machine and the internal Flow control circuit. Based on the current set of inputs and the last state of this state machine, the next Data/FIFO state is entered and a related set of outputs is generated to the Source Host and to the HIPPI channel.

As before, all external device signal names shall be CAPITALIZED and underlined, the SM input 'alpha-beta' or decode names shall be in double quotes ("), and all internal state names shall be enclosed in curly brackets '{}'. Signals internal to the Source device other than previously defined state names shall be in caret brackets '< >'.
< >

2.1 HOST DATA/FIFO SM INPUTS

2.1.1 External Inputs

PKTAV PacKeT AVailable signal from the Source Host: Indicates the current delimiting of data across the HIPPI channel. A '1' on this signal indicates the Source Host's request to either initiate a Packet or maintain the current Packet on the HIPPI channel. A '0' on this signal indicates the Source Host's request to terminate the current Packet.

BSTAV BurST AVailable signal from the Source Host: Indicates the availability of other controls and data from the Source Host system. A '1' on this signal will enable the Source device to initiate a new read sequence from the Source Host FIFO. A '0' will disable the initiation of any new read sequences. This signal must not go active until at least one valid HIPPI Burst is available from the Source Host. If this signal goes inactive after a Burst read sequence has begun, the current burst will be completely read, but subsequent read operations will be disabled.

SHBST SHort BurST signal from the Source Host: Indicates the end of a HIPPI data Burst with a length shorter than 256 words. A '1' on this signal during an active Packet will terminate the current burst with the current word being the last word of the burst, and will initiate the completion and subsequent transmission of the LLRC word. A '0' on this signal will allow the Source device to transfer at least one more data word from the Source Host FIFO to the HIPPI channel unless the current word is the 256th word of the current Burst.

DATAV DATA AVailable signal from the Source Host: Indicates the availability of at least one more data word, or I-Field in the Source Host FIFO. A '1' on this signal will enable the Source device to advance any pending operation that requires more data from the Host. A '0' on this signal will prevent the advancement of any such operations, and will legally terminate the current data Burst being transferred across the HIPPI channel.

2.1.2 Internal Inputs

<FLOWON> Flow control signal from the READY/BURST counter block: Indicates the current capacity of the HIPPI channel (Destination) to accept a HIPPI Burst. A '1' on this signal enables the transmission of one Burst to be initiated, if available from the Source Host system. A '0' on this signal allows the completion of any Burst that has been initiated, but disables any subsequent Bursts. The state of this signal is observable at the DTREQ (DaTa REQuest) output of the Source Device.

<CONREQ> Connect request signal from the Connect Control State Machine: This signal is active for any of the Connect SM states {REQ} thru {CON16} during a normal HIPPI channel Connection Request sequence. When active, this signal allows the Data/FIFO SM to read the I-Field from the Source Host FIFO, and then present the I-Field data and the REQ signal to the HIPPI channel.

<CONNECTED> Connected signal from the Connect Control State Machine: This signal is active only for the {CONNECTED} state. A '1' on this signal enables all the HIPPI data delimiting and transfer functions. A '0' will disable all delimiting and transfer functions.

<256THWRD> The Terminal Count signal from the 8-bit word counter of the Host Data/FIFO Control Block: This signal indicates that the 256th word of the current Burst is being transferred from the FIFO to the Source device. A '1' on this signal will legally terminate the current Burst. A '0' will allow the Source device to transfer at least one more data word.

<RESET> The Reset signal from the Clock Control Block: This signal is the registered decode of the MSEL2-1 for the Mode = 0 state. A '1' on this signal indicates the Reset state for the entire Source device including the Host Data/FIFO SM. A '0' on this signal will enable all other inputs to the SM.

2.2 HOST DATA/FIFO SM INTERNAL STATES

The defined states are as follows:

- {INIT}** The INITialization state is the entry point of the Host Data/FIFO SM. This state is unconditionally entered by a "RST" decode of the inputs. The state is also entered by a "DSCN" decode representing the disconnected state of the HIPPI channel. This state remains active if a "CNRQ" decode is true while the "NODT" decode remains false, indicating a Connection request without Data available from the FIFO. The state is exited to the {RDIFL} state by the decode of "CNRQ" and "DTAV" both true. The decode of "CON" in this state is a Destination error and the {DESTERR} state is entered.
- {RDIFL}** The ReaD I-Field state is entered when a Connect request is initiated by the Source Host system and there is data available from the Source Host. When in this state the FIFO read function is active resulting in an active low level on the NREN output. The read operations of the FIFO will continue until the "IFLD" decode is true, at which point the {PSTIFLD} state is entered. The decode of "RST" or "DSCN" will exit this state back to the {INIT}. The decode of "CON" in this state will force entry to the {DESTERR} state.
- {PSTIFLD}** The PoSt I-Field state is entered when an I-Field is successfully read from the Source Host system. While in this state, the I-Field data is presented to the HIPPI channel and the REQ signal is asserted on the HIPPI channel. Although the NREN signal remains inactive, the internal data and parity pipeline remains active. If the I-Field was presented from the FIFO, the FIFO output register is stable with that data. If the FIFO data outputs were disabled, any other data applied to the Source device inputs (ie. via 3-state multiplexing) would appear at the HIPPI channel outputs two 25MHz clock cycles later. The decode of "DSCN" or "RST" will force entry to {INIT}. The decode of "CON" indicates successful connection to the HIPPI channel, and the {IDLE} state will be entered.
- {IDLE}** The IDLE state is maintained when there is a Connection established, but there is no Packet and no data to transmit. No read operations are performed on the FIFO in this state. When "DRDY" indicates that Data and Burst are available, the {WAITPKT} state is entered.
- {WAITPKT}** The WAIT PacKeT state is entered when there is no active Packet and the decode of "DRDY" is true, indicating that both BSTAV and DATAV were asserted from the Source Host system.
- This state will read one word from the Source Host FIFO. If the "NPIF" decode is detected at the read (ie. PKTAV not asserted) then the {IDLE} state is entered. This loop of {IDLE}-{WAITPKT} will advance the FIFO up to the next valid Packet.
- Any data words not delimited by PKTAV will appear at the HIPPI channel, but the PKT and BST signals on the HIPPI channel remain inactive. If the PKTAV is asserted at the read, the {PENDBST} state is entered.
- {PENDBST}** The PENDING BurST state is entered when the Source Host system has a Burst of data to send. No read operations are performed in this state. If the "FLOF" decode is true (indicating that the Destination is not Ready for a Burst), this state is maintained. When the "FLOF" decode is false then this state is exited. If the PKTAV signal is deasserted, the {SRCERR} state is entered. If the pending Burst has only one word either by the assertion of SHBST in the first word or by the deassertion of DATAV (the last word in the FIFO was read), then the {LSTWD} state is entered. If the Burst has more than one word, then the {BURST} state is entered.
- {BURST}** The BURST state is entered when everything is prepared for transmission; a valid connection is established on the HIPPI channel, the Source Host system has at least one Burst available, a Packet is currently active, and the Destination is capable of receiving at least one complete Burst. In this state, Source Host system read operations are performed continuously until the the Packet is terminated, the 256th word is read, the SHBST signal is asserted, or the Source Host FIFO runs out of data. When any of these terminating conditions occur, the {LSTWD} state is entered.
- {LSTWD}** The LaST WorD state is entered when the last word of the current Burst has been read from the Source Host system. No read operations are performed in this state. This state is only one cycle in duration, and except for error conditions, the {LLRC} state is next.

{LLRC} The LLRC state is entered after the {LSTWD} state. This state will deassert the BST signal on the HIPPI channel while completing and posting the LLRC word to the channel. If the current Packet has been terminated by the Source Host system (PKTAV was deasserted at the read of the last word of the Burst), then the {IDLE} state will be entered. If the "DRDY" decode is true (BSTAV and DATAV are both asserted), and the current Packet is to be continued, then the {WTBST} state is entered. If the current Packet is to be continued, but the "DRDY" decode is false, then this state is maintained. No read operations are performed in this state.

{WTBST} The Wait BurST state is entered after one Burst is complete and the "DRDY" decode is true. One read operation is performed in this state. If PKTAV is asserted at that read operation, then the {PENDBST} state is entered. If PKTAV was deasserted at the read, then the {IDLE} state is entered.

{SRCERR} The Source Error state is entered if the PKTAV changes from a "1" to a "0" and the "FLOF" decode is false during the {PNDBST} state.

This state is exited to the {INIT} state when the HIPPI Connection is broken or if the <RESET> signal is true. The state is exited to the {DSTERR} state if the "CNRQ" decode is true. This error state is reported to the Source Host system by setting both SQERR and SRNDS output to logical "1".

{DSTERR} The Destination Error state is entered if the <CONREQ> signal is received while a valid HIPPI Connection is already established. The most likely cause of this error is an unstable signal on the HIPPI channel from the Destination. This state is also entered if CON is asserted when not expected (during the {INIT} or {RDIFL} states). This state is exited by either the "RST" or "DSCN" decodes being true, either of which force the {INIT} state. This error state is reported to the Source Host system by setting the SQERR output to "1" and the SRNDS output to "0".

2.3 DATA/FIFO SM EXTERNAL OUTPUTS

REQ REQuest signal to the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

BRST BuRST signal to the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

PKT PacKeT signal to the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

NREN Not Read ENable signal to the Source Host system FIFO. This is an active low signal to be used to enable the FIFO to load a new data word into its output register. This signal is controlled not only by the state of the Data/FIFO SM, but also by the inputs PKTAV, SHBST, DATAV and BSTAV.

As an example, in the {RDIFL} state, the detection of the "IFLD" decode (PKTAV = '0', SHBST = '1') will asynchronously deassert (raise to logical '1') the NREN signal prior to the next rising edge of RDCLK such that the tagged data remains held in the FIFO's output buffer. Similarly, the "DRDY" decode asynchronously controls the assertion of NREN on the transition from the trapped {IDLE} state to the {WAITPKT} state.

Figure 3. Data/FIFO SM Input Decode Alphabet

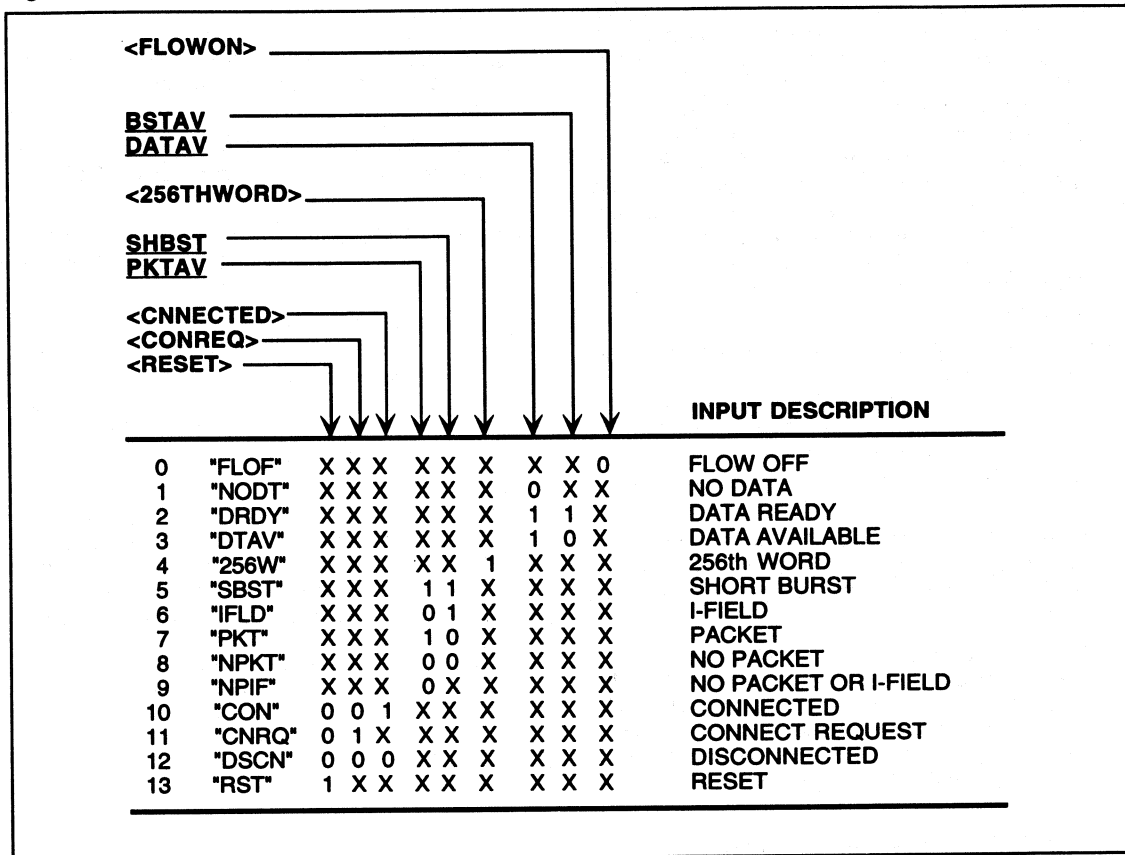


Figure 4. S2020 Data/FIFO Interface SM State Transition Diagram

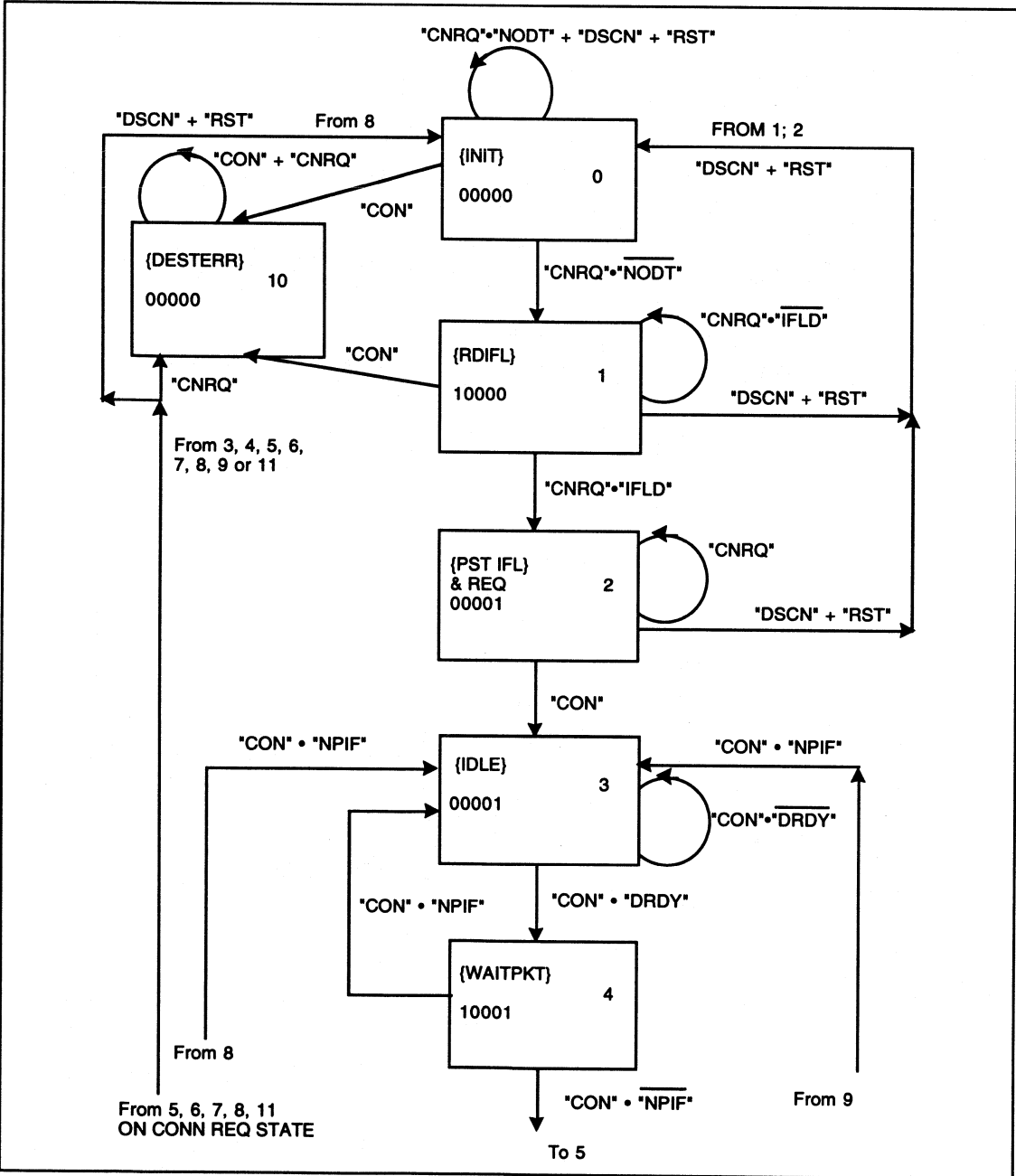
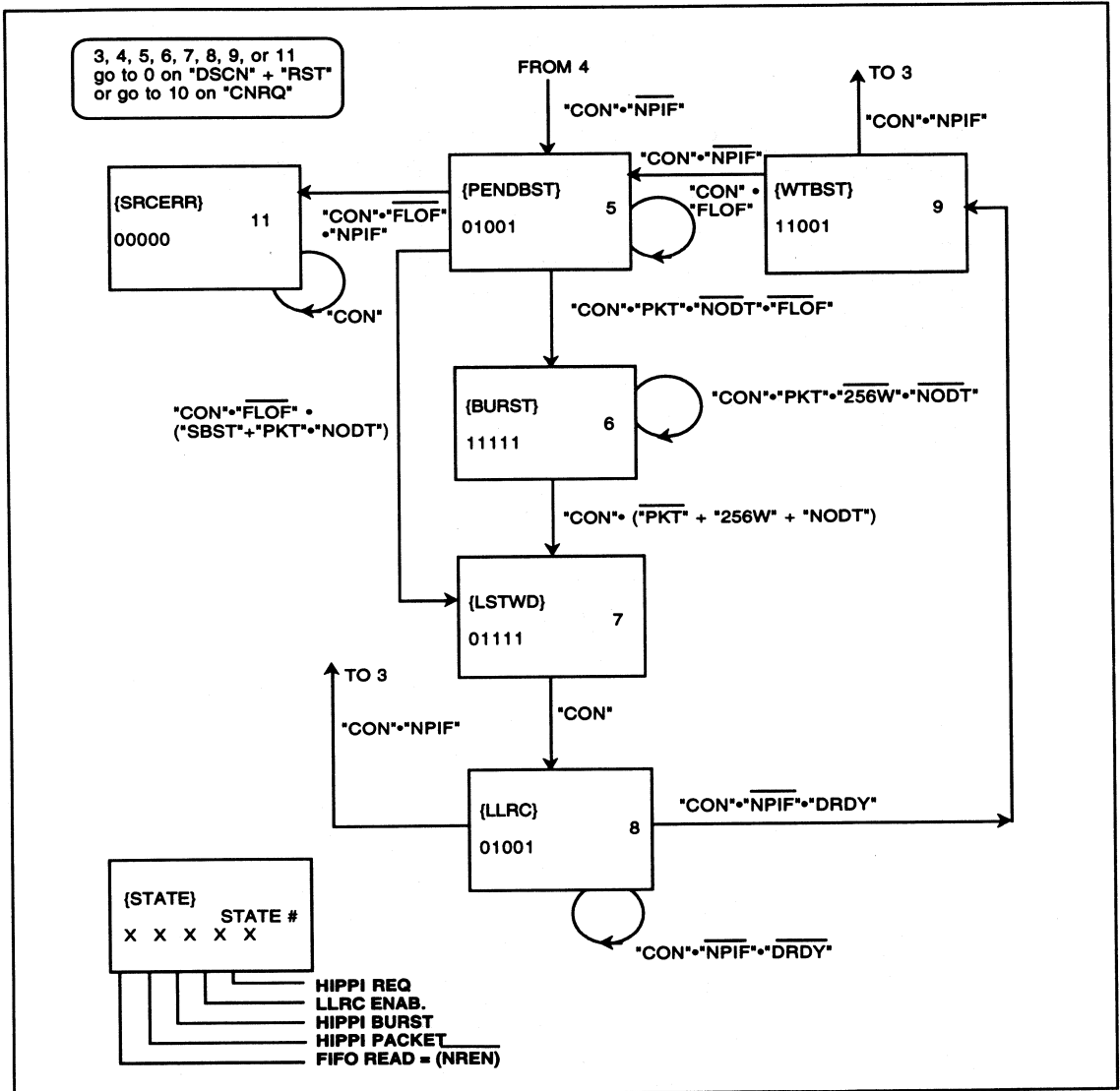


Figure 4. S2020 Data/FIFO Interface SM State Transition Diagram (continued)



3.0 S2021 HIPPI DESTINATION CONNECT CONTROL

S2021 HIPPI Destination Device Normal Functional Sequence

The S2021 Destination Device responds to Connection and data transfer requests received from the HIPPI Source.

The RESET Command (Mode 0) initializes all internal registers and state machines of the S2021. The Reset Command also places all Host side TTL outputs in the high-impedance state and the HIPPI Channel outputs (CONNECT and READY) in the deasserted state. The Destination to Source Interconnect output (DSIC) is also placed in the high logic low state. If the circuit recommended on page 19 of the S2020/S2021 Device Specification is used, this will result in a high inactive level on the HIPPI Channel DSIC signal.

After the RESET Command initialization is complete the Device should be placed in the operational state through the Mode 5 Command. The Host system should place a logic low signal on the CONIN input. The SRCV output should then be monitored to determine the status of the Source Driving the HIPPI Channel.

If this signal is at a logic 0, either the Source to Destination Interconnect (SDIC) is inactive or one of the Channel Control signals (REQUEST, PACKET or BURST) from the Source is active. A logic 1 on the SRCV output indicates the presence of a functional Source capable of initiating data transfers.

In the initialized but not connected condition, the S2021 cycles through the {DISCON0-2} state sequence. This is monitored by the host system by observing the 5,6,7 repeating sequence on the SELB(2:0) outputs and the appropriate internal status words on the data outputs.

At this point the Host system may initialize the internal Buffer Counter of the S2021 with the number of Burst-sized (256 word) buffer blocks available in the external FIFO and memory system. This is accomplished by placing a rising edge signal on the RDYIN input for each buffer block to be counted. Thus, if the available FIFO is 4K words deep, and the process that empties the FIFO is slower than the data rate of the HIPPI Channel, 16 pulses would be supplied to the RDYIN input.

During the disconnected condition, the state of the Buffer counter can be monitored by observing its contents in the lower half of the Flow status Word 2 which is presented to the outputs during the SELB=7 state. The Buffer Counter has a capacity of $2^{exp16} - 1$ counts (65,535 buffers). Inputs to RDYIN greater than this will be ignored.

If the process that empties the FIFO is faster than the data rate of the HIPPI Channel, the RDYIN input may be driven by a free-running TTL signal at a frequency less than or equal to 12.5 MHz. In that configuration the Buffer counter will quickly fill to 65,535.

After a connection is accepted, the READY signals are continuously generated at the maximum rate allowed by the HIPPI Standard (160 ns asserted, 160 ns deasserted) and counted in the internal READY Counter until the two counters are equal. If a continuous toggling signal is applied to RDYIN, 65,535 READY pulses will be sent at the maximum rate. From that point on each received Burst will allow one and only one READY pulse to be generated.

When an active REQUEST is detected on the HIPPI Channel the {REQCON} state and the {IFIELD} state are entered. The data on the HIPPI Channel is presented at the outputs of the S2021 along with a logic high on the CONRQ output.

The SELB outputs assume the 001 code for the HIPPI I-Field. At this point the Host system must decide to either accept or reject the connection. The Host system must place a logic high on the CONIN input while holding the ACCRJ at logic high to accept the connection. If ACCRJ is held low when CONIN is asserted the connection will be rejected. For applications where all REQUESTs must be accepted, the CONRQ output may be connected directly to the CONIN input and the ACCRJ input held high.

If the REQUEST is rejected (CONIN =1, ACCRJ =0) the S2021 will assert the CONNECT signal on the HIPPI Channel for four clock cycles and then deassert the CONNECT signal for four cycles. If at the end of this sequence the Source has deasserted the REQUEST signal the S2021 will return to either the {IDLDSAB} state (CONIN=1) or the {IDLENAB} state (CONIN=0). When the {IDLENAB} state is reached the S2021 is able to process another Connection Request from the Source.

If the Host system has accepted the connection request (CONIN=1, ACCRJ=1) the S2021 will return to the {DISCON0-2} sequence until the CONNECT signal has been asserted for four clock cycles. At that point the S2021 enters the {IDLE} state (SELB=3) and remains there until the Source asserts the PACKET signal on the HIPPI Channel.

When the PACKET signal is detected from the Channel, the S2021 responds by placing a logic 1 on the PKOUT output and waits for a Burst data transfer to begin. The SELB bus remains in state 3. If the Source drops the PACKET on the Channel without beginning a Burst, i.e. attempts to form an "empty" Packet, the S2021 will detect a Sequence Error.

The detected Sequence Error will force the CONNECT to deassert, issue one Sequence Error word on the data outputs (SELB=4), and then return to the {DISCON0-2} sequence with its accompanying SELB5,6,7 sequence.

In the normal data transfer procedure, the Source will follow the asserted PACKET by asserting the BURST signal at least one clock cycle later. If the BURST is asserted at the same time as or before PACKET, the Sequence Error process described above will occur.

A legally asserted and detected Burst will cause the S2021 to place a logic 1 on the BROUT output, place the SELB bus to state 0, and place the received data and parity bits on the data and parity outputs as the first word of the Burst.

The S2021 will continue to place received data and parity on the outputs (with SELB=0) until the Source deasserts the BURST signal. The S2021 makes no distinction between short Bursts (less than 256 words), normal Bursts (exactly 256 words), or "extended" Bursts (greater than 256 words). As long as the Source provides an LLRC word calculated with a modulo 256 word count in accordance with the HIPPI Specification, the S2021 will process the Burst without error.

The Burst is ended when the S2021 detects that the Source has deasserted the BURST signal on the HIPPI Channel. The data and parity word received with the deasserted BURST are placed on the outputs as the LLRC word (SELB=2). The received LLRC word is compared with the LLRC internally calculated and any mismatch will set the RLLER output to logic 1 at the next clock cycle.

As each Burst is completed, the internal Burst Counter is incremented by one as described above. During the inter-Burst idle time the SELB bus is placed in state 3 and the general operational status word appears on the data outputs. That status word allows the comparison flags for the Flow Control circuit to be observed.

The ALLBSTS flag is 1 when the READY and BURST counters are equal. The 64KBFRS flag is 1 when the Last Burst and Buffer counters are equal. The ALLRDYS flag is one when the READY and Buffer counters are equal.

The S2021 will continue to process received Bursts until the Source deasserts the PACKET signal. The inter-Packet condition will also result in the general operational status word appearing at the outputs (with SELB=3).

At this point the Source may elect to start another Packet or end the Connection by deasserting the REQUEST signal. It should be noted that the Source may deassert the REQUEST signal at the same time as it deasserts the PACKET signal. In either case the S2021 returns to the SELB5,6,7 sequence (internal states {DISCON0-2}).

The value in the BURST Counter is loaded into the READY Counter, since the previous difference between these two counters represents the READYS that were "lost" or unanswered by the now disconnected Source.

Unless the Destination Host System resets the flow counters (NRRDY set to logic 0) or resets the S2021 (Mode 0 Reset) The available Buffer count is preserved for the next Connection.

The HIPPI Destination device Connect Control State Machine (SM) controls the Connection state of the HIPPI channel to which it is attached. The Connect Control SM has inputs from the Destination Host and from the HIPPI channel (remote Source). Based on the current set of inputs and the last state of this circuit the next Connect state is entered and a related set of outputs is generated to the Destination Host and to the HIPPI channel (remote Source).

For this discussion, all external device signal names shall be CAPITALIZED and underlined, the SM input 'alphabet' or decode names shall be in double quotes (") and all internal state names shall be

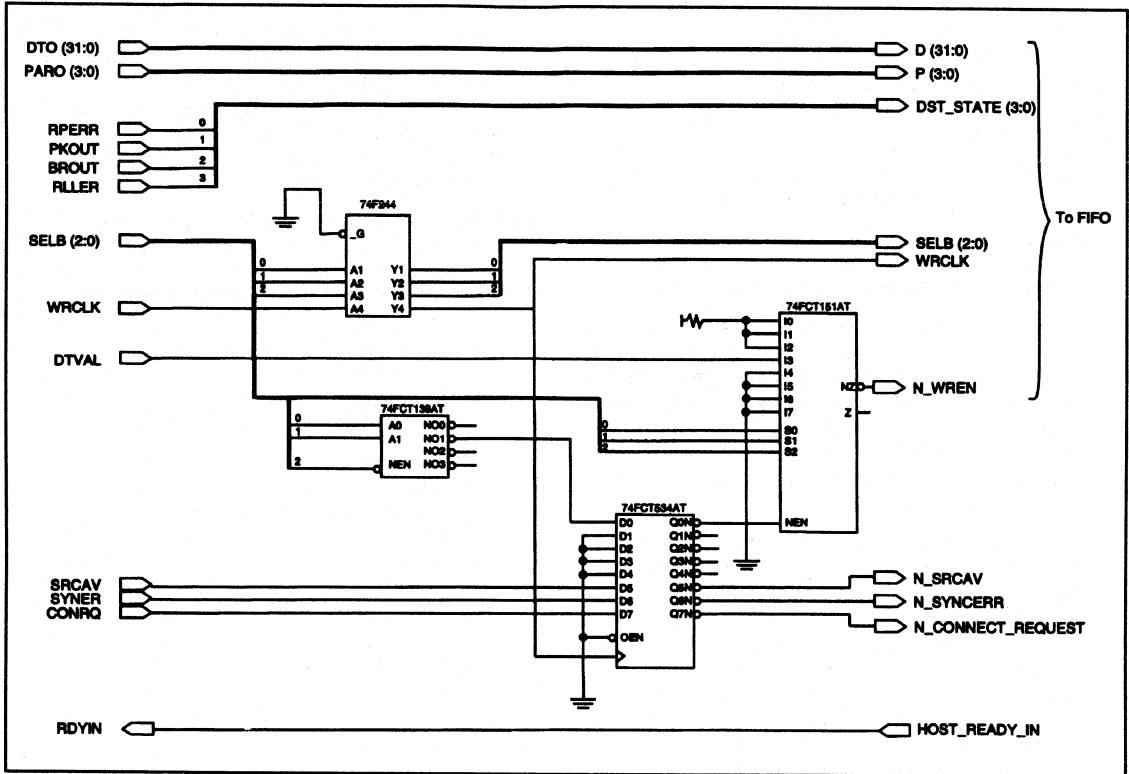
enclosed in curly brackets '{}'. Signals internal to the Destination device other than previously defined state names shall be in caret brackets '< >'.

3.1 CONNECT STATE MACHINE EXTERNAL INPUTS

MSEL2-0 Mode SElect lines 2 - 0 from the Destination Host system. Although there are eight possible modes for the Destination device selected by these signals, only modes 0 (RESET) and 5(OPERATIONAL) are part of this discussion.

SDIC Source to Destination InterConnect signal. A '0' on this signal indicates the presence of a functioning Source on the HIPPI channel. A '1' on this signal indicates the absence of a functioning Source on the HIPPI channel. This signal is debounced and inverted to form <NRAWSDIC> (active high). A '1' on this input (or '0' on the <NRAWSDIC> signal) is sufficient to force the internal "DSBL" decode independent of other inputs.

Figure 4B. S2021 Destination FIFO Interface



REQ REQuest signal from the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec. When debounced and synchronized as <SYNCREQ> this signal is used in the input 'alphabet' decoder for the Connect Control SM.

CONIN CONnect IN signal from the Destination Host system. This signal when asserted during a Connection Request cycle, indicates an active response to the Request by the Destination Host system.

If this signal is asserted prior to the detection of a Connection Request cycle, the "IDSB" decode inhibits its response to Requests from the HIPPI channel.

If this signal remains low after an asserted **REQ** from the HIPPI channel, the channel remains 'hung' in the Connection Request state until the Remote Source exercises a time-out of the unanswered request. The **CONIN** signal may be tied directly to the **CONRQ** output, and the **ACCRJ** used as the active Connection control by the Destination Host system.

ACCRJ ACcept/not ReJect signal from the Destination Host system. This signal together with the **CONIN** signal described above, control the Destination device's response to a Connection Request (asserted **REQ**) from the HIPPI channel remote Source. If a '1' is placed on this input, the accompanying active **CONIN** is considered as an acceptance response to the Connection Request. If a '0' is placed on this input, the asserted **CONIN** will result in an active Rejection of the Connection Request (the **CON** signal to the HIPPI channel will be asserted for four clock cycles only, then deasserted). The active Rejection avoids possible 'hung' conditions on the HIPPI channel.

3.2 CONNECT STATE MACHINE INTERNAL INPUTS

<**RSTCON**> ReSeT CONnection signal from the internal Data/FIFO Control SM. This signal is asserted during error states of the DATA/FIFO SM. When asserted, this signal is sufficient to force the internal "DSBL" decode independent of other inputs.

3.3 CONNECT SM INTERNAL STATES

{**DISABLED**} The DISABLED state of the Connect SM is forced by the decode of "DSBL" from the input 'alphabet'. "DSBL" will force this state from all other states of the Connect SM. While in this state the **SRCAV** output is held to '0'. This state is exited to the {**IDLDSAB**} state if the "IDSB" decode is true (**CONIN** asserted with no **REQ** active). The {**IDLENAB**} state will be entered if the "IENB" decode is true.

{**IDLDSAB**} THE IDLe DiSABled state is entered from the {**DISABLED**} state, the {**IDLENAB**} state, and from the {**REJCOMPL**} state when the "IDSB" decode is true. This state will persist until the "IDSB" decode is false. The normal exit from this state is to the {**IDLENAB**} state if the "IENB" decode is true. The "DSBL" decode will force exit to the {**DISABLED**} state. Any other decode forces the {**HANGERR**} state.

{**IDLENAB**} The IDLe ENABled state is entered from the {**DISABLED**} state, the {**IDLENAB**} state, and from the {**REJCOMPL**} state when the "IENB" decode is true. This state will persist until the "IENB" decode is false. This state is exited to the {**REQCON**} state if the "RQCN" decode is true, the {**ACC0**} state if the "CNAC" decode is true, the {**REJ0**} state if the "CNRJ" decode is true, and the {**IDLDSAB**} state if the "IDSB" decode is true.

{**REQCON**} The REQuest CONnection state is entered from the {**IDLENAB**} state at the detection of an asserted **REQ** from the HIPPI channel while **CONIN** is deasserted ("RQCN" decode is true). This state will persist while "RQCN" remains true. If the **REQ** is deasserted, this state is exited to the {**IDLENAB**} state. This state is exited to the {**ACC0**} state if the "CNAC" decode is true, the {**REJ0**} state if the "CNRJ" decode is true, the {**IDLENAB**} state if the "IENB" decode is true and the {**IDLDSAB**} state if the "IDSB" decode is true.

{**ACC0-3**} The ACcept 0 through ACcept 3 states are entered at {**ACC0**} from either {**IDLENAB**} or {**REQCON**} when the "CNAC" decode is true. These states are then sequenced in order unless overridden by a "DSBL" decode. The **CON** signal is asserted on the HIPPI channel for these states. This sequence is exited to the {**CONNECTED**} state if the "DSBL" decode remains false.

{**CONNECTED**} The CONNECTED state is entered when a valid Connection is established across the HIPPI channel between the Destination and the Source. This state enables the output of the **RDY** signals on the HIPPI channel to initiate the transfer of Burst data from the remote Source. This state will persist while either the "CNAC" or the "CNRJ" decodes are true and the "DSBL" decode remains false. The **CON** signal on the HIPPI channel remains asserted while in this state. This state is exited to the {**REJCOMPL**} state if the "RQCN" decode is true, the {**DISCON0**} state if the "IENB" decode is true, and the {**INCOMPDCON**} state if the "IDSB" decode is true.

Figure 5. S2021 Connect SM Input Decode Alphabet

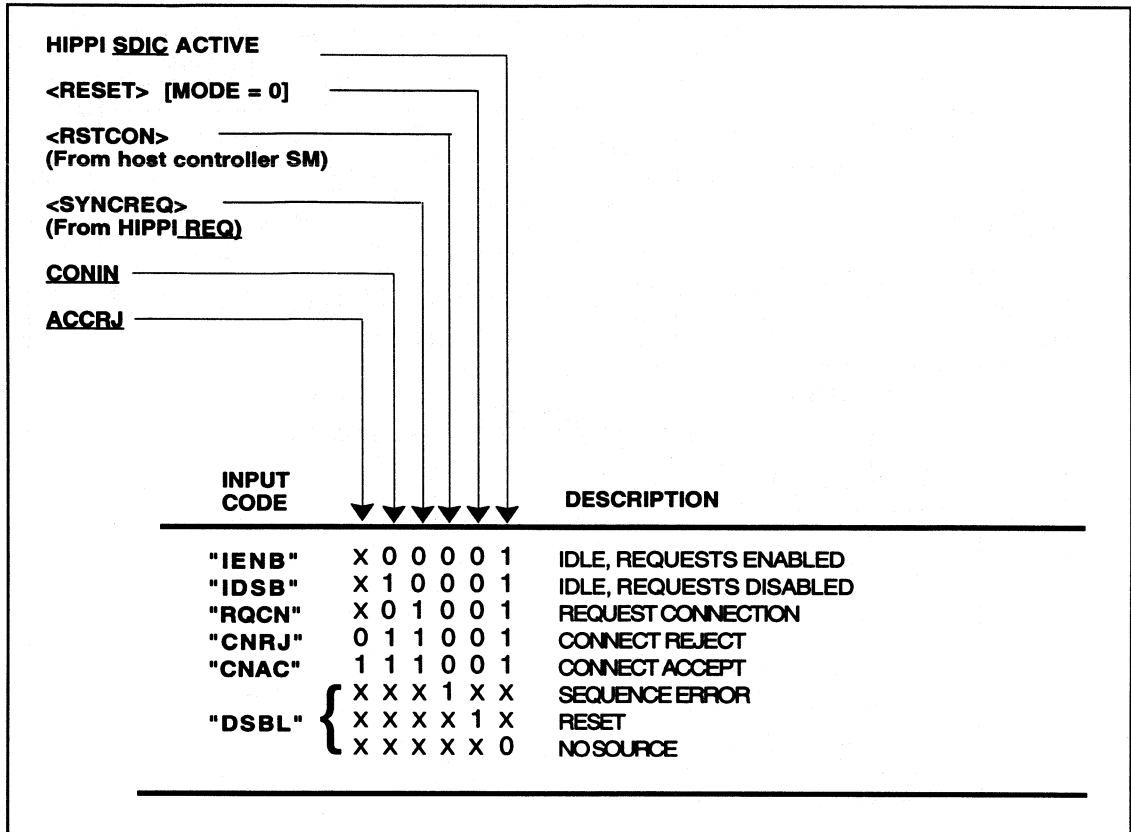


Figure 6. S2021 Connect SM State Transition Diagram

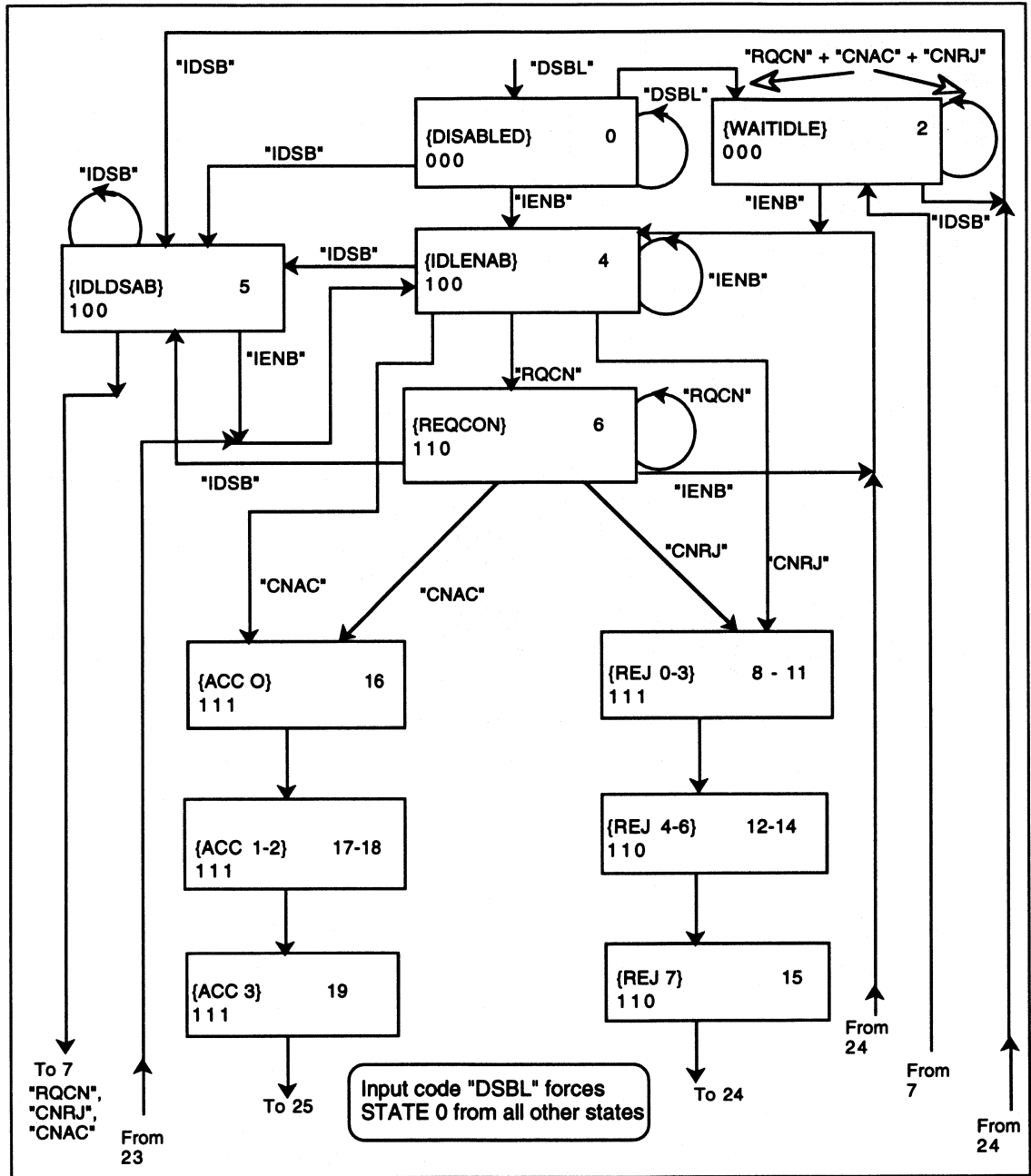
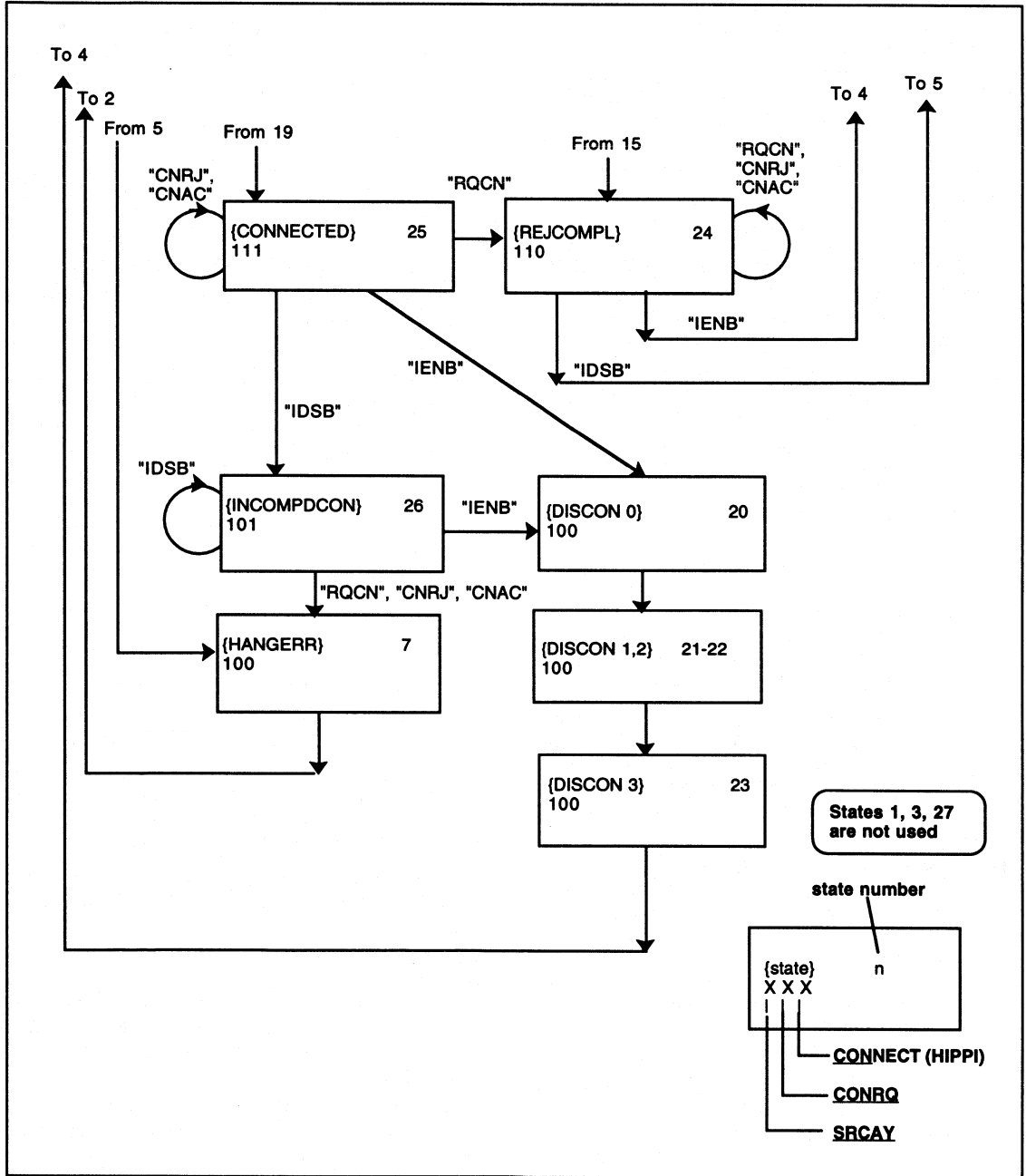


Figure 6. S2021 Connect SM State Transition Diagram (continued)



{REJ0-3} The REJect 0 through REJect 3 states are entered at {REJ0} from either {IDLENAB} or {REQCON} when the "CNRJ" decode is true. These states are sequenced in order unless overridden by a "DSBL" decode. The CON signal is asserted on the HIPPI channel for these states, providing the minimum four clock cycle response for an active Connection Reject. This sequence is exited to the {REJ4} state if "DSBL" remains false.

{REJ4-7} The REJect 4 through REJect 7 states are entered at {REJ4} from {REJ3}. These states are sequenced in order unless overridden by a "DSBL" decode. The CON signal is deasserted for these states, defining the active Connection Reject. This sequence is exited to the {REJCOMPL} state if "DSBL" remains false.

{REJCOMPL} The REJect COMPLete state is entered from the {REJ7} state if "DSBL" decode is false, or from the {CONNECTED} state if the "RQCN" decode is true. This state persists while "RQCN", "CNRJ" or "CNAC" are true. This state is exited to the {IDLENAB} state if the "IENB" decode is true, or to the {IDLDSAB} state if the "IDSB" decode is true.

{DISCON0-3} The DISCONnect 0 through DISCONnect 3 states are entered in sequence from the {CONNECTED} state or from the {INCOMPDCON} state when the "IENB" decode is true. These states are sequenced in order unless overridden by a "DSBL" decode.

The function of this sequence is to assure that at least four clock cycles of deasserted CON on the HIPPI channel to recognize the Disconnected condition of the channel. This sequence is exited to the {IDLENAB} state if the "IENB" decode is true.

{INCOMPDCON} The INCOMPLete DisCONnect state is entered from the {CONNECTED} state if the "IDSB" decode is true (REQ on the HIPPI channel is deasserted, but CONIN remains asserted). This state persists if the "IDSB" decode remains true. This state is exited to the {DISCON0} state if the "IENB" decode is true, or to the {HANGERR} state if either the "RQCN", "CNAC" or "CNRJ" decodes are true.

{HANGERR} The HANG ERRor state is entered from from either the {IDLDSAB} or {INCOMPDCON} states if either the "RQCN", "CNAC" or "CNRJ" decodes are true. These decodes represent erroneous sequences of the Host or channel control signals. This state is exited after one clock cycle to the {WAITIDLE} state.

{WAITIDLE} The WAIT IDLE state is entered from the {HANGERR} state if the "DSBL" decode remains false. This state persists if either the "RQCN", "CNAC" or "CNRJ" decodes are true. This state is exited to the {IDLENAB} state if the "IENB" decode is true.

3.4 CONNECT SM EXTERNAL OUTPUTS

SRC AV SouRCe AVailable signal to the Destination Host system. A "1" on this signal indicates that the HIPPI channel, from the remote Source through the local Destination device is available.

A "0" on this signal indicates that either the SDIC is inactive, the Destination device is in a Reset or test mode, or that the Data/FIFO SM is in an Error state.

CON RQ CONNect ReQuest signal to the Destination Host system. A "1" on this signal indicates that the REQ signal from the HIPPI channel has been asserted and recognized by the Destination device. A "0" on this signal occurs when the REQ signal is deasserted.

This signal when active indicates the time during which the CONIN input may be used to actively accept or reject a Connection Request.

CON CONNect signal to the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

4.0 S2021 HIPPI DATA/FIFO CONTROL

The HIPPI Destination device Host Data/FIFO State Machine' (SM) is part of the Host Data/FIFO Control Block'. The State Machine controls the flow of data and status from the HIPPI channel, through the S2021 Destination device to the Destination Host FIFO and the associated status registers.

The Data/FIFO SM also provides addressing control to vector data and status words to their appropriate registers.

The Host Data/FIFO SM has inputs from the HIPPI channel and the Connect Control SM. Based on the current set of inputs and the last state of this state machine, the next Data/FIFO state is entered and a related set of outputs is generated to the Destination Host system.

As before, all external device signal names shall be CAPITALIZED and underlined, the SM input 'alphabet' or decode names shall be in double quotes ("), and all internal state names shall be enclosed in curly brackets '{}'. Signals internal to the Source device other than previously defined state names shall be in caret brackets '< >'.
< >

4.1 HOST DATA/FIFO SM INPUTS

4.1.1 EXTERNAL INPUTS

BRST BuRST signal from the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

PKT PacKeT signal from the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

4.1.2 INTERNAL INPUTS

<NXTST6> State 6 signal from the Connect Control SM: This signal is active when the Connect Control SM is in the {REQCON} state. This signal indicates the reception of an I-Field' from the HIPPI channel.

<NXTST25> State 25 signal from the Connect Control SM: This signal is active when the Connect Control SM is in the {CONNECTED} state. This signal allows the Data/FIFO SM to process Packet and Burst delimited data from the HIPPI channel.

4.2 HOST DATA/FIFO SM INTERNAL STATES

The defined states of the Data/FIFO SM are as follows:

{DISCON0-2} The DISCONnected 0 through DISCONnected 2 states are repetitively sequenced if the "DISC" input decode is true. This sequence is entered at {DISCON0} if the Mode 0 Reset is commanded via the MSEL0-2 inputs. While in this Sequence, the Idle/Disabled status word, the flow status word 1, and the flow status word 2 are presented in sequence on the data outputs of the Destination device. In addition to the standard transitions, this state sequence is exited to the {HSEQER} state if the "GLRC" or "DXFR" decodes are true, to the {IFIELD} state if the "HIFL" decode is true, or to the {IDLE} state if the "IDLG" decode is true.

{IFIELD} The I-FIELD state' is entered from the {DISCON0-2} state sequence if the "HIFL" decode is true. This state persists if the "HIFL" decode remains true. In addition to the standard transitions, this state is exited to {HSEQER} if the "GLRC" or "DXFR" decodes are true or to the {ILLINPT} state if the "IDLG" decode is true. The normal functional exit is the standard "DISC" to {DISCON0}. In this state the received I-Field from the HIPPI channel is presented on the data outputs of the Destination device.

{IDLE} The IDLE state is entered from the {DISCON0-2} state sequence, the {INTRPKT} state or the {ENDBPKT} state if the "IDLG" decode is true. In addition to the standard transitions, this state is exited to the {HSEQER} state if the "DXFR" decode is true, to the {ILLINPT} if the "HIFL" decode is true, and to the {BGNPKT} state if the "GLRC" decode is true. In this pre- and inter-packet state the general op status word is presented on the data outputs of the Destination device.

{BGNPKT} The BeGiN PacKeT state is entered from the {IDLE} state, the {INTRPKT} state or the {ENDBPKT} state if the "GLRC" decode is true. In addition to the standard transitions, this state is exited to the {HSEQER} if the "IDLG" decode is true, to the {ILLINPT} state if the "HIFL" decode is true, to the {PKTNBST} state if the "GLRC" decode is true, and to the {DTATRNSF} state if the "DXFR" decode is true. In this state the general op status word is presented on the data outputs of the Destination device.

{PKTNBST} The PacKeT No BurST state is entered from the {BGNPKT} state if the "GLRC" decode is true. This state persists if the "GLRC" decode remains true. In addition to the standard transitions, this state is exited to the {HSEQER} state if the "IDLG" decode is true, to the {ILLINPT} state if the "HIFL" decode is true, and to the {DTATRNSF} state if the "DXFR" decode is true. In this state the general op status word is presented on the data outputs of the Destination device.

{DTATRNSF} The DaTA TRaNSFer state is entered from the {BGNPKT} state, the {PKTNBST} state , or the {IBSTGP} state if the "DXFR" decode is true. this state persists if the "DXFR" decode remains true. In this state Burst data is received and presented to the data outputs of the Destination device. In addition to the standard transitions, this state is exited to the {HSEQER} state if the "IDLG" decode is true, to the {ILLINPT} state if the "HIFL" decode is true, or to the {LLRCCH} state if the "GLRC" decode is true.

{LLRCCH} The LLRC CHAracter state is entered from the {DTATRNSF} state if the "GLRC" decode is true. In this state the received LLRC character from the HIPPI channel is presented on the data outputs of the Destination device. During this state, the internally calculated LLRC character is compared to the received character and the result of this comparison is presented one clock cycle

Figure 7. S2021 Data/FIFO SM Input Decode Alphabet

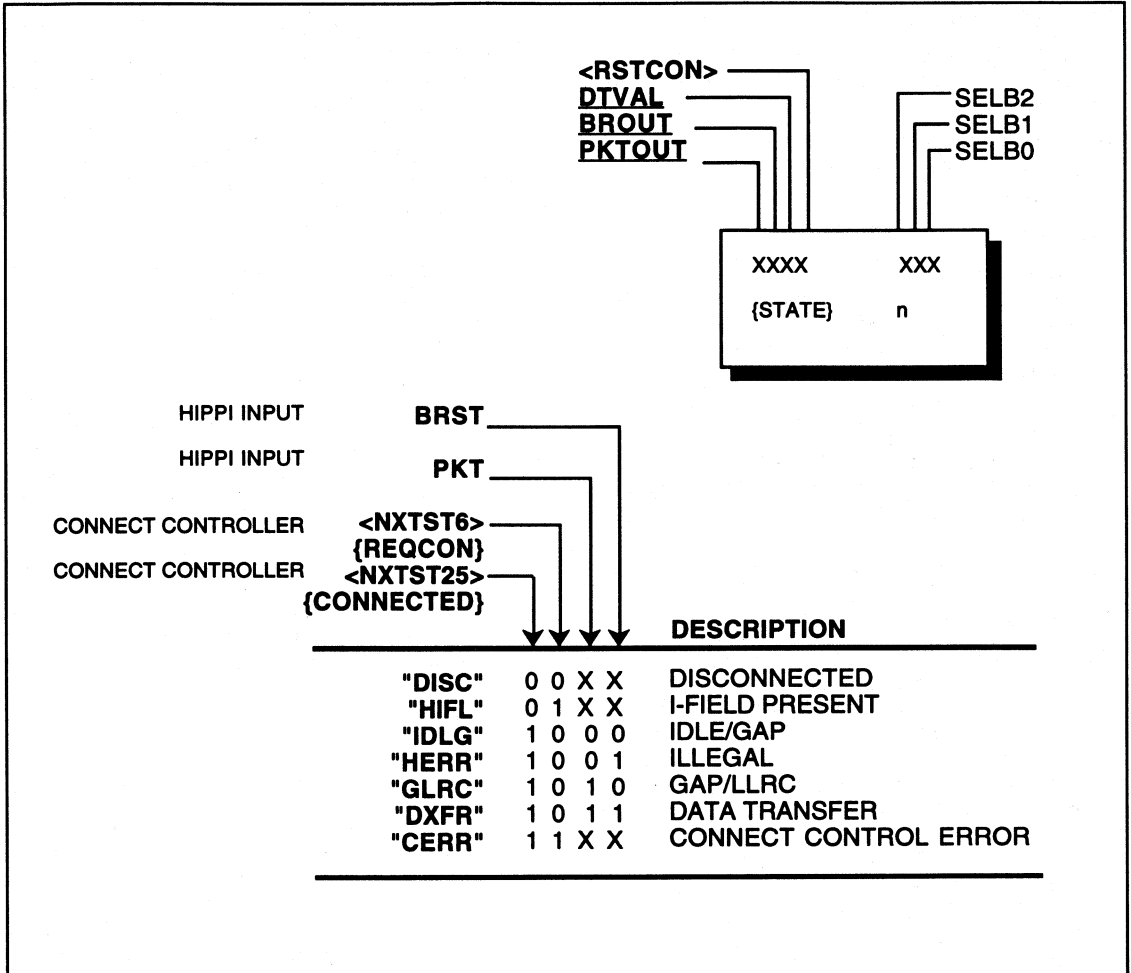
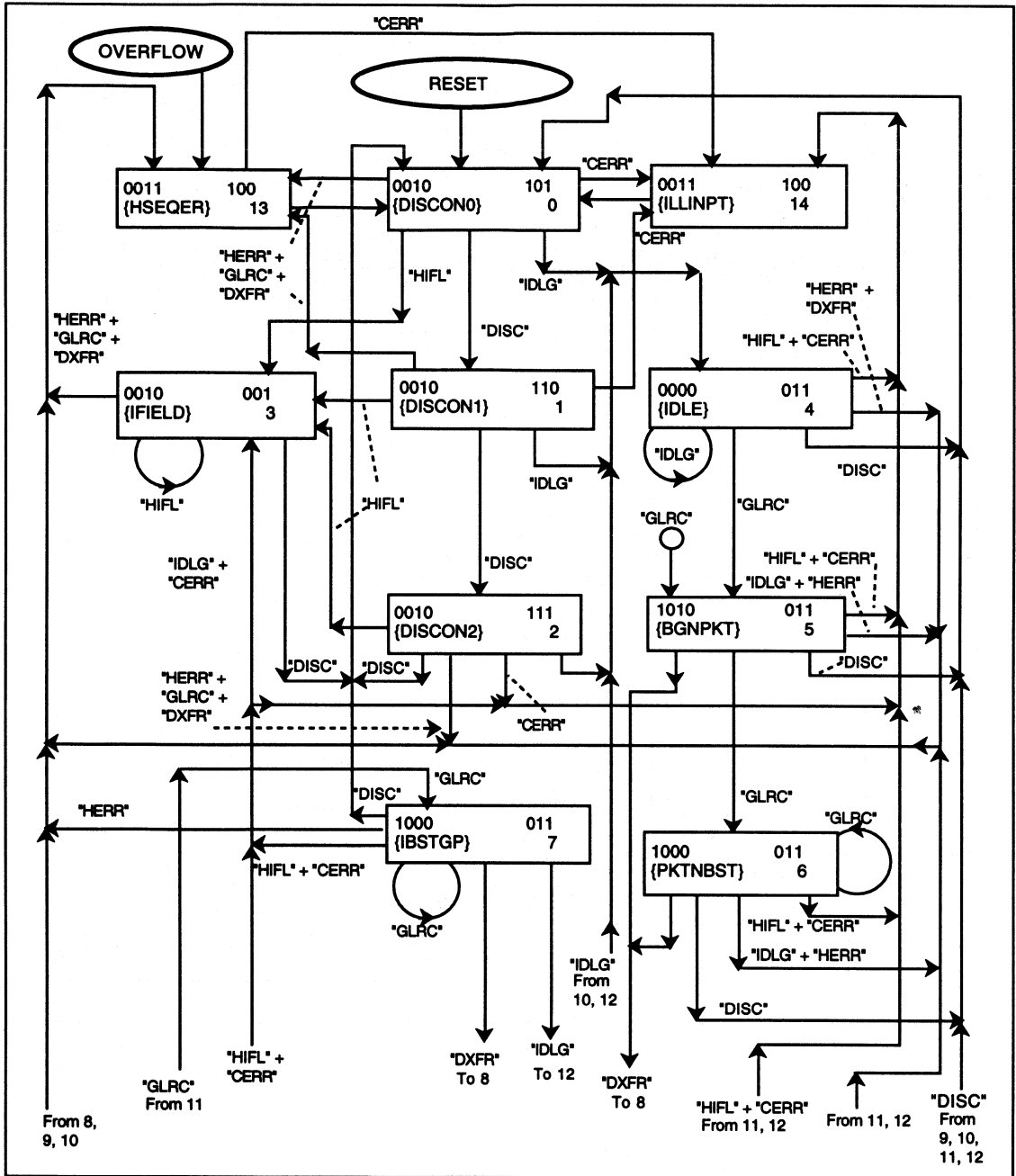
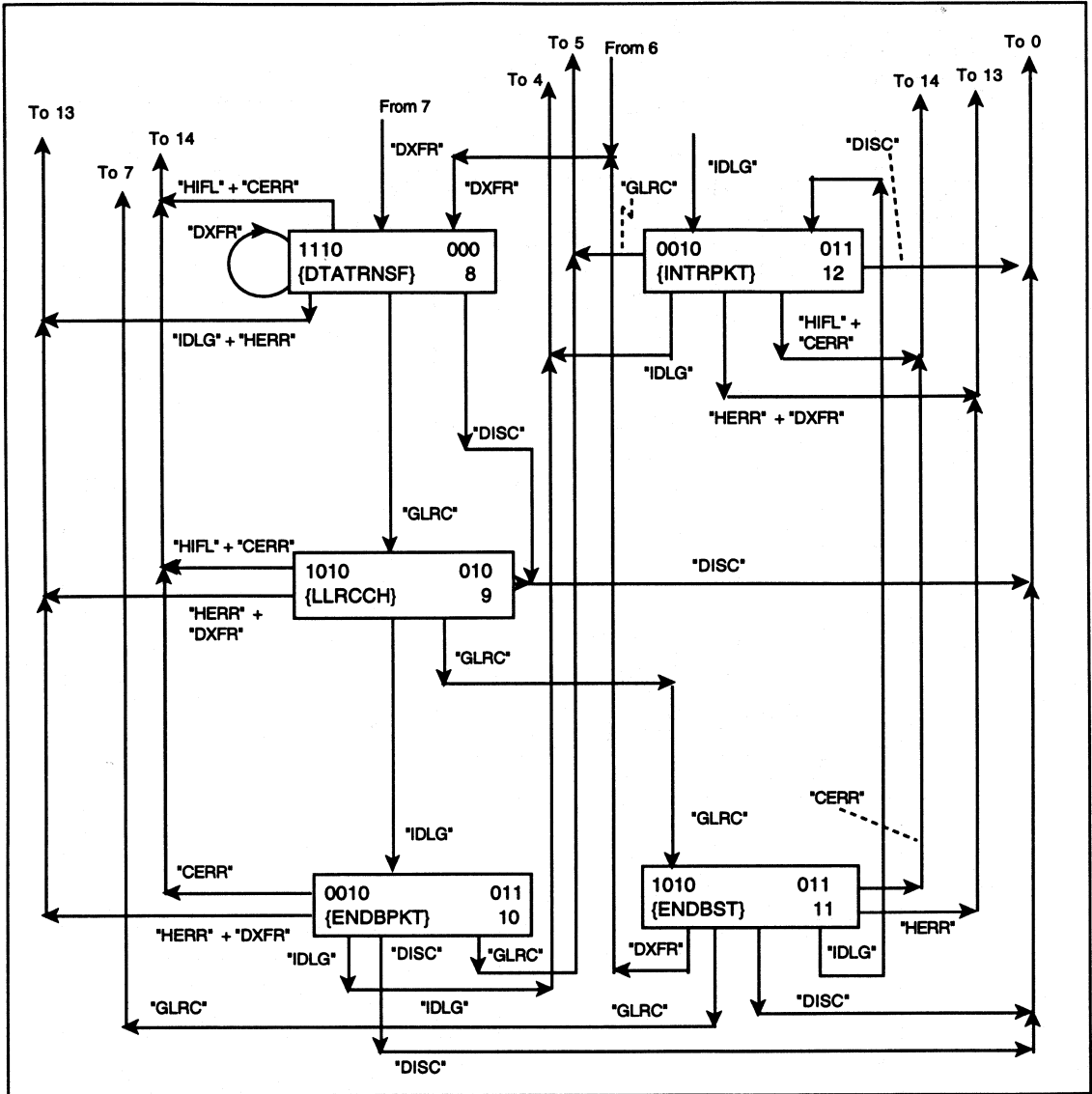


Figure 8. S2021 Host Data/FIFO SM State Transition Diagram



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Figure 8. S2021 Host Data/FIFO SM State Transition Diagram (continued)



later on the **RLLER** output of the Destination device. In addition to the standard transitions, this state is exited to the {HSEQER} state if the "DXFR" decode is true, to the {ILLINPT} state if the "HIFL" decode is true, to the {ENDBPKT} state if the

"IDLG" decode is true, or to the {ENDBST} state if the "GLRC" decode is true.

{ENDBST} The END BurST state is entered from the {LLRCCH} state if the "GLRC" decode is true. In this state the general op status word is presented on the data outputs of the Destination device. In addition to the standard transitions, this state is exited to the {ILLINPT} state if the "HIFL" decode is true, to the {DTATNSF} state if the "DXFR" decode is true, to the {IBSTGP} state if the "GLRC" decode is true, or to the {INTRPKT} state if the "IDLG" state is true.

{IBSTGP} The Inter BurST GaP state is entered from the {ENDBST} state if the "GLRC" decode is true. This state persists if the "GLRC" decode remains true. In this state the general op status word is presented on the data outputs of the Destination device. In addition to the standard transitions, this state is exited to the {ILLINPT} state if the "HIFL" decode is true, to the {DTATNSF} state if the "DXFR" decode is true, or to the {INTRPKT} state if the "IDLG" decode is true.

{INTRPKT} The INTeR PaCKeT state is entered from the {IBSTGP} state or from the {ENDBST} state if the "IDLG" decode is true. In this state the general op status word is presented on the data outputs of the Destination device. In addition to the standard transitions, this state is exited to the {HSEQER} state if the "DXFR" decode is true, to the {ILLINPT} state if the "HIFL" decode is true, to the {BGNPKT} state if the "GLRC" decode is true, or to the {IDLE} state if the "IDLG" decode is true.

{HSEQER} The HIPPI SEQUENCE ERror state is entered unconditionally if the OVERFLOW condition occurs (Burst received when Burst and Ready counters are equal). The {HSEQER} is also entered from all states except {ILLINPUT}. For specific states other decodes incorrect that state will also force the {HSEQER} state. In this state the Sequence Error status word is presented to the data outputs of the Destination device. During this state the <RSTCON> signal is generated to force the reset of the Connect Control SM and abandon the compromised HIPPI Connection. This state is exited to the {DISCON0} state unconditionally on the next clock cycle.

{ILLINPT} The ILLegal INPuT signals state is entered from all other states except the {HSEQER} state if the "CERR" decode is true. For specific states other decodes incorrect that state will also force the {ILLINPT} state. In this state the Sequence Error status word is presented to the data outputs of the Destination device. During this state the <RSTCON> signal is generated to force the reset of the Connect Control SM and abandon the compromised HIPPI Connection. This state is exited to the {DISCON0} state unconditionally on the next clock cycle.

4.3 HOST DATA/FIFO SM EXTERNAL OUTPUTS

PKOUT PaCKeT OUT signal to the Destination Host system. A '1' on this signal indicates the detection and synchronization of an asserted PKT signal from the HIPPI channel. A '0' indicates the end of a HIPPI Packet.

BROUT BuRst OUT signal to the Destination Host system. A '1' on this signal indicates the detection and synchronization of an asserted **BRST** signal from the HIPPI channel. A '0' indicates a deasserted **BRST** signal.

DTVAL DaTa VALid signal to the Destination Host system. This signal is at a '1' when new data or status is available on the data outputs of the Destination device. This signal is at '0' in the {IDLE}, {IBSTGP}, and {PKTNBST} states.

SELB0-2 SELEct Bus 0, 1, 2 signals' to the Destination Host system. These signals are intended to be the primary addressing delimiters of the various status and data words presented at the data outputs of the Destination device. The functions of these signals are described in the S2020/S2021 Preliminary Device Specification.

Figure A-1. Source Flow Diagram

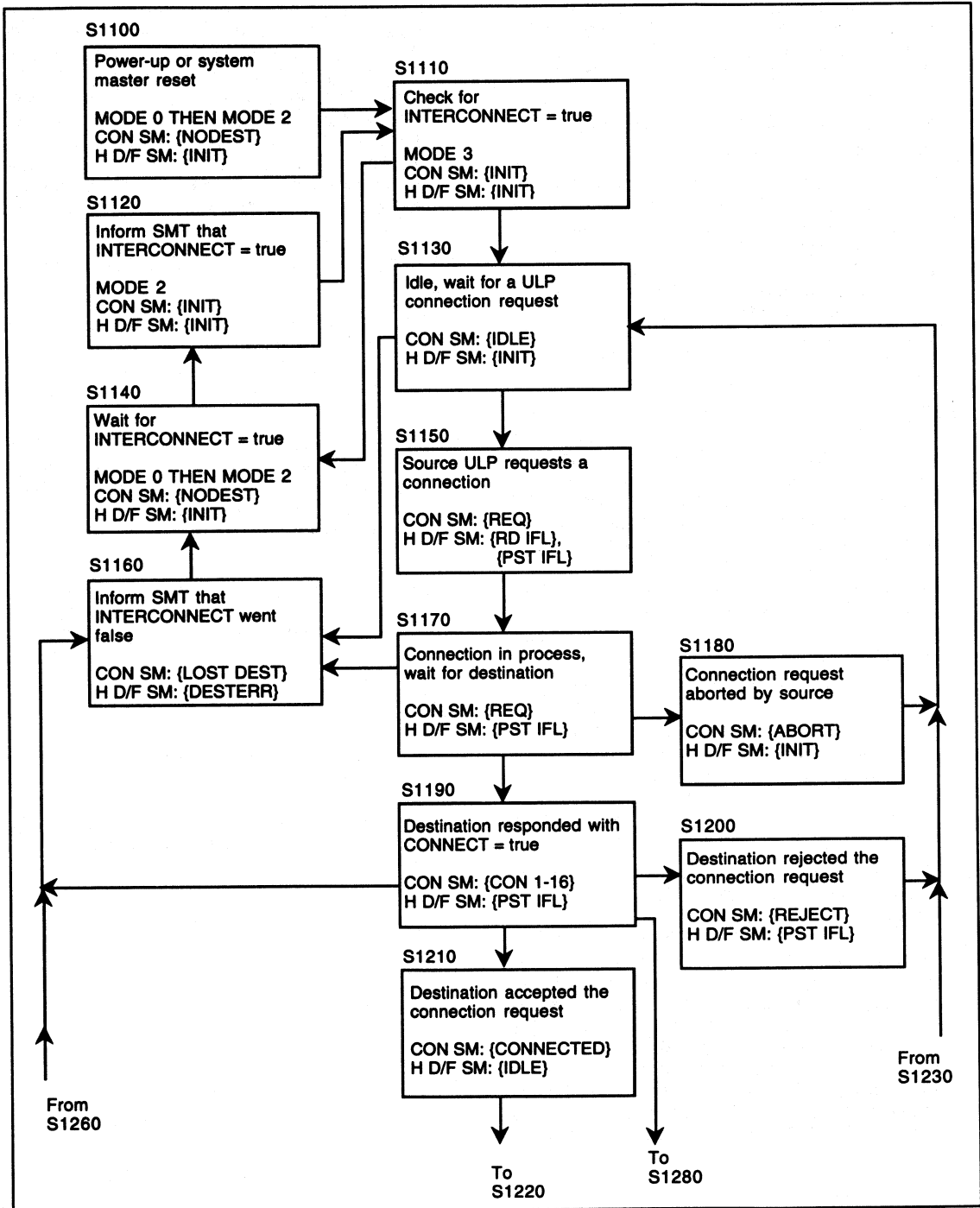


Figure A-1. Source Flow Diagram (continued)

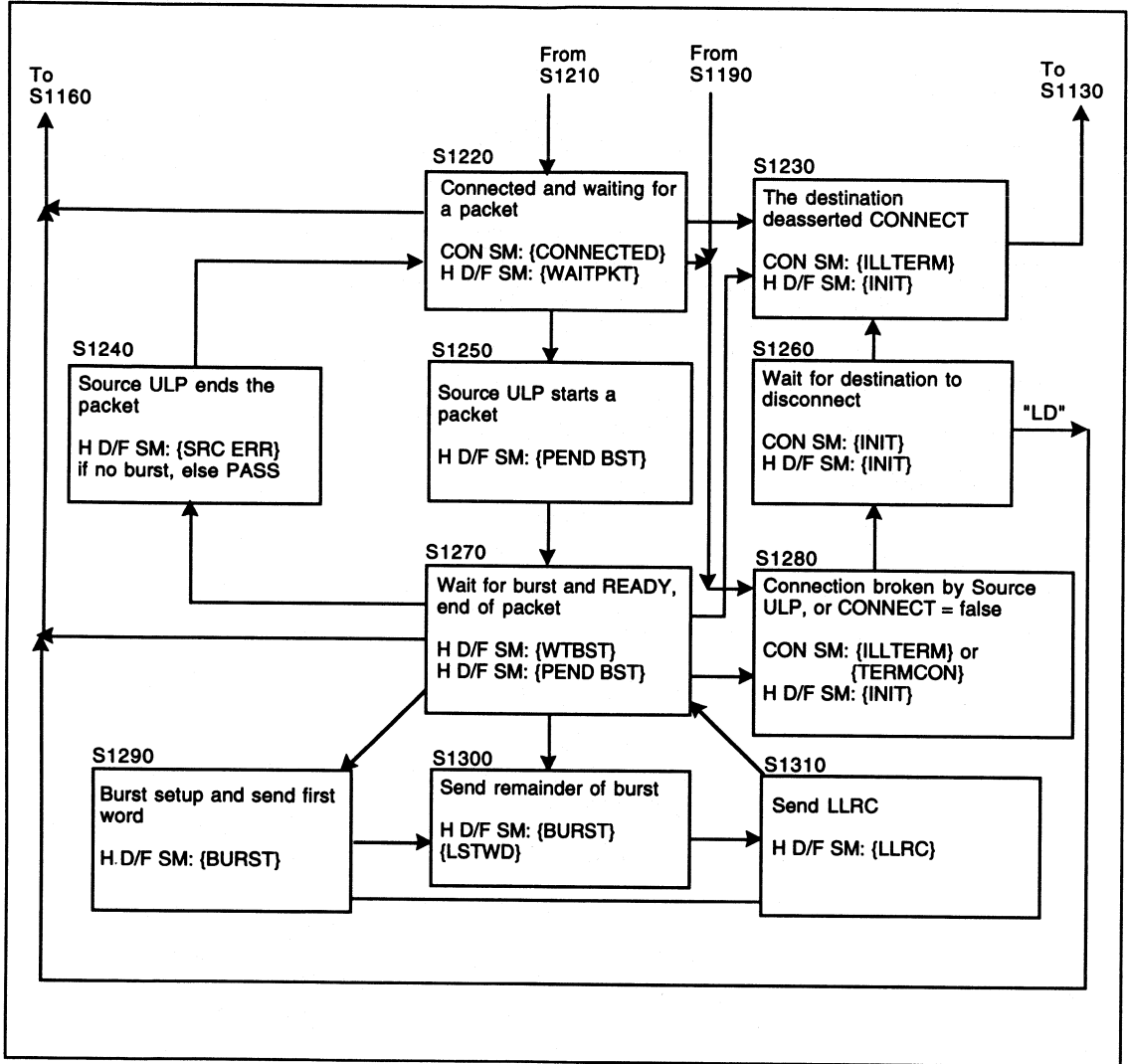


Figure A-2. Destination Flow Diagram

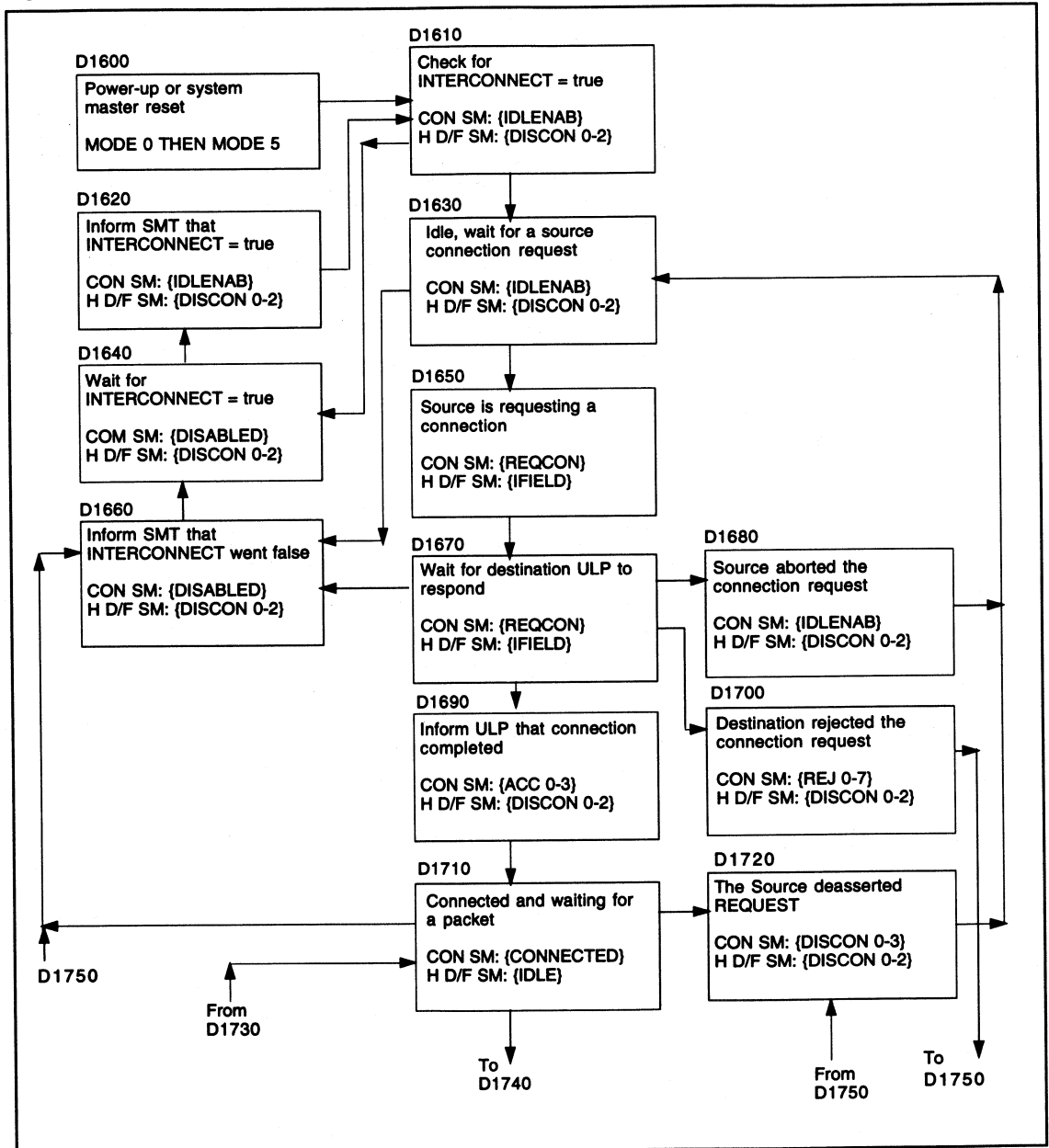
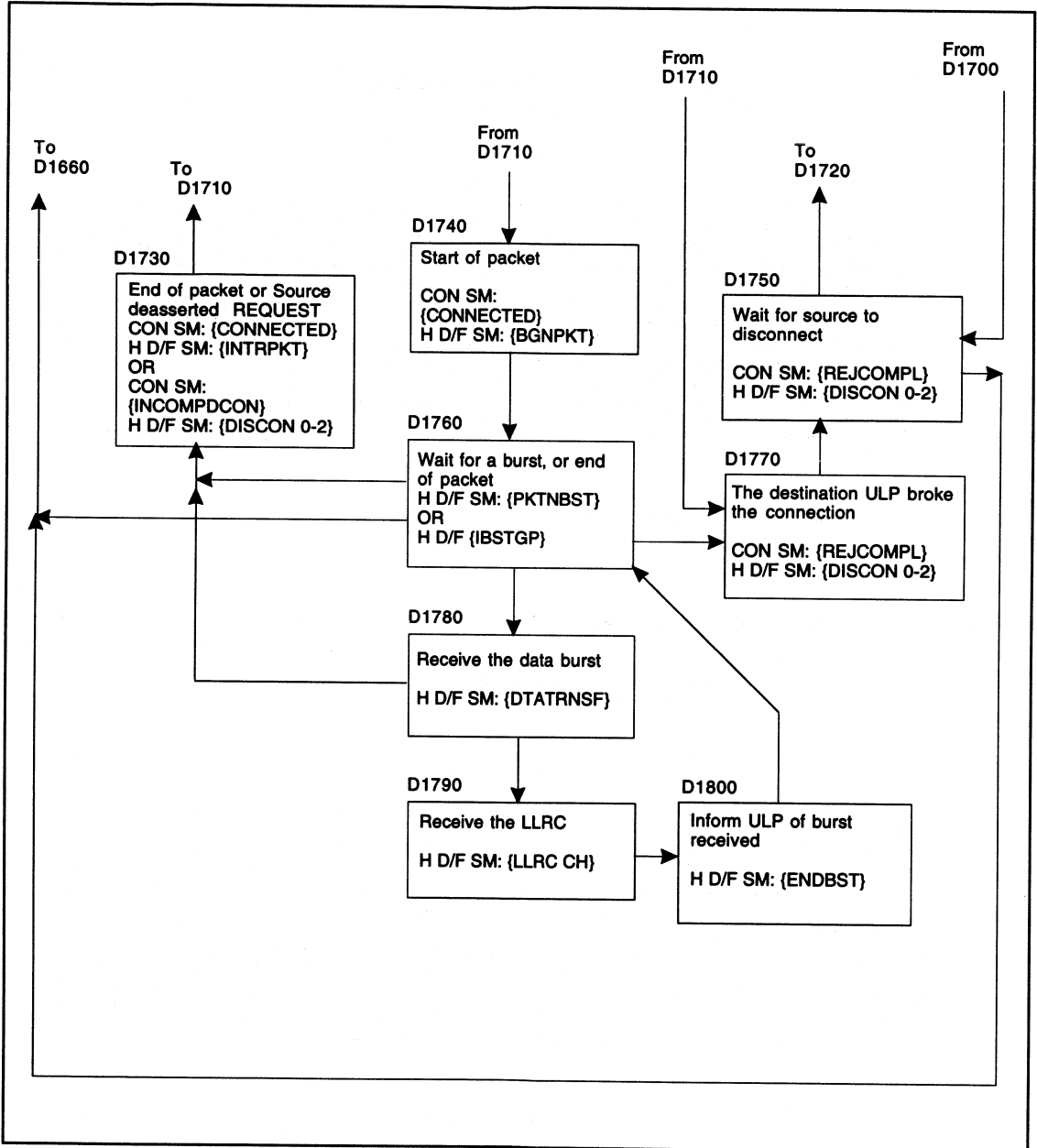


Figure A-2. Destination Flow Diagram (continued)



SELECT = 0: HIPPI CHANNEL DATA

DOUT0-31

3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	

BYTE 0								BYTE 1								BYTE 2								BYTE 3																	
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0								
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	0	0								

HOST DATA BUS FORMAT IN FUNCTIONAL MODE

SELECT = 1: HIPPI I-FIELD

DOUT0-31

3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0

BYTE 0								BYTE 1								BYTE 2								BYTE 3																	
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0								
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	0	0								

HOST DATA BUS FORMAT IN FUNCTIONAL MODE

SELECT = 2: HIPPI BURST LLRC WORD

DOUT0-31

3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	

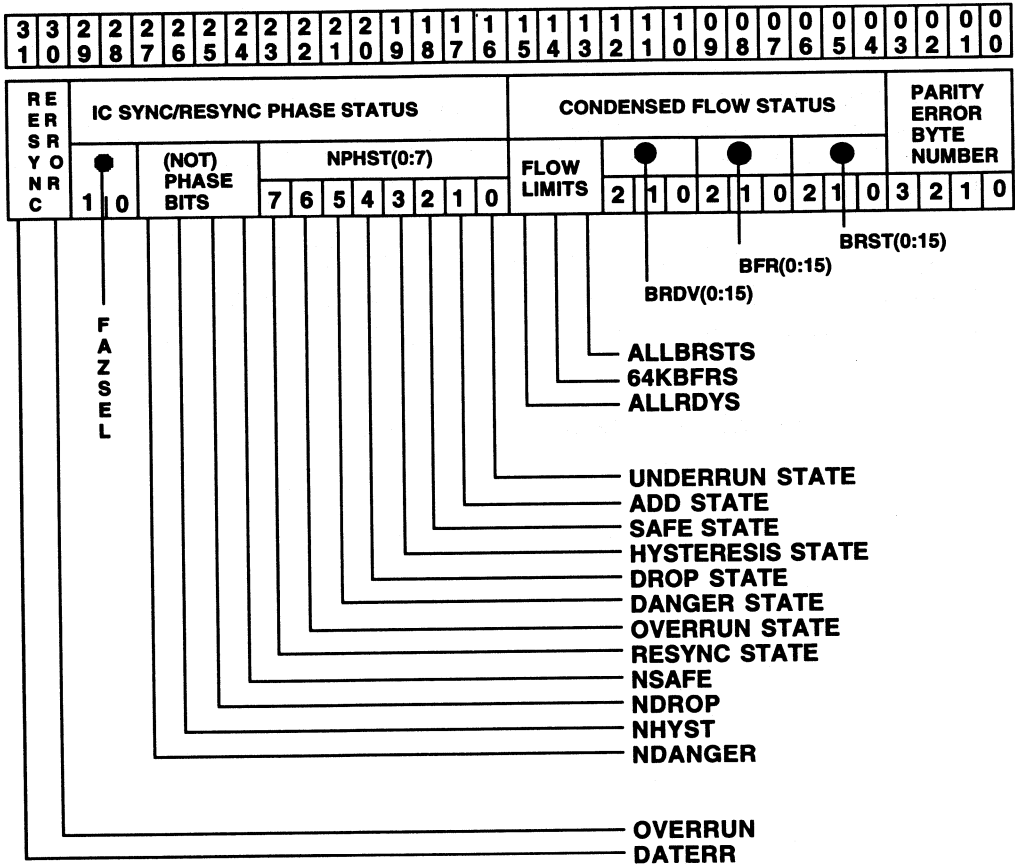
BYTE 0								BYTE 1								BYTE 2								BYTE 3									
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		

5

HOST DATA BUS FORMAT IN FUNCTIONAL MODE

SELECT 3: GENERAL OPERATIONAL STATUS

DOUT0-31



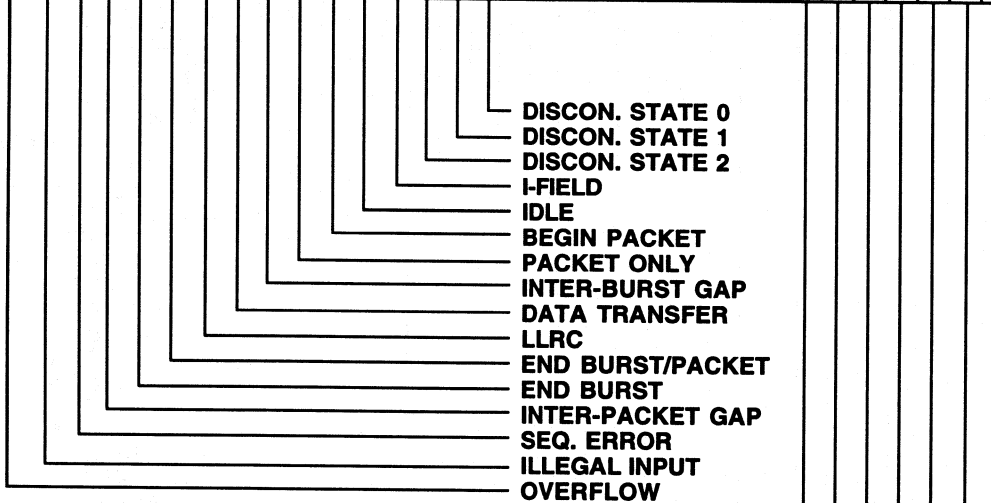
HOST DATA BUS FORMAT IN FUNCTIONAL MODE

SELECT 4: SEQUENCE ERROR STATUS

DOUT0-31

3	3	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	

E R R	LAST DATA BUS CONTROLLER STATE														LLRC BURST COUNTER							X	LAST CONTROLLER INPUTS						
	NDBUST(0:14)														WORD(0:7)							'0'	NDBUSC(0:6)						
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2		1	0	6	5	4	3	2



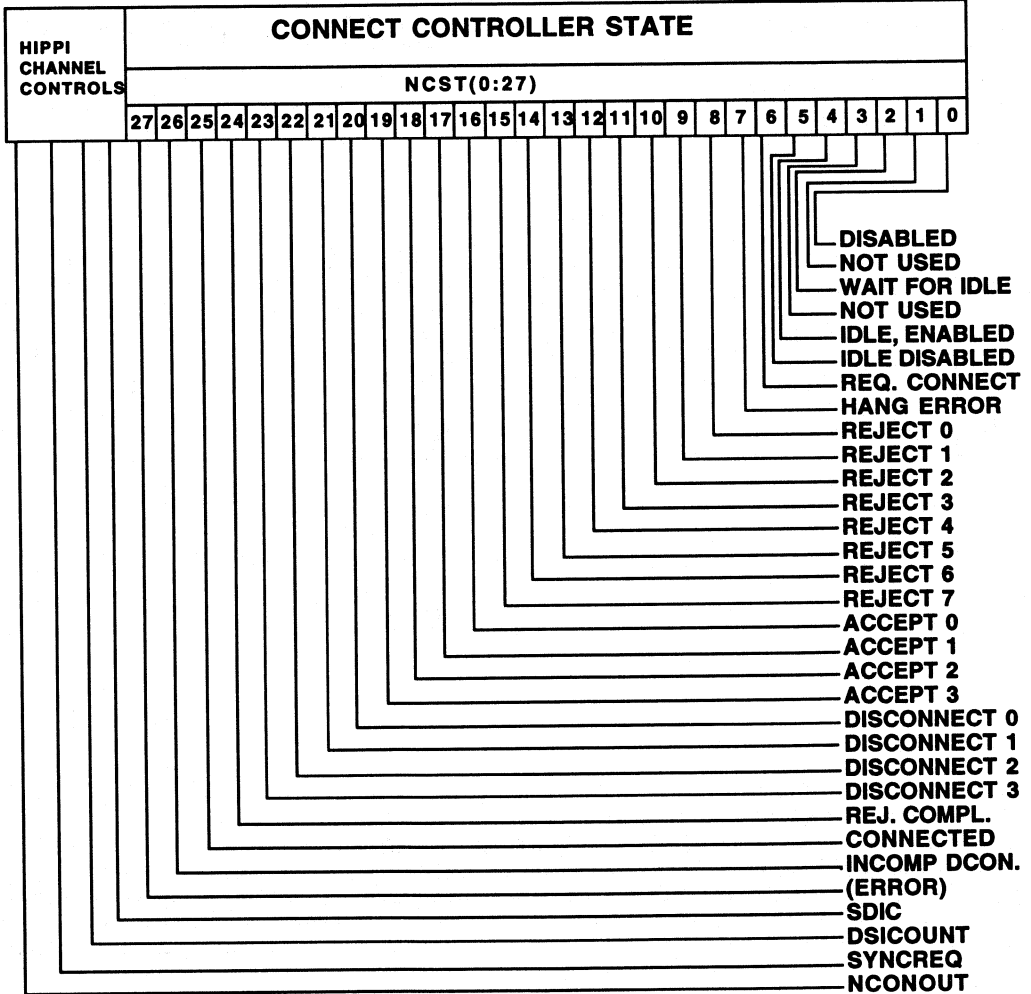
- "CERR" - ERROR: CONNECTED, I-FIELD
- "DXFR" - DATA: CONNECTED, PACKET, BURST
- "LLRC" - GAP/LLRC: CONNECTED, PACKET, NO BURST
- "HERR" - ERROR: CONNECTED, NO PACKET, BURST
- "IDLG" - IDLE: CONNECTED, NO PACKET, NO BURST
- "HIFL" - I-FIELD: CONNECT REQUEST
- "DISC" - DISCONNECTED

HOST DATA BUS FORMAT IN FUNCTIONAL MODE

SELECT 5: IDLE/DISABLED STATUS

DOUT0-31

3	3	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	



HOST DATA BUS FORMAT IN FUNCTIONAL MODE

SELECT = 6: FLOW STATUS WORD 1

3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	

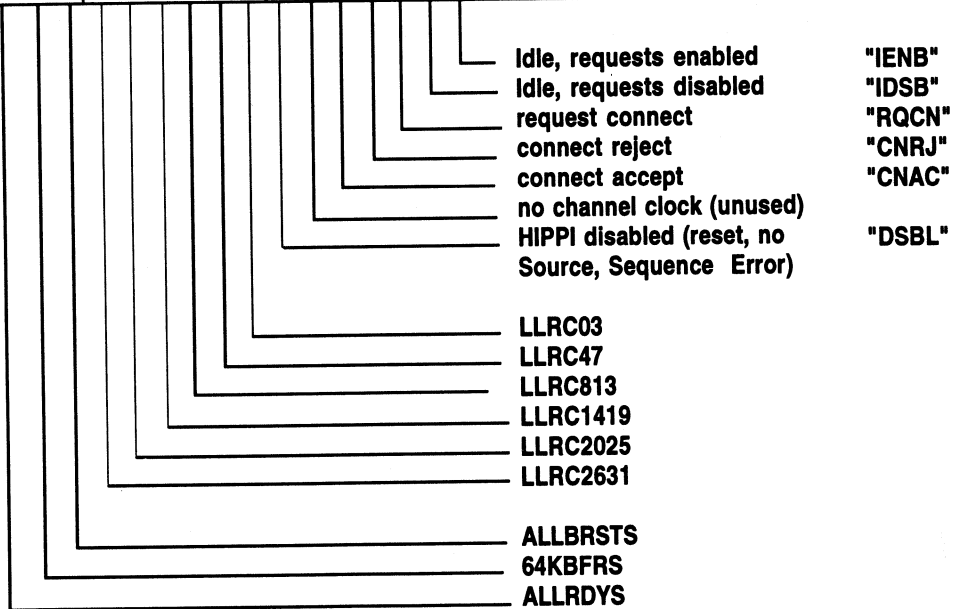
READY COUNTER																BURST COUNTER															
RDY(0:15)																BRST(0:15)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SELECT 7: FLOW STATUS WORD 2

DOUT0-31

3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	

Flow Controller Limits	LLRC CHECKER PARTIAL TERMS	Connect Controller State Inputs						BUFFER COUNTER														
	(FOR TESTABILITY)	NEPCON(0:6)						BFR(0:15)														
		6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2



HOST DATA BUS FORMAT IN FUNCTIONAL MODE

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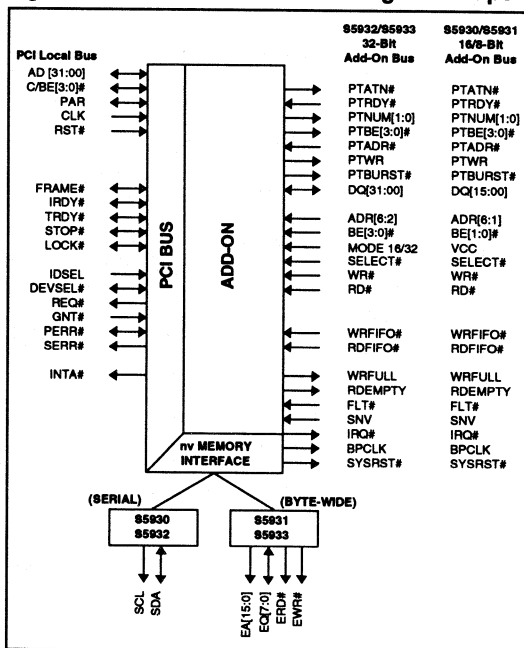
- Low Cost
- Supports Full PCI Bus Bandwidth
- Single-chip PCI bus master/slave interface for add-on products
- Two 32-byte FIFOs (one for each data direction)
- 32-bit (S5932, S5933), 8- or 16-bit (S5930, S5931) add-on data bus width
- Four configurable base address regions (memory space or I/O)
- Data bus size matching and lane steering for 8 and 16-bit add-on data buses (master and slave)
- Supports PCI Burst transfers
- Dual address counters (one for writes, one for reads) for PCI port
- Throttle control on PCI port
- Two sets of mailbox registers with empty/full status and interrupts (16 bytes/set)
- Interrupt on PCI transfer complete and/or mailbox status
- Synchronous or asynchronous add-on interface
- Supports external byte-wide nvRAM (S5931, S5933) or serial nvRAM (S5930, S5931, S5932, S5933)
- Allows expansion BIOS ROM implementation within nvRAM
- Pass-thru interface permits PCI Bus access to add-on resources
- FIFO interface allows PCI bus mastering
- 120, 144 and 160 PQFP package

APPLICATIONS

- RAID Systems—File Servers/Work Stations
- Communication Boards—File Servers/Work Stations
- Image Processing—Video Conferencing, Editing, Multimedia, Games, Image Recognition
- Instrumentation, Custom Applications
- Data Acquisition Systems

GENERAL DESCRIPTION

AMCC's PCI Local Bus Master/Slave Controller provides a high performance single-chip interface between the PCI bus and custom add-on boards. Address decoding, bus mastering, burst transfer support, and all elements necessary to perform efficient and timely data transfers are provided within the device. A bidirectional, 32-bit wide FIFO is integrated which facilitates the system-to-system synchronization and data transfers between the local bus and the add-on application. A custom expansion BIOS can be implemented to perform any pre-boot initialization required for the add-on application. The external ROM/EPROM/nvRAM can be either in x8 or serial form and provides a convenient method to configure the S593X for a specific add-on application.

Figure 1. PCI Interface Controller Signal Groups

APPLICATIONS

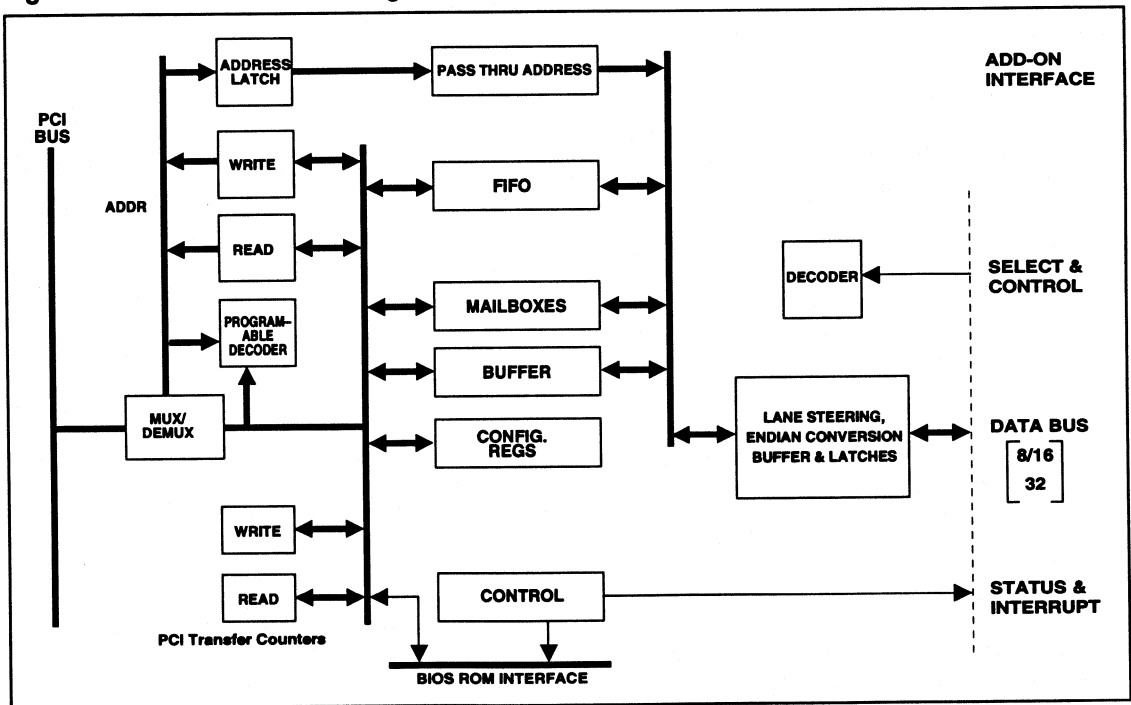
The S593X is designed to permit direct connection between the PCI local bus and a variety of general purpose microprocessor-style buses. Bus master transfers can be performed on the PCI bus while device accesses occur on the add-on interface. PCI transfer addresses, transfer counts, mailbox registers, and control/status information are provided on the PCI interface as I/O or memory mapped locations on the PCI bus.

The S593X contains three signal groupings: the PCI bus interface, the EPROM interface, and the add-on general purpose bus interface signals.

Many of the high-performance, complex peripheral functions in today's PCs require a dedicated, embedded microprocessor. Often, the functions desired and the local memory requirements necessary for these add-on products prohibit integration into a single device. The benefits from the embedded microprocessor approach come from the flexibility, time to market, and function complexity which only software techniques can achieve.

AMCC's PCI controllers provide a high performance, highly integrated, easy-to-use method to interface an embedded microprocessor subsystem to the PCI bus.

Figure 2. S5930–S5933 Block Diagram



DEVELOPER'S KIT INCLUDES

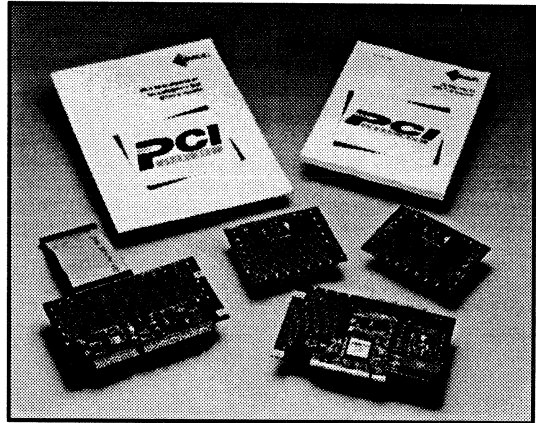
- PCI compliant circuit board with an S5933Q controller, two 22V10 PLDs, one byte-wide FLASH EPROM and one serial NVRAM
- Two breadboard "daughter cards" with connectors
- One ISA "loopback" card with ribbon cable
- Developer's Kit User's Guide including PLD equations, board schematics and layout
- S5930-S5933 PCI Controllers Data book
- S5930-S5933 Quick Reference Guide

DESCRIPTION

The S5933DK PCI Controllers Developer's Kit provides a proven reference platform for use in prototype applications. The kit has a modular design that allows hardware "breadboarding" as well as general evaluation of the S5933Q PCI Matchmaker Controllers. Diagnostic and development utility software is included to reduce time-to-market for new applications.

The S5933 demonstration board consists of a PCI compliant edge connector and an S5933Q device packaged in a 160-pin plastic quad flat pack (PQFP). In addition, two pre-programmed 22V10 Programmable Logic Devices (PLD's) are provided for device control. Both serial and byte-wide FLASH EPROMs are included and may be programmed by the user.

Via on-board connectors, the S5933 board can be interfaced to either of two breadboard daughter cards that are included in the kit. Each daughter card has a 22V10 PLD socket along with 3 x 4 inches of uncommitted wire wrap area and 2 x 3 inches of customizable wire wrap area.



Alternatively, the evaluation board can be interfaced with the ISA loopback card provided. The ISA card consists of a standard edge connector and a ribbon cable which connects to the S5933 evaluation board.

The ISA card allows the user to "emulate" an add-on processor using either the host system or a second PC. The loopback feature provides direct access to the S5933's add-on bus, enabling the user to pass commands and data through the S5933 on to the PCI bus. The uncommitted breadboard area provided on the ISA card allows for customized functionality.

Software developers' tools included with the kit allow the user to exercise various configurations and controller registers using a "high level" DOS interface: AMCCDIAG, a diagnostic program which also verifies the integrity of the S5933 data. The NVBUILD program assists in the in-system programming of the external nonvolatile memory to implement application-specific configurations.

A user's manual and full design documentation complete the kit.

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FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLL for clock generation and clock recovery
- Supports 139.264 Mbit/s (E4), 155.52 Mbit/s (OC-3), and 622.08 Mbit/s (OC-12) transmission rates
- Supports 139.264 Mbit/s and 155.52 Mbit/s Code Mark Inversion (CMI) interfaces
- Selectable reference frequencies of 19.44, 38.88, 51.84, and 77.76 MHz (OC-3/12) and 17.408, 34.816, 46.421, and 69.632 MHz (E4)
- Interface to both ECL and TTL logic
- 8-bit TTL/CMOS datapath
- Bypass mode for off-chip clocking
- Local and line loopback mode
- Lock detect
- Low jitter ECL interface
- Low power
- 80 PQFP or 68 LDCC package

APPLICATIONS

- SONET/SDH or E4-based transmission systems
- SONET/SDH or E4 modules
- SONET/SDH or E4 test equipment
- ATM over SONET
- Section repeaters
- Add drop multiplexors
- Broadband cross-connects
- Fiber optic terminators
- Fiber optic test equipment

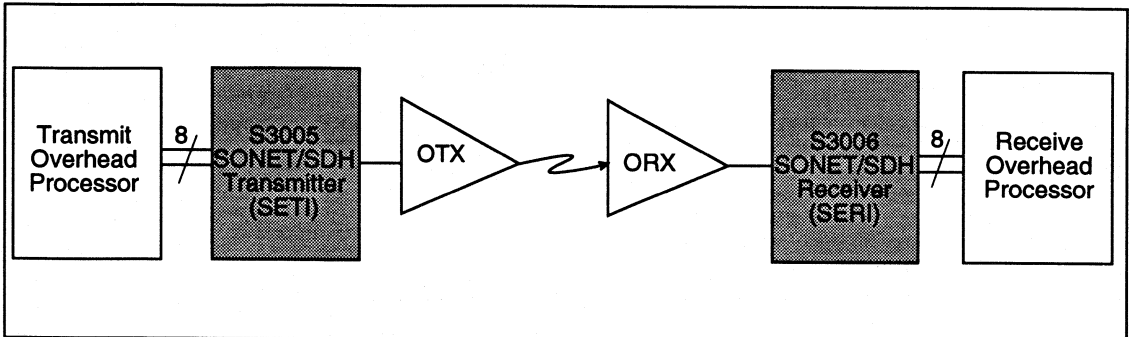
GENERAL DESCRIPTION

The S3005/S3006 Synchronous Electrical Transmit Interface, SETI, and Synchronous Electrical Receive Interface, SERI, SONET/SDH and E4 transmitter and receiver chips are the first fully integrated serialization/deserialization interface devices covering E4 (139.264 Mbit/s), SONET OC-3 (155.52 Mbit/s) and SONET OC-12 (622.08 Mbit/s). With architecture developed by PMC-Sierra, the chipset performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH and E4 transmissions standards. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3005 SETI transmitter chip allowing the use of a slower external transmit clock reference. Clock recovery is performed on the S3006 SERI receiver chip by synchronizing its on-chip VCO directly to the incoming data stream. The S3006 also performs SONET/SDH frame detection. The chipset can be used with 19.44, 38.88, 51.84, and 77.76 MHz reference clocks when operated in the SONET/SDH OC-3 or OC-12 modes. In the E4 mode the chipset can be operated with 17.408, 34.816, and 69.632 MHz reference clocks in support of existing system clocking schemes. On-chip code-mark-inversion (CMI) encoding and decoding is provided for 139.264 Mbit/s and 155.52 Mbit/s interfaces. If desired, both clock generation and recovery can be bypassed, allowing the use of externally generated and recovered clocks.

The very low jitter ECL interface guarantees compliance with the bit-error rate requirements of the Bellcore, ANSI, and ITU-T standards. The S3005/S3006 SETI and SERI chipset is packaged in a 50 mil pitch, 68-pin LDCC or 25 mil pitch, 80 PQFP package, offering designers a small package outline.

Figure 1. Link Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Figure 2. SONET Structure

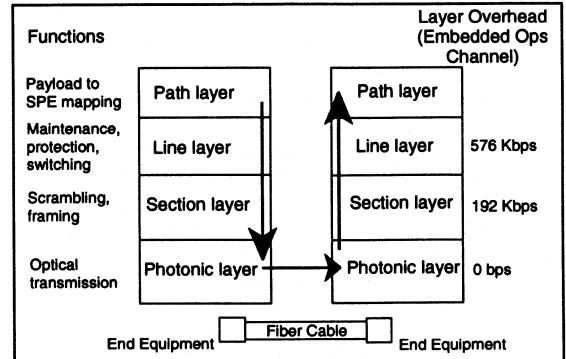


Table 1. SONET Signal Hierarchy

Elec.	ITU-T	Optical	Data Rate (Mbit/s)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-9		OC-9	466.56
STS-12	STM-4	OC-12	622.08
STS-18		OC-18	933.12
STS-24		OC-24	1244.16
STS-36		OC-36	1866.24
STS-48	STM-16	OC-48	2488.32

Data Rates and Signal Hierarchy

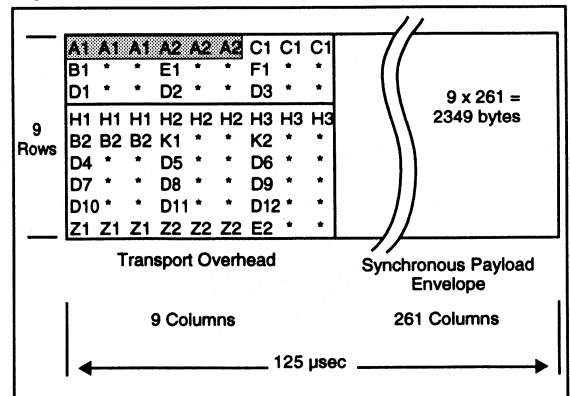
Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3005/S3006 chipset supports OC-3 rates (155.52 Mbit/s) and OC-12 (622.08 Mbit/s) rates.

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-3 consists of nine transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 9 overhead and 261 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3)

For more details on SONET operations, refer to the ANSI SONET standard document.

Figure 3. STS-3/OC-3 Frame Format



S3005/S3006 OVERVIEW

The S3005 SETI and S3006 SERI implement SONET/SDH serialization/deserialization, transmission, and frame detection/recovery functions. The block diagrams in Figures 4 and 5 show basic operation of both chips. These chips can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface (S3005) and the serial receive interface (S3006). The chipset handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation and recovery, and system timing, which includes management of the datastream, framing, and clock distribution throughout the front end.

Operation of the S3005/S3006 chips is straightforward. The sequence of operations is as follows:

Transmitter

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. CMI encoding (optional)
4. Serial output

Receiver

1. Clock and data recovery from serial input
2. CMI decoding (optional)
3. Frame detection
4. Serial-to-parallel conversion
5. 8-bit parallel output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 10 through 18. On-chip clock generation can be bypassed and an externally generated clock used in its place, providing an additional measure of design flexibility.

A lock detect feature is provided on both chips.

S3005 TRANSMITTER ARCHITECTURE/FUNCTIONAL DESIGN

The S3005 SETI transmitter chip performs the serializing stage in the processing of a transmit SONET STS-12, STS-3, or ITU-T E4 bit serial data stream. It converts the byte serial data stream to bit serial format at 622.08, 155.52, or 139.264 Mbit/s depending on the control settings and reference frequency provided by the user. A Coded-Mark-Inversion (CMI) is available for use during 155.52 Mbit/s STS-3 (electrical) and 139.264 Mbit/s E4 operational modes. (See Other Operating Modes.)

A high-frequency bit clock can be generated from a variety of lower frequency references by using the

Suggested Interface Devices

PMC PM5345	SUNI	Saturn User Network Interface
PMC PM5355	SUNI-622	Saturn User Network Interface
IGT WAC-013-A		SONET LAN ATM Processor
Fujitsu MB86683B	NTC	Network Termination Controller
PMC PM5301	SSTX	Section Terminating Transceiver
PMC PM5312	STTX	Transport Terminating Transceiver
AT&T ASTROTEC 1227/1230	650 Mbit/s	Fiber Optic Transmitter
Mitsubishi MF-622DF-T12-XXX	622 Mbit/s	Fiber Optic Transmitter
AT&T ASTROTEC 1310	650 Mbit/s	Fiber Optic Receiver
Mitsubishi MF-622DS-R1X-XXX	622 Mbit/s	Fiber Optic Receiver

Figure 4. SONET/SDH Transmitter

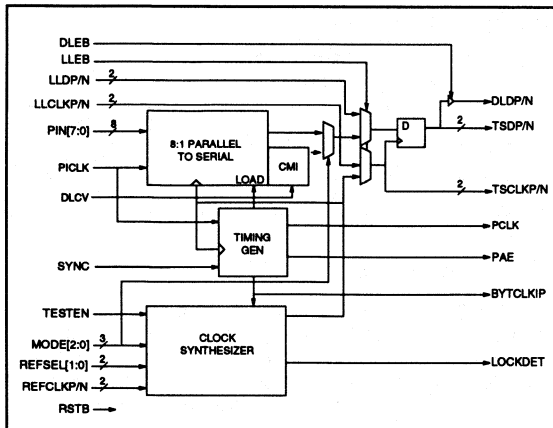
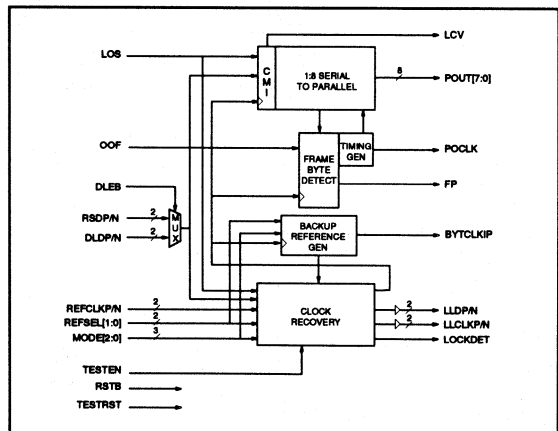


Figure 5. SONET/SDH Receiver



integral frequency synthesizer consisting of a phase-locked loop circuit with an adjustable divider in the loop. For applications that provide a high-frequency bit clock externally, the internal synthesizer may be bypassed. Reference frequencies of 19.44 MHz, 38.88 MHz, 51.84 MHz, or 77.76 MHz are selectable for SONET/SDH by the two reference select input pins. In E4 applications, these same pins can select the reference frequency from 17.408 MHz, 34.816 MHz, 46.421 MHz, or 69.632 MHz.

Loopback modes are provided for diagnostic loopback (transmitter to receiver), or line loopback (receiver to transmitter) when used with the compatible S3006. (See Other Operating Modes.)

The operating mode is selected by three mode programming inputs to be 622.08 Mbit/s, 155.52 Mbit/s, 155.52 Mbit/s with Coded-Mark-Inversion (CMI) encoding, or 139.264 Mbit/s with CMI encoding.

Clock Synthesizer

The Clock Synthesizer, shown in the block diagram in Figure 4, is a monolithic PLL that generates the serial output clock phase synchronized with the input reference clock (REFCLK). There are three selectable output clock frequencies that are synthesizable from any of four selectable reference frequencies for SONET/SDH operation.

The MODE[2:0] inputs select the output serial clock frequency to be 622.08 MHz for STS-12, 311.04 MHz for CMI-encoded STS-3, 155.52 MHz for STS-3, or 278.528 MHz for CMI-encoded E4. Their frequencies are selected as shown in Table 2.

Table 2. Clock Frequency Options

MODE[2:0]	OUTPUT CLOCK FREQUENCY	OPERATING MODE
100	622.08 MHz	STS-12
001	311.04 MHz	STS-3 CMI
010	155.52 MHz	STS-3
011	278.528 MHz	E4 CMI

The REFSEL[1:0] inputs in combination with the MODE[2:0] inputs select the ratio between the output clock frequency and the reference input frequency, as shown in Tables 3 and 4. This ratio is adjusted for each of the four modes so that the reference frequency selected by the REFSEL[1:0] is the same for all modes.

The REFCLK input must be generated from a differential ECL crystal oscillator which has a frequency accuracy of better than 20 ppm in order for the TSCLK frequency to have the same accuracy required for operation in a SONET system.

In order to meet the .01 UI SONET jitter specifications, the maximum reference clock jitter must be guaranteed over the 12KHz to 1MHz bandwidth. For details of reference clock jitter requirements, see Table 5.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCLK input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. The loop filter's corner frequency is optimized to minimize output phase jitter. The loop filter capacitor is included on the package.

Table 3. Reference Frequency Options

REF-SEL [1:0]	REFERENCE CLOCK FREQUENCY	OPERATING MODE
00	19.44 MHz	STS-12, STS-3, CMI
01	38.88 MHz	STS-12, STS-3, CMI
10	51.84 MHz	STS-12, STS-3, CMI
11	77.76 MHz	STS-12, STS-3, CMI

Table 4. E4CMI Reference Frequency Options

REF-SEL [1:0]	REFERENCE CLOCK FREQUENCY	OPERATING MODE
00	17.408 MHz	—
01	34.816 MHz	—
10	46.421 MHz	—
11	69.632 MHz	—

Table 5. Reference Jitter Limits

Maximum Reference Clock Jitter in 12 KHz to 1 MHz Band	Operating Mode
14 ps	STS-12
28 ps	STS-3 CMI
56 ps	STS-3

Timing Generator

The Timing Generator function, seen in Figure 4, provides two separate functions. It provides a byte rate version of the TSCLK, and a mechanism for aligning the phase between the incoming byte clock and the clock which loads the parallel-to-serial shift register.

The PCLK output is a byte rate version of TSCLK. For STS-12, the PCLK frequency is 77.76 MHz, and for NRZ or CMI coded STS-3, its frequency is 19.44 MHz. For CMI coded E4, its frequency is 17.408 MHz. PCLK is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3005 device.

In the parallel-to-serial conversion process, the incoming data is passed from the PCLK byte clock timing domain to the internally generated byte clock timing domain, which is phase aligned to TSCLK. Although the frequency of PCLK and the internally generated byte clock is the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PCLK and the internally generated byte clock. Should the magnitude of the phase difference be less than one bit period, and if the SYNC input is high, the timing block inverts the internal byte clock.

Since the inversion of the internal byte clock will corrupt one byte of data, SYNC should be held low except when a phase correction is desired. When a timing domain phase difference of less than one bit period is detected, the Phase Alignment Event output (PAE) pulses high for one PCLK clock period. If the condition persists, PAE will remain high. When PAE conditions occur, SYNC should be activated until the condition is no longer present.

The Timing Generator also produces a feedback reference clock to the Clock Synthesizer (BYTCLKIP). A counter divides the synthesized clock down to the same frequency as the reference clock REFCLK. The PLL in the Clock Synthesizer maintains the stability of the synthesized clock by comparing the phase of the BYTCLKIP clock with that of the reference clock (REFCLK). The modulus of the counter is a function of the reference clock frequency and the operating frequency.

Parallel-to-Serial Converter

The Parallel-to-Serial converter shown in Figure 4 is comprised of two byte-wide registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PCLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

An internally generated byte clock, which is phase aligned to the transmit serial clock as described in the Timing Generator description, activates the parallel data transfer between registers. In STS-12 and STS-3 NRZ modes, the serial data is shifted out of

the second register at the TSCLK rate. In STS-3 CMI and E4 CMI modes, the serial data shifts out at the TSCLK/2 rate to the CMI encoder.

TRANSMITTER PIN DESCRIPTIONS

Input Signals

Parallel Data Input [PIN]<7:0>. TTL. A 77.76 Mbyte/s, 19.44 Mbyte/s, or 17.408 Mbyte/s word, aligned to the PCLK parallel input clock. PIN<7> is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PIN<0> is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). PIN[7:0] is sampled on the rising edge of PCLK.

Parallel Input Clock [PICKL]. TTL. A 77.76 MHz, 19.44 MHz, or 17.408 MHz nominally 50% duty cycle input clock, to which PIN[7:0] is aligned. PICKL is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PICKL samples PIN[7:0].

Test Clock Enable [TESTEN]. TTL. Set high to provide access to the PLL during production tests. (See Table 6.)

Synchronization Enable [SYNC]. TTL. Active high input that enables the timing generator to invert the internal byte transfer clock if transfers from the PIN<7:0> input holding register are occurring less than one bit period before or after clocking new data into the holding register. The SYNC pin is an asynchronous input.

Reference Clock [REFCLKP/N]. Differential ECL. Input used as the reference for the internal bit clock frequency synthesizer, or used as an externally provided bit clock. (See Tables 3 and 4.)

Reference Select [REFSEL]<1:0>. TTL. Inputs used to select the reference frequency for the internal clock synthesizer. (See Tables 3 and 4.)

Mode [MODE]<2:0>. TTL. Inputs used to select the operating mode of the device as 622.08 Mbit/s (STS-12); 155.52 Mbit/s (STS-3); 155.52 Mbit/s CMI (STS-3 electrical); or 139.764 Mbit/s (E4 CMI). (See Table 2.)

Line Loopback Data [LLDP/N]. Differential ECL. Inputs normally provided from a companion S3006 device. Used to implement a line loopback, in which the received bit serial data and clock signals are regenerated and passed through the S3005 transmitter. An internal 100- Ω resistor terminates LLDP to LLDN.

Line Loopback Clock [LLCLKP/N]. Differential ECL. Inputs normally provided from a companion S3006 device. Used to implement a line loopback, in which

received bit serial data and clock signals are regenerated and passed through the S3005 transmitter. An internal 100- Ω resistor terminates LLCLKP to LLCLKN.

Diagnostic Line Code Violation [DLCV]. TTL. A rising edge causes a CMI code violation in the serial output data. DLCV is an asynchronous input which is only valid when CMI is enabled.

Diagnostic Loopback Enable [DLEB]. TTL. Enables the DLD output when low. When DLEB is high, the DLD output is held in the inactive state to prevent interference between the transmit and receive devices. This signal will not affect the TSD signals.

Line Loopback Enable [LLEB]. TTL. When low, the LLD and LLCLK inputs are connected to the TSD and TSCLK outputs to implement line loopback. When in normal mode (LLEB high), the internally generated data and clock signals are output at TSD and TSCLK.

Master Reset [RSTB]. TTL. Reset input for the device, active low.

Output Signals

Transmit Serial Data [TSD P/N]. High-speed Source-terminated Differential ECL. Serial data stream signals, normally connected to an optical transmitter module. Updated on the falling edge of TSCLK.

Diagnostic Loopback Data [DLD P/N]. High-speed Differential ECL. Serial data stream signals, normally connected to a companion S3006 device for diagnostic loopback purposes. The DLD outputs are updated on the falling edge of TSCLK. They are held in the inactive state, except when DLEB is low.

Transmit Serial Clock [TSCLK P/N]. High-speed Source-terminated Differential ECL. Phase-aligned with the TSD and DLD output signals. TSCLK can be a buffered version of the internal frequency synthesizer clock, of the REFCLK inputs during clock bypass (TESTEN high), or of the LLCLK inputs during line loopback (LLEB low).

Parallel Clock [PCLK]. TTL/CMOS. A reference clock generated by dividing the internal bit clock by eight. It is normally used to coordinate byte-wide transfers between upstream logic and the S3005 device.

Phase Alignment Event [PAE]. TTL/CMOS. Pulses high during each PCLK cycle for which there is less than one bit period between the internal byte clock and PCLK timing domains. PAE is updated on the falling edge of the PCLK output.

Reference Feedback Clock [BYTCLKIP]. TTL/CMOS. It is compared with the reference clock (REFCLK) to maintain stability of the clock synthesis PLL. BYTCLKIP is at the same frequency as REFCLK and is an asynchronous output.

Lock Detect [LOCKDET]. TTL. Goes high after the PLL has had time to lock onto the clock provided on the REFCLK pins (approximately 2000 REFCLK cycles). LOCKDET is an asynchronous output.

S3006 RECEIVER ARCHITECTURAL/FUNCTIONAL DESIGN

The S3006 SERI receiver chip provides the first stage of digital processing of a receive SONET STS-12, STS-3, or ITU-T E4 bit serial stream. It converts the bit-serial 622.08, 155.52, or 139.264 Mbit/s data stream into 78 Mbyte/s, 19 Mbyte/s, or 17 Mbyte/s byte-serial data format depending on the control settings and reference frequency provided by the user. A Coded Mark Inversion (CMI) decoder can be enabled during 155.52 Mbit/s and 139.264 Mbit/s operation for decoding STS-3 electrical and E4 signals. These modes are selected by three input pins.

Clock recovery is performed on the incoming scrambled NRZ or CMI-coded data stream. A reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference frequency to the nominal bit rate. Reference frequencies of 19.44 MHz, 38.88 MHz, 51.84 MHz, or 77.76 MHz are selectable for SONET/SDH by the two reference select input pins. In E4 applications, these same pins can select the reference frequency from 17.408 MHz, 34.816 MHz, 46.421 MHz, or 69.632 MHz. For applications that provide a high-frequency bit clock externally, the internal synthesizer may be bypassed. (See Other Operating Modes.)

A loopback mode is provided for diagnostic loopback (transmitter to receiver). Signal pins are provided to allow for line loopback (receiver to transmitter) when used with the compatible S3005 device.

Clock Recovery

The Clock Recovery function, as shown in the block diagram in Figure 5, generates a clock that is frequency matched to the incoming data baud rate at the RSD or DLD differential inputs. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock. Frequency stability without incoming data

is guaranteed by an alternate reference input (REFCLK) to which the PLL locks when data is lost.

The MODE[2:0] inputs select the recovered serial clock frequency to be 622.08 MHz for STS-12, 311.04 MHz for CMI-encoded STS-3, 278.528 MHz for CMI-encoded E4, or 155.52 MHz for STS-3 NRZ. These frequencies are selected as shown in Table 2.

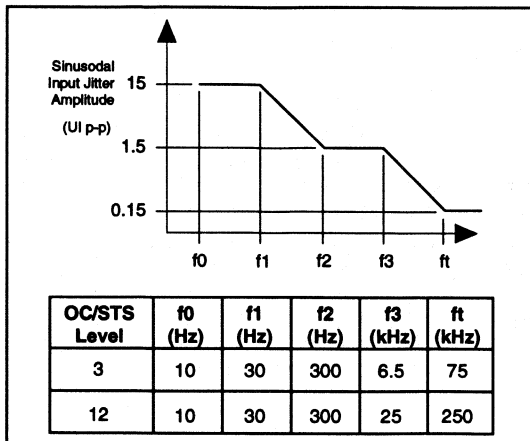
The clock recovery circuit monitors the incoming data stream for loss of signal. If the incoming encoded data stream has been low continuously for 4000 to 8000 recovered clock cycles, loss of signal is declared and the PLL will switch from locking onto the incoming data to locking onto the reference clock. Alternatively, the loss-of-signal (LOS) input can be used to force a loss-of-signal condition. When active, LOS squelches the incoming data stream, and causes the PLL to switch its source of reference. Loss-of-signal condition is removed when LOS is inactive, and good data, with acceptable pulse density and run length, returns on the incoming data stream.

When the test clock enable (TESTEN) input is set high, the clock recovery block is disabled. The reference clock (REFCLK) is used as the bit rate clock input in place of the recovered clock. The frequency of the REFCLK should be appropriate for the desired data rate. The reference selection inputs REFSEL[1:0] have no effect when TESTEN is set high.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields a typical capture time of 32 μ s for random incoming NRZ data.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which meets, with ample margin, the minimum tolerance proposed for SONET equipment by the T1X1.6/91-022 document, shown in Figure 6.

Figure 6. Clock Recovery Jitter Tolerance



Backup Reference Generator

The Backup Reference Generator seen in Figure 5 provides backup reference clock signals to the clock recovery block when the clock recovery block detects a loss of signal condition. It contains a counter that divides the clock output from the clock recovery block down to the same frequency as the reference clock REFCLK. The modulus of the counter is a function of the reference clock frequency and the operating frequency. The frequency of the reference clock is selected by the REFSEL[1:0] inputs, as shown in Tables 3 and 4.

Frame and Byte Boundary Detection

The Frame and Byte Boundary Detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. This pattern occurs in both STS-3 and STS-12. Framing pattern detection is enabled and disabled by the out-of-frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration OOF is set high. It is disabled when a framing pattern is detected and OOF is no longer set high. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (RSD or DLD). The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). The frame boundary is reported on the frame pulse (FP) output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an STS-3 or STS-12 stream will generate the 48-bit framing pattern is extremely small. It is highly improbable that a mimic pattern would occur within one frame of data. Therefore, the time to match the first frame pattern and to verify it with down-stream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 μ s, even for extremely high bit error rates.

Once down-stream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input can be set low to disable the frame search process from trying to synchronize to a mimic frame pattern.

The Frame and Byte boundary Detection function is not utilized in the E4 operating mode. It is recommended that the OOF input remain low at all times for E4 operation to avoid spurious realignment of the byte boundary, and the FP output should be ignored.

Serial to Parallel Converter

The Serial to Parallel Converter consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the clock generated by the clock recovery block. The second is an 8-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the Serial to Parallel converter can vary from 1.5 to 2.5 byte periods (12 to 20 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries, with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial to parallel converter is that POCLK is neither truncated nor extended during reframe sequences.

S3006 RECEIVER PIN DESCRIPTIONS

Input Signals

Receive Serial Data [RSDP/N]. High Speed differential ECL. Serial data stream signals normally connected to an optical receiver module. When internal clock recovery is used, clock is recovered from transitions on the RSD inputs. When external clock recovery is used, the RSD inputs are sampled on the rising edge of the reference clock (REFCLK). An internal 100-Ω termination resistor is connected across RSDP and RSDN.

Diagnostic Loopback Data [DLDP/N]. High Speed differential ECL. Serial data stream signals, normally connected to a companion S3005 device for diagnostic loopback purposes. Clock is recovered from transitions on the DLD inputs while in diagnostic loopback. An internal 100-Ω termination resistor is connected across DLDP and DLDN.

Diagnostic Loopback Enable [DLEB]. TTL. Selects diagnostic loopback. When DLEB is high, the S3006 device uses the primary data (RSD) input. When low, the S3006 device uses the diagnostic loopback data (DLD) input.

Out of Frame [OOF]. TTL. Indicator used to enable framing pattern detection logic in the S3006. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set low, whichever is longer. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. (See Figures 17 and 18.)

Loss of Signal [LOS]. ECL. Active high. A single-ended 10K ECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When LOS is high, the data on the Serial Data In (RSDP/N) pins will be internally forced to a constant zero, LOCKDET forced low, and the PLL forced to lock to the REFCKINP/N inputs.

This signal must be used to assure correct automatic reacquisition to serial data following an interruption and subsequent reconnection of the optical path. This will assure that the PLL does not "wander" out of reacquisition range by tracking the random phase/frequency content of the optical detector's noise floor while monitoring "dark" fiber.

When LOS is low, data on the RSDP/N pins will be processed normally.

Reference Clock [REFCLKP/N]. Differential ECL. Input normally used as the reference for the integral clock recovery PLL. (See Tables 3 and 4.) When the test clock enable (TESTEN) input is set high, REFCLK replaces the bit rate recovered clock. (See Table 6.)

Reference Select [REFSEL]<1:0>. TTL. Inputs used to select the reference frequency for the internal clock synthesizer. (See Tables 3 and 4.)

Mode [MODE]<2:0>. TTL. Inputs used to select the operating mode of the device as 622.08 Mbit/s (STS-12); 155.52 Mbit/s (STS-3); 155.52 Mbit/s CMI (STS-3 electrical); or 139.764 Mbit/s (E4 CMI). (See Table 2.)

Test Clock Enable [TESTEN]. TTL. Set high to provide access to the PLL during production tests. It can also be used to enable an external clock source in bypass mode (see Table 6).

Test Reset [TESTRST]. TTL. Used to reset portions of the clock recovery PLL during production testing. Held low for normal operation.

Master Reset [RSTB]. TTL. Input for the device, active low. After reset, frame boundary detection is disabled.

Output Signals

Line Loopback Data [LLDP/N]. High-speed Source-terminated Differential ECL. A regenerated version of either the incoming data stream (RSD) input in normal mode, or the diagnostic loopback data (DLD) input in diagnostic loopback mode (DLEB set high). LLD is updated on the rising edge of LLCLK.

Line Loopback Clock [LLCLKP/N]. High-speed Source-terminated Differential ECL. Phase aligned with the line loopback data (LLD) output signals. LLCLK can be a buffered version of the internally recovered bit clock, or the reference clock (REFCLK) input when clock recovery is bypassed (TESTEN set high).

OTHER OPERATING MODES

Parallel Output [POUT]<7:0>. TTL/CMOS A 77.76 Mbyte/s, 19.44 Mbyte/s, or 17.408 Mbyte/s word, aligned to the POCLK parallel output clock. POUT<7> is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). POUT<0> is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). POUT[7:0] is updated on the falling edge of POCLK.

Line Code Violation [LCV]. TTL/CMOS. Set high to indicate that one or more bits of the byte currently presented on POUT<7:0> contains a CMI line code violation. LCV is only active in STS-3 CMI and E4 CMI modes. LCV is updated on the falling edge of POCLK.

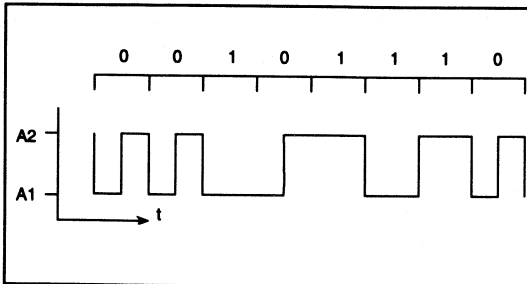
Frame Pulse [FP]. TTL/CMOS. Indicates frame boundaries in the incoming data stream (RSD). If framing pattern detection is enabled, as controlled by the OOF input, FP pulses high for one POCLK cycle when a 48-bit sequence matching the framing pattern is detected on the RSD inputs. When framing pattern detection is disabled, FP pulses high when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK.

Parallel Output Clock [POCLK]. TTL/CMOS. A 77.76 MHz, 19.44 MHz, or 17.408 MHz nominally 50% duty cycle byte rate output clock, that is aligned to POUT<7:0> byte serial output data. POUT<7:0>, FP and LCV are updated on the falling edge of POCLK.

Reference Feedback Clock [BYTCLKIP]. TTL/CMOS. Compared with the reference clock (REFCLK) to maintain stability of the clock recovery PLL when it is in loss of signal state. BYTCLKIP is at the same frequency as REFCLK and is an asynchronous output.

Lock Detect [LOCKDET]. TTL. Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming data stream. LOCKDET will go low if the incoming encoded data stream has been low continuously for 4000 to 8000 bit times. LOCKDET will go high if LOS is low and good data with acceptable run length and transition density returns on the incoming data stream. LOCKDET is an asynchronous output.

Figure 7. CMI Encoded Data



OTHER OPERATING MODES

CMI Encoding and Decoding

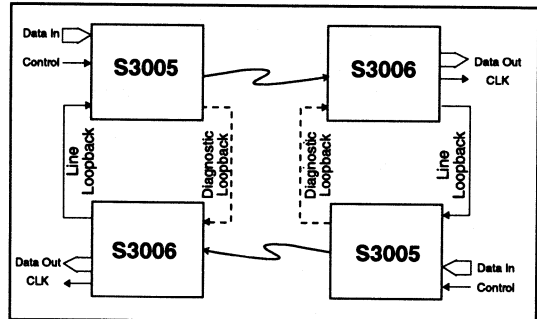
Coded Mark Inversion format (CMI) ensures at least one data transition per bit period, thus aiding the clock recovery process. Zeros are represented by a Low state for one half a bit period, followed by a High state for the rest of that bit period. Ones are represented by a steady Low or High state for a full bit period. The state of the ones bit period alternates at each occurrence of a one. Figure 7 shows an example of CMI-encoded data. The STS-3 electrical interface and the E4 interface are specified to have CMI-encoded data.

The CMI encoder on the S3005 SETI accepts serial data from the Parallel-to-Serial converter block at one half the TSCLK rate. The data is then encoded into CMI format, and the result is shifted out into the output selection logic at the TSCLK rate (311.04 MHz for STS-3 electrical, 278.528 MHz for E4). The MODE[2:0] inputs control whether the CMI encoder is in the data path. The encoder is only in the data path when the STS-3 CMI or the E4 CMI modes are selected. A single CMI violation can be inserted for diagnostic purposes by applying a low-to-high transition on DLCV. This violation is either an inverted zero code or an inversion of the alternating ones logic level, depending on the state of the data. Subsequent one codes take into account the induced violation to avoid error multiplication.

The CMI decoder block on the S3006 SERI accepts serial data from the RSDP/N input at the TSCLK rate (311.04 MHz or 278.528 MHz). The data is then decoded from CMI to NRZ format and converted from serial to parallel at one half the TSCLK rate.

Note that in CMI operating mode, the data bit rate is one half of the recovered clock rate.

Figure 8. Interface Diagram



Diagnostic Loopback

The Diagnostic Loopback path consists of alternate serial data outputs (in the case of the S3005) and inputs (in the case of the S3006).

On the S3005, the differential ECL output DLD provides Diagnostic Loopback serial data. When the Diagnostic Loopback Enable (DLEB) input is low, this data output is a replica of TSD. When DLD is connected to the S3006, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. When DLEB is high, DLD is held in the inactive state, with the positive output high and the negative output low. In the inactive state, there will be no interference from the transmitter to the receiver. The DLD outputs on the S3005 should be held inactive (DLEB high) when not in use to avoid potential crosstalk of the asynchronous DLD signals with the serial data signals.

On the receiver side, the differential ECL input DLD is the Diagnostic Loopback serial data input. When the Diagnostic Loopback Enable (DLEB) input is set low, the DLD input is routed in place of the normal data stream (RSD).

Line Loopback

The Line Loopback circuitry consists of alternate clock and data output drivers. For the S3005, it selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable input (LLEB) is high, it selects data and clock from the Parallel to Serial Converter block or the CMI Encoder block. When LLEB is low, it forces the output data multiplexor to select data and clock from the LLD and LLCLK inputs. When these inputs are connected to the Line Loop Clock (LLCLK) and Line Loop Data (LLD) outputs of a S3006 receiver, a receive-to-transmit loopback can be established at the serial data rate.

Test and Bypass Modes

The Test Clock Enable (TESTEN) inputs on both chips provide access to the PLL.

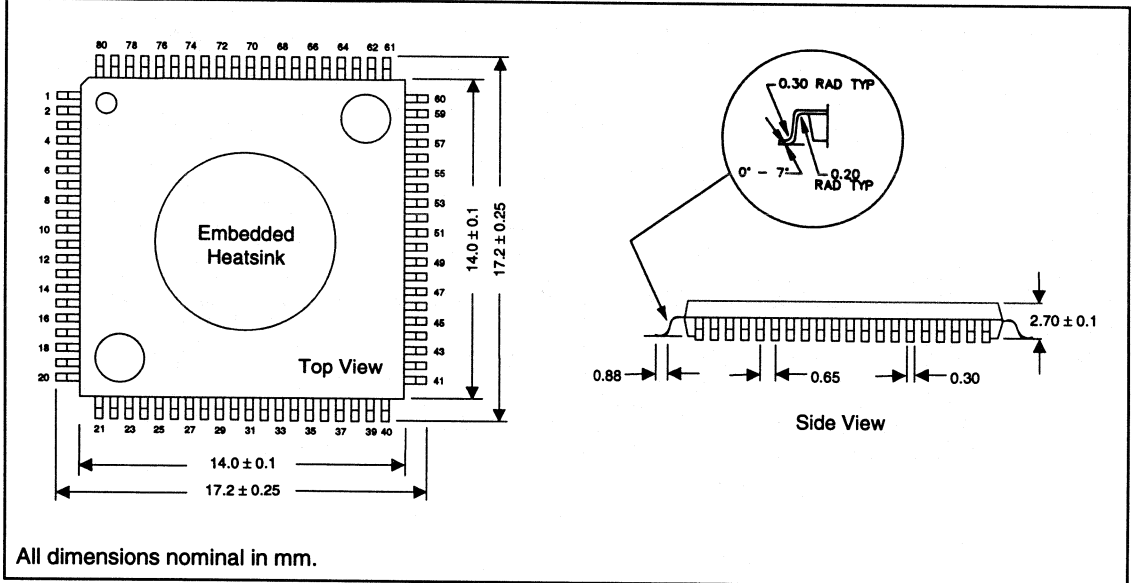
The PLL-generated clock source on both the S3005 and S3006 can be bypassed by setting TESTEN high. In this mode, an externally generated bit serial clock source must be applied at the REFCLK input. Table 6 lists the possible combinations allowed in bypass mode.

Table 6. Bypass Mode

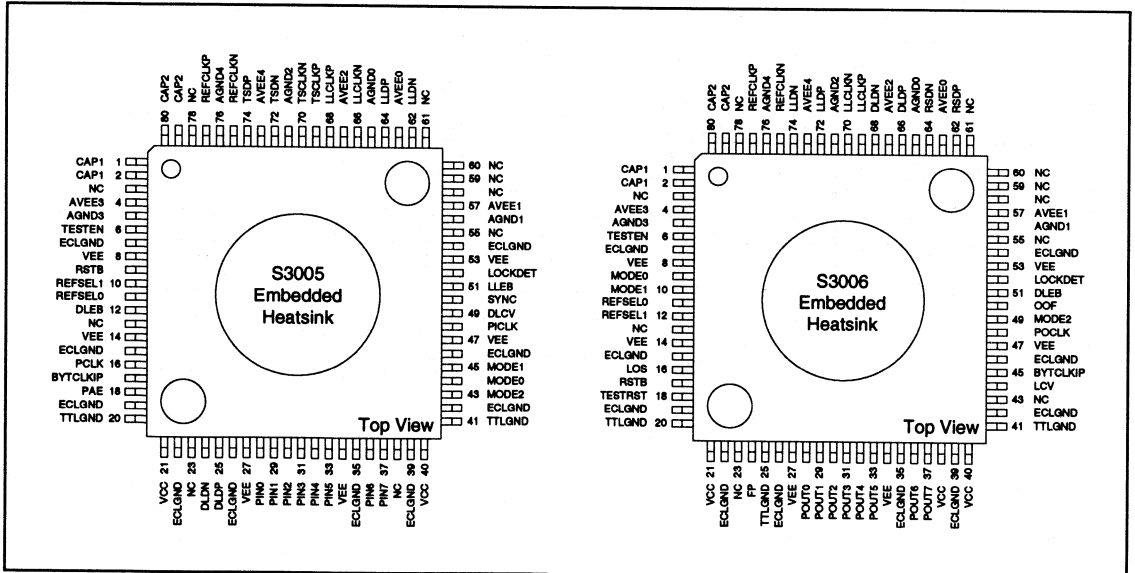
TESTEN	MODE[2:0]	Reference Clock Frequency In Bypass Mode	Serial Data Rate (Mbit/s)
0	XXX	Normal Operating Mode (See Table 2)	—
1	100	622.08	622.08
1	101	311.04	155.52 CMI
1	101	278.528	139.264 CMI
1	110	155.52	155.52

80 TEP PINOUTS

80 PQFP Package



S3005 and S3006 80 PQFP Pinouts



S3005 68 LDCC PINOUT

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	VCC	18	ECL GND	35	NC	52	ECL GND
2	PIN[7]	19	VCC	36	REFCLKP	53	AVEE1
3	PIN[6]	20	PAE	37	AGND4	54	AGND1
4	ECL GND	21	BYTCLKIP	38	REFCLKN	55	NC
5	PIN[5]	22	TTL GND	39	TSDP	56	LOCKDET
6	VEE	23	PCLK	40	AVEE4	57	LLEB
7	VEE	24	VEE	41	TSDN	58	SYNC
8	PIN[4]	25	ECL GND	42	AGND2	59	DLCV
9	PIN[3]	26	DLEB	43	TSCLKN	60	PICLK
10	PIN[2]	27	REFSEL[0]	44	TSCLKP	61	ECL GND
11	VEE	28	REFSEL[1]	45	LLCLKP	62	VEE
12	PIN[1]	29	RSTB	46	AVEE2	63	MODE[1]
13	ECL GND	30	VEE	47	LLCLKN	64	TTL GND
14	PIN[0]	31	TESTEN	48	AGNDØ	65	MODE[0]
15	DLDP	32	AGND3	49	LLDP	66	MODE[2]
16	DLDN	33	AVEE3	50	AVEEØ	67	TTL GND
17	VCC	34	ECL GND	51	LLDN	68	ECL GND

S3006 68 LDCC PINOUT

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	VCC	18	ECL GND	35	NC	52	ECL GND
2	POUT[7]	19	VCC	36	REFCLKP	53	AVEE1
3	POUT[6]	20	TESTRST	37	AGND4	54	AGND1
4	ECL GND	21	RSTB	38	REFCLKN	55	NC
5	POUT[5]	22	TTL GND	39	LLDN	56	LOCKDET
6	VEE	23	LOS	40	AVEE4	57	DLEB
7	VEE	24	VEE	41	LLDP	58	OOF
8	POUT[4]	25	ECL GND	42	AGND2	59	MODE[2]
9	POUT[3]	26	REFSEL[1]	43	LLCLKN	60	POCLK
10	POUT[2]	27	REFSEL[0]	44	LLCLKP	61	ECL GND
11	VEE	28	MODE[1]	45	DLDN	62	VEE
12	POUT[1]	29	MODE[0]	46	AVEE2	63	BYTCLKIP
13	ECL GND	30	VEE	47	DLDP	64	TTL GND
14	POUT[0]	31	TESTEN	48	AGNDØ	65	LCV
15	TTL GND	32	AGND3	49	RSDN	66	VCC
16	FP	33	AVEE3	50	AVEEØ	67	TTL GND
17	VCC	34	ECL GND	51	RSDP	68	ECL GND

Power Supply Connections:

VCC	+5V
VEE	-4.5V
TTL GND	0V
ECL GND	0V
AGND 0, 1, 2, 3, 4	0V
AVEE 0, 1, 2, 3, 4	-4.5V

Table 7. Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	Given REFCLK = SERCLK + 8, 12, 16 or 32 per REFSEL<1:0> settings
ECL Data Output Jitter (S3005 TSDP/N, DLDP/N) OC-3/STS-3 OC-STS-3 CMI OC-12/STS-12 ¹			64 32 16	ps (rms) ps (rms) ps (rms)	Given the jitter on REFCLK (12KHz to 1 MHz band) is less than: <ul style="list-style-type: none"> • 56 ps rms (OC-3) • 28 ps rms (OC-STS-3 CMI) • 14 ps rms (OC-12), REFCLK = 77.76 MHz
Reference Clock Frequency Tolerance Clock Synthesis S3005 REFCKINP/N S3006 REFCKINP/N	-20 -100		20 100	ppm ppm	Required to meet SONET output frequency specification
OC-3/STS-3 & OC-12/STS-12 Capture Range Lock Range		±200 +8, -12		ppm %	With respect to fixed reference frequency Minimum transition density of 20%
Acquisition Lock Time ² OC-3/STS-3 OC-STS-3 CMI OC-12/STS-12			64 32 16	μsec	With device already powered up and valid REFCLK
Reference Clock Input Duty Cycle	30		70	% of period	
Reference Clock Rise & Fall Times			2.0	ns	10% to 90% of amplitude
ECL Output Rise & Fall Times (S3005 DLDP/N)			600	ps	20% to 80%, 50Ω to -2V equivalent load, as per Figure 19
Source Terminated Differential ECL Compatible Outputs Rise and Fall Times			450	ps	20% to 80%, 100Ω line to line, as per Figure 19

1 For REFCLK = 19.44, 38.88 or 51.84 MHz, multiply the specified value by three.

2 Specifications based on design values. Not tested.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	Min	Typ	Max	Unit
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Respect to GND	-0.5		+7.0	V
Voltage on VEE with Respect to GND	+0.5		-8.0	V
Voltage on Any TTL Input Pin	-0.5		+5.5	V
Voltage on Any ECL Input Pin	-3		0	V
TTL/CMOS Output Sink Current			20	mA
TTL/CMOS Output Source Current			25	mA
High Speed ECL Output Source or Sink Current			50	mA
Static Discharge Voltage		500		V

RECOMMENDED OPERATING CONDITIONS

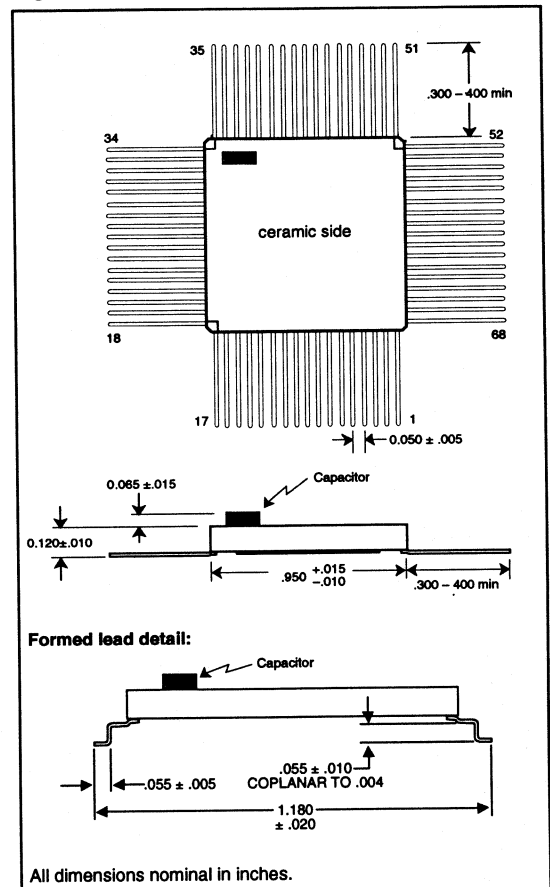
PARAMETER	Min	Typ	Max	Unit
Ambient Temperature under Bias	-40		85	°C
Junction Temperature under Bias	-10		130	°C
Voltage on VCC with Respect to GND	4.75	5.0	5.25	V
Voltage on VEE with Respect to GND ¹	-4.2	-4.5/-5.2	-5.46	V
Voltage on Any TTL Input Pin	0		VCC	V
Voltage on Any ECL Input Pin	-2.0		0	V
TTL/CMOS Output Sink Current			8	mA
TTL/CMOS Output Source Current			20	mA
ECL Output Source Current			25	mA
Source Terminated Diff. ECL Compatible Output Source or Sink Current			10	mA
S3005 ICC		41	52	mA
S3005 IEE		314	402	mA
S3006 ICC		54	69	mA
S3006 IEE		324	414	mA

1. V_{EE} (min) = -4.2V for Ambient Temperature $\geq 0^\circ\text{C}$, -4.5V for Ambient Temperature $< 0^\circ\text{C}$.

Thermal Management

Device	Package	Θ_{jc}	Θ_{ja} Still Air	Power	Max Still Air	Air/70°C	Air/85°C	Air/70°C for 100°C Tj
S3005	68 LDCC	2.5°C/W	33.9°C/W	2.4W	49°C	200 LFPM	500 LFPM	750 LFPM
	w/45-20 HS		26.4°C/W	2.4W	66°C	<50 LFPM	140 LFPM	210 LFPM
S3005	80 TEP	2.0°C/W	30°C/W	2.4W	58°C	200 LFPM	700 LFPM	1050 LFPM
	w/45-28 HS		23°C/W	2.4W	75°C	N/A	200 LFPM	300 LFPM
S3006	68 LDCC	2.5°C/W	33.9°C/W	2.6W	42°C	310 LFPM	600 LFPM	900 LFPM
	w/45-20 HS		26.4°C/W	2.6W	61°C	100 LFPM	150 LFPM	230 LFPM
S3006	80 TEP	2.0°C/W	30°C/W	2.6W	52°C	300 LFPM	750 LFPM	1130 LFPM
	w/45-28 HS		23°C/W	2.6W	70°C	N/A	250 LFPM	380 LFPM

Figure 9. 68-pin LDCC Package



TTL INPUT/OUTPUT DC CHARACTERISTICS¹

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{EE} = -4.5\text{ V} \pm 7\%$ or $-5.2 \pm 5\%$)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IL}^2	Input LOW Voltage	Guaranteed Input LOW Voltage		0.8	Volts
V_{IH}^2	Input HIGH Voltage	Guaranteed Input HIGH Voltage	2.0		Volts
I_{IL}	Input LOW Current	$V_{CC} = \text{MAX}$, $V_{IN} = 0.5\text{V}$	-400.0		μA
I_{IH}	Input HIGH Current	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7\text{V}$		50.0	μA
I_I	Input HIGH Current at Max VCC	$V_{CC} = \text{MAX}$, $V_{IN} = 5.25\text{V}$		1.0	mA
I_{OS}	Output Short Circuit Current	$V_{CC} = \text{MAX}$, $V_{OUT} = 0.5\text{V}$	-100.0	-25.0	mA
I_{OZL}	Output Three-State Current LOW	$V_{CC} = \text{MAX}$, $V_{OL} = 0.4\text{V}$	-50.0	50.0	μA
I_{OZH}	Output Three-State Current HIGH	$V_{CC} = \text{MAX}$, $V_{OH} = 2.4\text{V}$	-50.0	50.0	μA
V_{IK}	Input Clamp Diode Voltage	$V_{CC} = \text{MIN}$, $I_{IN} = -18\text{mA}$	-1.2		Volts
V_{OL}	TTL Output LOW Voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 8\text{mA}$		0.5	Volts
V_{OH}	TTL Output HIGH Voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -1.0\text{mA}$	2.4		Volts
V_{OL}	CMOS Compatible Output LOW Voltage	$V_{CC} = \text{MIN}$, $I_{OH} = 100\mu\text{A}$		0.4	Volts
V_{OH}	CMOS Compatible Output HIGH Voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -100\mu\text{A}$	3.4		Volts

- These conditions will be met with an airflow of 400 LFPM.
- These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

ECL INPUT/OUTPUT DC CHARACTERISTICS⁷

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{EE} = -4.5\text{ V} \pm 7\%$ or $-5.2 \pm 5\%$)

Symbol	Parameter	Conditions	Signal Name	Min	Max	Unit
V_{IL}^1	Input LOW Voltage	Guaranteed Input LOW Voltage for all single ended inputs		-2.00	-1.47	Volts
V_{IH}^1	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all single ended inputs		-1.18	-0.80	Volts
V_{IL}^2	Input LOW Voltage	Guaranteed Input LOW Voltage for all differential inputs		-2.00	-0.70	Volts
V_{IH}^2	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all differential inputs		-1.75	-0.45	Volts
V_{ID}^2	Input DIFF Voltage	Guaranteed Input DIFF Voltage for all differential inputs		0.25	1.40	Volts
I_{IL}	Input LOW Current	$V_{EE} = \text{MAX}$, $V_{IL} = -1.95\text{V}$	LOS ⁶	-0.50	20.00	μA
		$V_{EE} = \text{MAX}$, $V_{DIFF} = 0.5\text{V}$	LLDP ⁵ , LLCLKP ⁵ , RSDP ⁶ , DLDP ⁶	-7.00	-3.50	mA
		$V_{EE} = \text{MAX}$, $V_{DIFF} = 0.5\text{V}$	LLDN ⁵ , LLCLKN ⁵ , RSDN ⁶ , DLDN ⁶	-8.30	-2.80	mA
		$V_{EE} = \text{MAX}$, $V_{DIFF} = 0.5\text{V}$	REFCLKP ^{5,6} , REFCLKN ^{5,6}	-1.00	20.00	μA
I_{IH}	Input HIGH Current	$V_{EE} = \text{MAX}$, $V_{IH} = -0.80\text{V}$	LOS ⁶	-0.50	20.00	μA
		$V_{EE} = \text{MAX}$, $V_{DIFF} = 0.5\text{V}$	LLDP ⁵ , LLCLKP ⁵ , RSDP ⁶ , DLDP ⁶	3.50	7.00	mA
		$V_{EE} = \text{MAX}$, $V_{DIFF} = 0.5\text{V}$	LLDN ⁵ , LLCLKN ⁵ , RSDN ⁶ , DLDN ⁶	2.80	8.30	mA
		$V_{EE} = \text{MAX}$, $V_{DIFF} = 0.5\text{V}$	REFCLKP ^{5,6} , REFCLKN ^{5,6}	-1.00	20.00	μA
V_{OL}^3	Output LOW Voltage	50 Ω to -2V termination		-2.00	-1.50	Volts
V_{OH}^3	Output HIGH Voltage	50 Ω to -2V termination		-1.11	-0.62	Volts
V_{OL}^4	Output LOW Voltage	100 Ω between differential outputs		-2.50	-0.80	Volts
V_{OH}^4	Output HIGH Voltage	100 Ω between differential outputs		-2.20	-0.50	Volts
V_{OD}^4	Output DIFF Voltage	100 Ω between differential outputs		0.30	1.00	Volts

- Single Ended ECL Inputs
- Differential ECL Inputs
- Standard ECL Outputs
- Source Terminated Differential ECL Compatible Outputs
- S3005 Signals
- S3006 Signals
- These conditions will be met with an airflow of 400 LFPM.

Table 8. S3005 AC Timing Characteristics

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{EE} = -4.5\text{ V} \pm 7\%$ or $-5.2\text{ V} \pm 5\%$)

Symbol	Description	Min	Max	Units
	TSCLK Frequency (nom. 155, 311, or 622 MHz)		640	MHz
	TSCLK Duty Cycle	40	60	%
	PICLK Duty Cycle	33	67	%
t_{SPIN}	PIN [7:0] Set-up Time w.r.t. PICLK	2.0		ns
t_{HPIN}	PIN [7:0] Hold Time w.r.t. PICLK	1.0		ns
t_{SLLD}	LLD Set-Up Time w.r.t. LLCLK	100		ps
t_{HLLD}	LLD Hold Time w.r.t. LLCLK	100		ps
	LLCLK Duty Cycle	40	60	%
t_{PTSD}	TSCLK Low to TSD Valid Propagation Delay		440	ps
t_{STSD}	TSD Set-Up Time w.r.t. TSCLK	400		ps
t_{HTSD}	TSD Hold Time w.r.t. TSCLK	400		ps
t_{PPAE1}	PCLK Low to PAE Valid Propagation Delay		3.0	ns
TSD^1_{ESK}	TSD \pm Edge Skew		100	ps
$TSCLK^1_{ESK}$	TSCLK \pm Edge Skew		100	ps

¹ Guaranteed but not tested.

Figure 10. PIN AC Input Timing

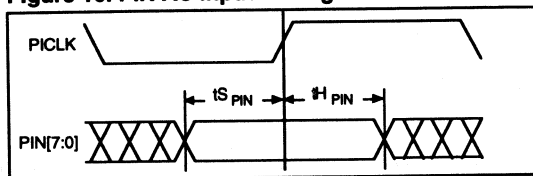
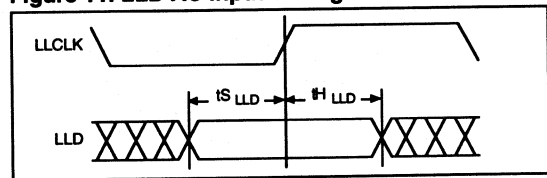
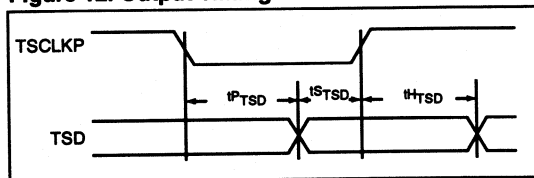


Figure 11. LLD AC Input Timing



- When a set-up time is specified on TTL signals between an input and a clock, the set-up time is the time in picoseconds from the 50% point of the input to the 50% point of the clock.
- When a hold time is specified on TTL signals between an input and a clock, the hold time is the time in picoseconds from the 50% point of the clock to the 50% point of the input.
- When a set-up time is specified on differential ECL signals between an input and a clock, the set-up time is the time in picoseconds from the cross-over point of the input to the cross-over point of the clock.
- When a hold time is specified on differential ECL signals between an input and a clock, the hold time is the time in picoseconds from the cross-over point of the clock to the cross-over point of the input.

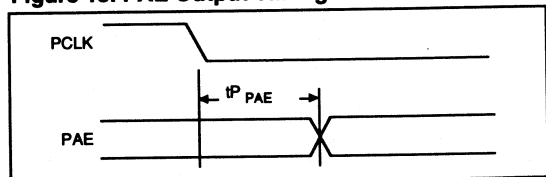
Figure 12. Output Timing



Notes on High-Speed PECL Output Timing

- Output propagation delay time is the time in nanoseconds from the cross-over point of the reference signal to the cross-over point of the output.

Figure 13. PAE Output Timing



Notes on TTL Output Timing

- Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
- Maximum output propagation delays are measured with a 15pF load on the outputs.

Table 9. S3005 External Clock Mode Timing

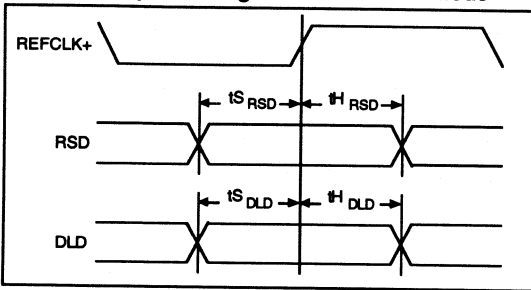
Description	Min	Max	Units
REFCLK in Bypass Mode (nom. 155, 311, or 622 MHz)		640	MHz
REFCLK in Bypass Mode duty cycle	33	67	%

Table 10. S3006 AC Timing Characteristics

Symbol	Description	Min	Max	Units
	POCLK Duty Cycle ¹	40	60	%
$t_{P_{POUT}}$	POCLK Low to POUT [7:0] Valid Prop. Delay @ STS-3 POCLK Low to POUT [7:0] Valid Prop. Delay @ STS-12	0 0	5 1.5	ns ns
$t_{P_{FP}}$	POCLK Low to FP Valid Propagation Delay @ STS-3 POCLK Low to FP Valid Propagation Delay @ STS-12	0 0	5 1.5	ns ns
	LLCLK Frequency		640	MHz
	LLCLK Duty Cycle	40	60	%
$t_{P_{LLD}}$	LLCLK Low to LLD Valid Propagation Delay @ STS-3 LLCLK Low to LLD Valid Propagation Delay @ STS-12	-800 -500	800 500	ps ps

¹ Driving CMOS with a 2.5V threshold and a 500Ω load, or driving TTL with a 1.4V threshold and a 150Ω load.

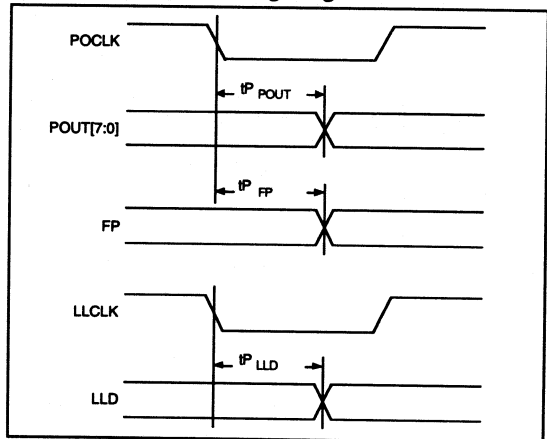
Figure 14. Input Timing - External Clock Mode



Notes on Input Timing:

- When a set-up time is specified between a data input and a clock input, the set-up time is the time in picoseconds from the crossover point of the differential data input to the crossover point of the differential clock input.
- When a hold time is specified between a data input and a clock input, the hold time is the time in picoseconds from the crossover point of the differential clock input to the crossover point of the differential data input.

Figure 15. Output Timing Diagram



Notes on Output Timing:

- Output timing specification are valid when terminating all outputs with 500Ω to GND.
- Output propagation delay time of TTL outputs is the time in picoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
- Maximum output propagation delays of TTL outputs are measured with a 15 pF load on the outputs.
- Output propagation delay time of high speed ECL outputs is the time in picoseconds from the cross-over point of the reference signal to the cross-over point of the output.
- Maximum output propagation delays of TTL outputs are measured with a 50Ω transmission line on the outputs.

Table 11. S3006 External Clock Mode Timing

Symbol	Description	Min	Max	Units
	REFCLK Freq. (Nominally 622/311//155 MHz)		640	MHz
	REFCLK Duty Cycle	33	67	%
$t_{S_{RSD}}$	RSD to REFCLK Set-up Time	300		ps
$t_{H_{RSD}}$	REFCLK to RSD Hold Time @ STS-3 REFCLK to RSD Hold Time @ STS-12	1.0 100		ns ps
$t_{S_{DLD}}$	DLD to REFCLK Set-up Time	300		ps
$t_{H_{DLD}}$	REFCLK to DLD Hold Time @ STS-3 REFCLK to DLD Hold Time @ STS-12	1.0 100		ns ps

RECEIVER FRAMING

Figure 16 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is high. Both boundaries are recognized upon receipt of the third A2 byte which is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUT[7:0]). Concurrently, the frame pulse is set high for one POCLK cycle.

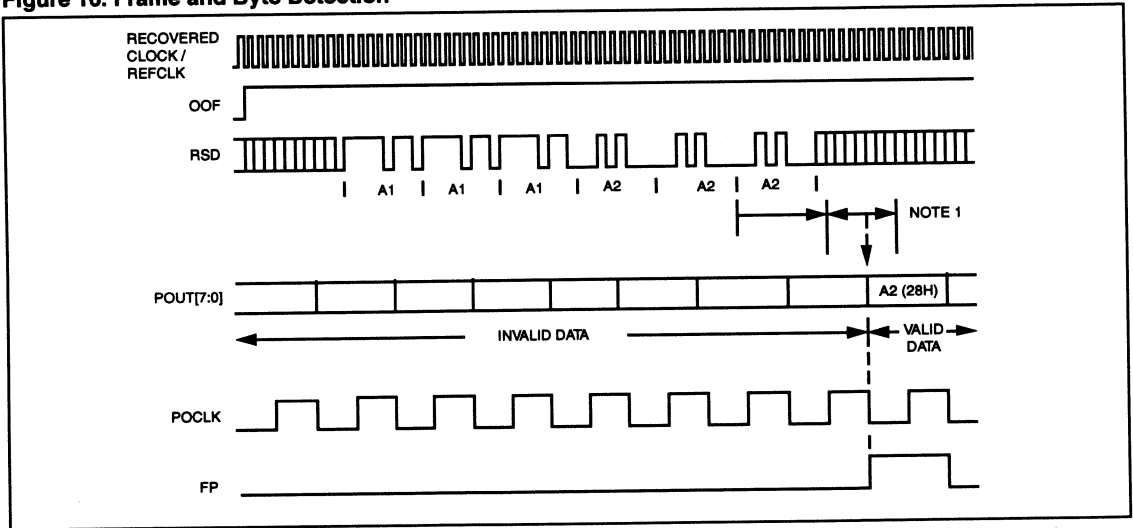
When interfacing with a section terminating device, the OOF input remains high for one full frame after the first frame pulse while the section terminating device verifies internally that the frame and byte alignment are correct, as shown in Figure 17. Since at least one framing pattern has been detected since the rising

edge of OOF, boundary detection is disabled when OOF is set low.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse or until OOF goes low, whichever occurs last. Figure 17 shows a typical OOF timing pattern which occurs when the S3006 is connected to a down stream section terminating device. OOF remains high for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes low.

Figure 18 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 16. Frame and Byte Detection



NOTE 1: Range of input to output delay can be 1.5 to 2.5 POCLK cycles

Figure 17. OOF Operation Timing with SSTX

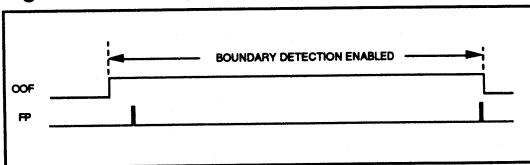


Figure 18. Alternate OOF Timing

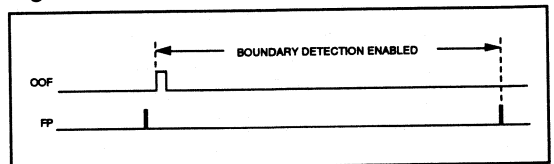
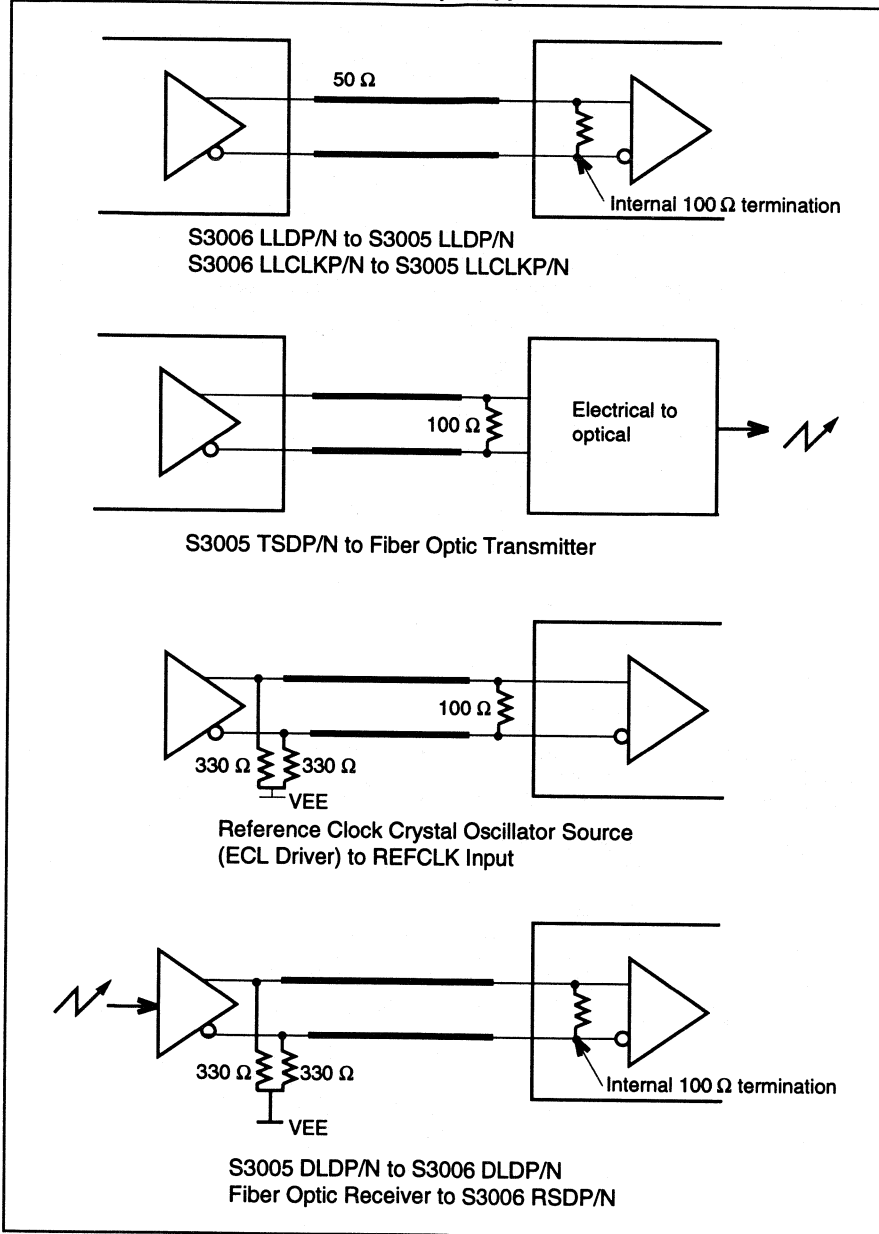


Figure 19. Differential ECL Input and Output Applications

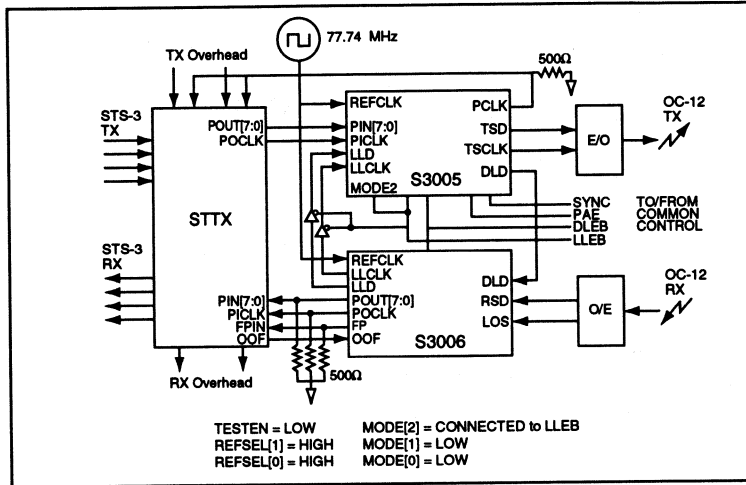


STS-12/STS-3 OPTICAL INTERFACE

The S3005 and S3006 devices are designed to interface seamlessly to make a SONET transceiver for STS-12, CMI-encoded STS-3, and STS-3. Figure 20 shows these two devices connected together with

receive and transmit overhead processors on the equipment side and electrical-to-optical converters on the line side to realize the core of a typical SONET transceiver.

Figure 20. OC-12 Application

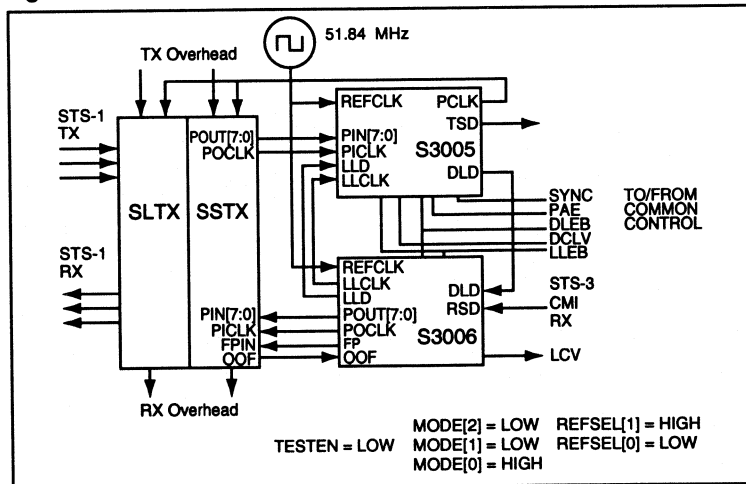


STS-3 CMI ELECTRICAL INTERFACE

With the S3006 devices optioned for CMI-coded STS-3, an electrical SONET transceiver can be implemented as shown in Figure 21. In this case, a clock reference

of 51.84 MHz was selected. TSD would be coupled through a line driver and transformer to a coaxial cable for short span applications.

Figure 21. CMI Electrical Interface

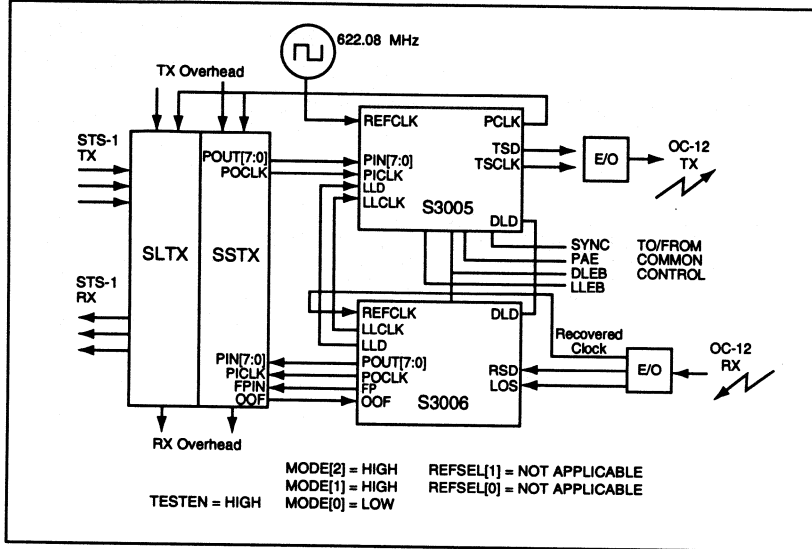


EXTERNAL CLOCK APPLICATION

The S3006 can receive data at SONET or other standard data rates by bypassing the internal clock recovery PLL and supplying the appropriate clock to the REFCLK input. Figure 22 shows an application for

STS-12 with external clock recovery on the receive side, and an external transmit clock connected to REFCLK of the S3005 device.

Figure 22. OC-12 External Clock Application



Ordering Information

GRADE	TRANSMITTER	PACKAGE	SPEED GRADE
S – commercial	3005	A – 68 LDCC with straight leads B – Bare Die C – 68 LDCC lead formed D – 80 PQFP	1 – 139 Mbit/s 1 – 139 Mbit/s CMI 1 – 155 Mbit/s 1 – 155 Mbit/s CMI 6 – 622 Mbit/s

GRADE	TRANSMITTER	PACKAGE	SPEED GRADE
S – commercial	3006	A – 68 LDCC with straight leads B – Bare Die C – 68 LDCC lead formed D – 80 PQFP	1 – 139 Mbit/s 1 – 139 Mbit/s CMI 1 – 155 Mbit/s 1 – 155 Mbit/s CMI 6 – 622 Mbit/s

X **XXXX** **X** — **X**
Grade Part number Package Speed Grade

EVALUATION BOARD DESCRIPTION

The S6004 SONET Evaluation Board allows demonstration of AMCC's S3005 and S3006 SONET/SDH OC-3/12 transmitter/receiver chipset. This data sheet provides information on board contents and layout. It should be used in conjunction with the S3005/S3006 data sheets, which contain full technical details on chip operation.

Figure 1 depicts the layout of the evaluation board, showing the location of connectors and components. Power is supplied to the board from external jacks supplied through the on-board banana jacks. Connectors allow easy access to all of the interface signals on the S3005/S3006 chips.

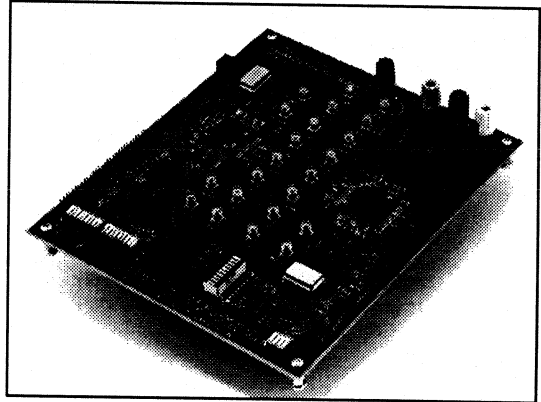
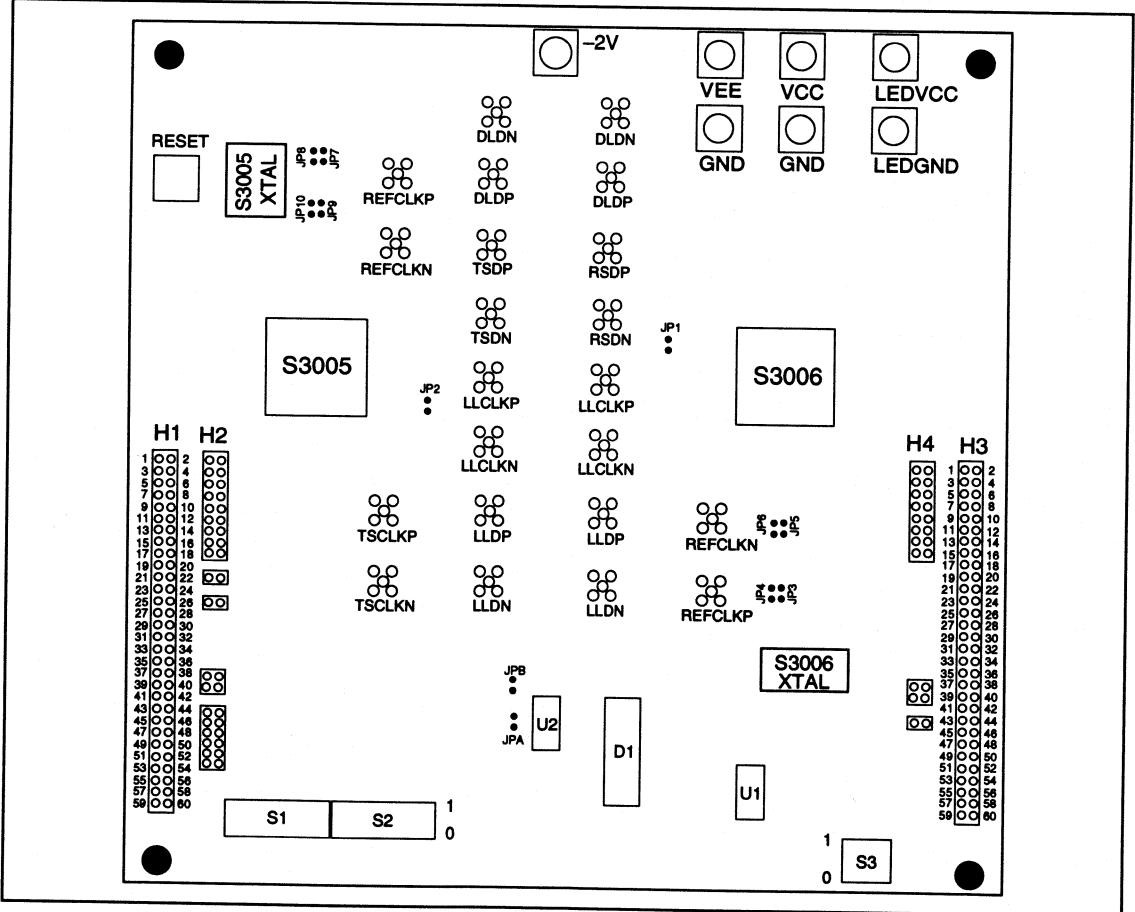


Figure 1. Board Layout



ELECTRICAL CONNECTIONS

The 60-pin header strips H1 and H3 allow simple ribbon cable connections to and from a user-provided pattern generator. Parallel data can be input to the S3005 transmitter either through the connector pins, or by using DIP switch S1. The on-board LED bank provides checks on output signals. DIP switches S1, S2, and S3 allow access to the control signals of both the S3005 and S3006 chips.

Banana jacks are provided for the power connections. Coaxial SMA connectors are used for serial data link and external reference clock connections.

Refer to Figure 1 for locations of the connectors discussed in the following sections. All connectors, controls, and jumpers are labeled on the board.

Power Connections

Power connections are made through the on-board banana jacks (VCC, VEE, GND, LEDVCC, and LEDGND). Refer to Table 1 for recommended operating conditions. A -2V connection provides proper on-board termination for the DLDP/N outputs of the S3005 when connected to the DLDP/N inputs of the S3006.

Table 1. Power Connection Recommended Operating Conditions

Power Supply	Nominal Input Voltage
VCC	5 V
Ground	0 V
VEE	-4.5 or -5.2V
LEDVCC	5 V

Table 2. H1 Pin Descriptions

Pin Names	Pin No.	Level	I/O	Description	Pin Names	Pin No.	Level	I/O	Description
GND	1	-	-	Ground	GND	31	-	-	Ground
SYNC	2	TTL	I	Synchronization Enable	PCLK	32	TTL/CMOS	O	Parallel Clock
GND	3	-	-	Ground	GND	33	-	-	Ground
REFSEL1	4	TTL	I	Reference Select 1	GND	34	-	-	Ground
GND	5	-	-	Ground	GND	35	-	-	Ground
REFSEL0	6	TTL	I	Reference Select 0	LOCKDET	36	TTL	O	Lock Detect
GND	7	-	-	Ground	GND	37	-	-	Ground
MODE2	8	TTL	I	Mode Select 2	PIN0	38	TTL	I	Parallel data input
GND	9	-	-	Ground	GND	39	-	-	Ground
MODE1	10	TTL	I	Mode Select 1	PIN1	40	TTL	I	Parallel data input
GND	11	-	-	Ground	GND	41	-	-	Ground
MODE0	12	TTL	I	Mode Select 0	GND	42	-	-	Ground
GND	13	-	-	Ground	GND	43	-	-	Ground
DLCV	14	TTL	I	Diag. Line Code Violation	PIN2	44	TTL	I	Parallel data input
GND	15	-	-	Ground	GND	45	-	-	Ground
DLEB	16	TTL	I	Diag. Loopback Enable	PIN3	46	TTL	I	Parallel data input
GND	17	-	-	Ground	GND	47	-	-	Ground
LLEB	18	TTL	I	Line Loopback Enable	PIN4	48	TTL	I	Parallel data input
GND	19	-	-	Ground	GND	49	-	-	Ground
PAE	20	TTL/CMOS	O	Phase Alignment Event	PIN5	50	TTL	I	Parallel data input
GND	21	-	-	Ground	GND	51	-	-	Ground
RSTB	22	TTL	I	Master Reset	PIN6	52	TTL	I	Parallel data input
GND	23	-	-	Ground	GND	53	-	-	Ground
BYTCLKIP	24	TTL/CMOS	O	Reference Feedback Clock	PIN7	54	TTL	I	Parallel data input
GND	25	-	-	Ground	GND	55	-	-	Ground
TESTEN	26	TTL	I	Test Clock Enable	GND	56	-	-	Ground
GND	27	-	-	Ground	GND	57	-	-	Ground
PICLK	28	TTL	I	Parallel Input Clock	GND	58	-	-	Ground
GND	29	-	-	Ground	GND	59	-	-	Ground
GND	30	-	-	Ground	GND	60	-	-	Ground

Transmitter Signals—Headers H1 and H2

Header H1 allows connection to a 60-pin ribbon cable or to single discrete cables. Controls for signals RSTB, DLEB, MODE0, and MODE1 are common to both transmitter and receiver and can be controlled via header H1. These signals can also be controlled by dipswitch S2 if H2 jumpers are installed.

Header H2 allows for DIP SWITCH control of signals SYNC, REFSEL [1:0], MODE [2:0], DLCV, DLEB, LLEB, TESTEN, and PIN[7:0]. Control of each signal will be transferred to the corresponding DIP switch S1 or S2 when the corresponding jumpers are installed on H2. (See Table 3.)

Table 3. H2 Pin Descriptions

Pin Names	Pin No.	Level	I/O	Description
SYNC	1	TTL	Input	SYNC input (pin 58) of S3005
SYNC	2	TTL	Input	DIP Switch S2 position 9
REFSEL1	3	TTL	Input	REFSEL1 input (pin 28) of S3005
REFSEL1	4	TTL	Input	DIP Switch S2 position 8
REFSEL0	5	TTL	Input	REFSEL0 input (pin 27) of S3005
REFSEL0	6	TTL	Input	DIP Switch S2 position 7
MODE2	7	TTL	Input	MODE2 input (pin 66) of S3005
MODE2	8	TTL	Input	DIP Switch S2 position 6
MODE1	9	TTL	Input	MODE1 input (pin 63) of S3005 and (pin 28) of S3006
MODE1	10	TTL	Input	DIP Switch S2 position 5
MODE0	11	TTL	Input	MODE0 input (pin 65) of S3005 and (pin 29) of S3006
MODE0	12	TTL	Input	DIP Switch S2 position 4
DLCV	13	TTL	Input	DLCV input (pin 59) of S3005
DLCV	14	TTL	Input	DIP Switch S2 position 3
DLEB	15	TTL	Input	DLEB input (pin 26) of S3005 and (pin 57) of S3006
DLEB	16	TTL	Input	DIP Switch S2 position 2
LLEB	17	TTL	Input	LLEB input (pin 57) of S3005
LLEB	18	TTL	Input	DIP Switch S2 position 1
RSTB	19	TTL	Input	RSTB input (pin 29) of S3005 and (pin 21) of S3006
RSTB	20	TTL	Input	RESET switch
TESTEN	21	TTL	Input	TESTEN input (pin 31) of S3005
TESTEN	22	TTL	Input	DIP Switch S1 position 9
PIN0	23	TTL	Input	PIN0 input (pin 14) of S3005
PIN0	24	TTL	Input	DIP Switch S1 position 8
PIN1	25	TTL	Input	PIN1 input (pin 12) of S3005
PIN1	26	TTL	Input	DIP Switch S1 position 7
PIN2	27	TTL	Input	PIN2 input (pin 10) of S3005
PIN2	28	TTL	Input	DIP Switch S1 position 6
PIN3	29	TTL	Input	PIN3 input (pin 9) of S3005
PIN3	30	TTL	Input	DIP Switch S1 position 5
PIN4	31	TTL	Input	PIN4 input (pin 8) of S3005
PIN4	32	TTL	Input	DIP Switch S1 position 4
PIN5	33	TTL	Input	PIN5 input (pin 5) of S3005
PIN5	34	TTL	Input	DIP Switch S1 position 3
PIN6	35	TTL	Input	PIN6 input (pin 3) of S3005
PIN6	36	TTL	Input	DIP Switch S1 position 2
PIN7	37	TTL	Input	PIN7 input (pin 2) of S3005
PIN7	38	TTL	Input	DIP Switch S1 position 1

Receiver Signals—Headers H3 and H4

Header H3 allows connection to a 60-pin ribbon cable or to single discrete cables. (Controls for signals RSTB, DLEB, MODE0, and MODE1 are common to both the transmitter and receiver and can be controlled via header H1. These signals can also be controlled by dipswitch S2 if H2 jumpers are installed. Mode2 is controlled via header H3. If the Mode2 jumper is installed, the Mode2 input will be low. If the Mode2 jumper is not installed, the Mode2 input will float to a high state.) When the associated pins on header H4 are jumpered, signals REFSEL[1:0] and TESTRST will be connected to DIP SWITCH S3. (See Table 3.) Without using any jumpers on these signal pins, they can be accessed directly by a 60-pin ribbon cable attached to header H3. Signal pins POUT [7:0] are always tied to LED bank D1, and can also be accessed by the same 60-pin ribbon cable by jumpering those outputs on header H4. Refer to Table 4 for pin descriptions of Header H3.

RESET

When the RSTB pins on Header H2 are shorted to each other, the push button switch on the top left of the board is connected to the S3005 and S3006 RSTB Master Reset inputs.

CRYSTAL REFERENCES AND CLOCK GENERATION

Two 19.44-MHz differential ECL crystal oscillators with 100-ppm stability are provided, one each for the transmitter and receiver. If a higher reference frequency is needed (38.88, 51.84, or 77.76 MHz), it can be selected by setting the two reference select input pins. The correct frequency is set with the REFSEL[1:0] inputs as shown in Table 6.

The output clock frequency can be 155.52 MHz (STS-3), 311.04 MHz (STS-3 CMI), or 622.08 MHz (STS-12). The output frequency is set with the MODE[2:0] inputs as shown in Table 7.

Table 4. H3 Pin Description

Pin Names	Pin No.	Level	I/O	Description	Pin Names	Pin No.	Level	I/O	Description
GND	1	-	-	Ground	GND	31	-	-	Ground
POUT0	2	TTL/CMOS	O	Parallel data output	POCLK	32	TTL/CMOS	O	Parallel Output Clock
GND	3	-	-	Ground	GND	33	-	-	Ground
POUT1	4	TTL/CMOS	O	Parallel data output	GND	34	-	-	Ground
GND	5	-	-	Ground	GND	35	-	-	Ground
POUT2	6	TTL/CMOS	O	Parallel data output	TESTEN	36	TTL	I	Test Clock Enable
GND	7	-	-	Ground	GND	37	-	-	Ground
POUT3	8	TTL/CMOS	O	Parallel data output	REFSEL1	38	TTL	I	Reference Select 1
GND	9	-	-	Ground	GND	39	-	-	Ground
POUT4	10	TTL/CMOS	O	Parallel data output	REFSEL0	40	TTL	I	Reference Select 0
GND	11	-	-	Ground	GND	41	-	-	Ground
POUT5	12	TTL/CMOS	O	Parallel data output	GND	42	-	-	Ground
GND	13	-	-	Ground	GND	43	-	-	Ground
POUT6	14	TTL/CMOS	O	Parallel data output	TESTRST	44	TTL	I	Test Reset
GND	15	-	-	Ground	GND	45	-	-	Ground
POUT7	16	TTL/CMOS	O	Parallel data output	LCV	46	TTL/CMOS	O	Line Code Violation
GND	17	-	-	Ground	GND	47	-	-	Ground
LOCKDET	18	TTL	O	Lock Detect	FP	48	TTL/CMOS	O	Frame Pulse
GND	19	-	-	Ground	GND	49	-	-	Ground
OOF	20	TTL	I	Out of Frame	-	50	-	-	-
GND	21	-	-	Ground	GND	51	-	-	Ground
LOS	22	ECL	I	Loss of Signal	-	52	-	-	-
GND	23	-	-	Ground	GND	53	-	-	Ground
MODE2	24	TTL	I	Operating Mode	-	54	-	-	-
GND	25	-	-	Ground	GND	55	-	-	Ground
-	26	-	-	-	GND	56	-	-	Ground
GND	27	-	-	Ground	GND	57	-	-	Ground
BYTCLKIP	28	TTL/CMOS	O	Ref. Feedback Clock	GND	58	-	-	Ground
GND	29	-	-	Ground	GND	59	-	-	Ground
GND	30	-	-	Ground	GND	60	-	-	Ground

To use the S3005 crystal oscillator as its reference, install jumpers on JP8 and JP10. To use an external reference clock through the S3005 REFCLKP/N SMA connector, install jumpers on JP7 and JP9. To use the S3006 crystal oscillator as its reference, install jumpers on JP3 and JP5. To use an external reference clock through the S3006 REFCLKP/N SMA connector, install jumpers on JP4 and JP6. (See Table 9, Jumpers.)

LEDs

The bank of 10 LEDs (D1) display when the S3005/S3006 chips are locked, and also light when the appropriate POUT is in the high state. The function of each LED is shown in Table 8, and is also labeled on the board.

SMA Connectors

SMA connectors provide input/output capability for a number of signals, including serial data I/O and reference clocks. These connectors are labeled on the board and are also shown in Figure 1.

Table 5. H4 Pin Description

Pin Names	Pin No.	Level	I/O	Description
POUT0	1	TTL/CMOS	Output	POUT0 output (pin 14) of S3006
POUT0	2	TTL/CMOS	Output	Connected to H3 pin 2
POUT1	3	TTL/CMOS	Output	POUT1 output (pin 12) of S3006
POUT1	4	TTL/CMOS	Output	Connected to H3 pin 4
POUT2	5	TTL/CMOS	Output	POUT2 output (pin 10) of S3006
POUT2	6	TTL/CMOS	Output	Connected to H3 pin 6
POUT3	7	TTL/CMOS	Output	POUT3 output (pin 9) of S3006
POUT3	8	TTL/CMOS	Output	Connected to H3 pin 8
POUT4	9	TTL/CMOS	Output	POUT4 output (pin 8) of S3006
POUT4	10	TTL/CMOS	Output	Connected to H3 pin 10
POUT5	11	TTL/CMOS	Output	POUT5 output (pin 5) of S3006
POUT5	12	TTL/CMOS	Output	Connected to H3 pin 12
POUT6	13	TTL/CMOS	Output	POUT6 output (pin 3) of S3006
POUT6	14	TTL/CMOS	Output	Connected to H3 pin 14
POUT7	15	TTL/CMOS	Output	POUT7 output (pin 2) of S3006
POUT7	16	TTL/CMOS	Output	Connected to H3 pin 16
REFSEL1	17	TTL	Input	Dip Switch S3 position 1
REFSEL1	18	TTL	Input	Connected to H3 pin 38
REFSEL0	19	TTL	Input	Dip Switch S3 position 2
REFSEL0	20	TTL	Input	Connected to H3 pin 40
TESTRST	21	TTL	Input	Dip Switch S3 position 3
TESTRST	22	TTL	Input	Connected to H3 pin 44

Jumpers

A number of jumpers allow the user to control various aspects of the characterization procedure. The function of each jumper is described in Table 9.

Table 6. REFSEL Settings

REFSEL1	REFSEL0	FREQUENCY
0	0	19.44 MHz
0	1	38.88 MHz
1	0	51.84 MHz
1	1	77.76 MHz

Table 7. Output Clock Frequency Settings

FREQ.	BYPASS MODE (TESTEN = 1)			NORMAL MODE (TESTEN = 0)		
	Mode2	Mode1	Mode0	Mode2	Mode1	Mode0
622.08 MHz	1	0	0	1	0	0
311.04 MHz	1	0	1	0	0	1
155.52 MHz	1	1	0	0	1	0

BIT ERROR RATE TEST PROCEDURE

The following method is commonly used to run a serial Bit Error Rate (BER) test on the S3006 device in STS-12 mode. This allows the use of a serial-out/serial-in bit error rate tester to verify the PLL frequency/phase lock capabilities and jitter tolerance testing.

1. Connect jumper wires between POUT[7:0] (H3 pins 2, 4, 6, 8, 10, 12, 14, 16) on the S3006 and PIN[7:0] (H1 pins 38, 40, 44, 46, 48, 50, 52, 54) on the S3005.
2. Connect a jumper wire between POCLK (H3 pin 32) on the S3006 and PICLK (H1 pin 28) on the S3005.
3. Connect the LLCLKP/N outputs of the S3006 to the REFCLKP/N inputs of the S3005 using SMA cables. (Be sure that jumpers JP7 and JP9 are connected and jumpers JP8 and JP10 are disconnected, as required when the S3005 REFCLKP/N SMA connectors are used for an external reference.)

4. Set TESTEN (H1 pin 26) on the S3005 High, to put the S3005 into bypass mode, which bypasses the PLL-generated clock source and enables the use of the REFCLKP/N as the bit rate clock input. (Note that in bypass mode, the frequency of the REFCLK must be appropriate for the desired data rate. Refer to the data sheet for more information.) Mode [2, 1, 0] should be 1, 0, 0 on both the S3005 and S3006.

At this point, serial data can be directed to the S3006, the parallel output data from the S3006 can be wrapped back to the parallel inputs of the S3005, and the serial outputs of the S3005 can be monitored.

Table 8. LEDs

LED	Function
D1-A	Tx LOCKDET
D1-B	Rx LOCKDET
D1-C	POUT0
D1-D	POUT1
D1-E	POUT2
D1-F	POUT3
D1-G	POUT4
D1-H	POUT5
D1-I	POUT6
D1-J	POUT7

Table 9. Jumpers

Jumper	Function
JP1	Connects S3006 op-amp power supply to enable S3006 PLL to function
JP2	Connects S3005 op-amp power supply to enable S3005 PLL to function
JP3, JP5	Connects on-board XTAL oscillator to S3006 REFCLK inputs
JP4, JP6	Connects REFCLKP/N SMA's to S3006 REFCLK inputs
JP7, JP9	Connects REFCLKP/N SMAs to S3005 REFCLK inputs
JP8, JP10	Connects on-board XTAL oscillator to S3005 REFCLK inputs
JPA, JPB	Connects S3005/S3006 LOCKDET outputs to LED

FEATURES

- Complies with ANSI, Bellcore, and CCITT specifications for jitter tolerance
- On-chip high frequency PLL with internal loop filter for clock generation or clock recovery
- Supports clock generation for STS-3/STM-1 (155.52 MHz)
- Supports clock recovery for STS-3/STM-1 (155.52 Mbit/s) or STS-12/STM-4 (622.08 Mbit/s) NRZ data
- Selectable 19.44 MHz, 51.84 MHz, or 155.52 MHz reference frequency
- Lock detect—monitors transition density and run length
- Low power
- Low-jitter ECL interface
- Small 44 PLCC or CLCC package
- TTL reference clock output

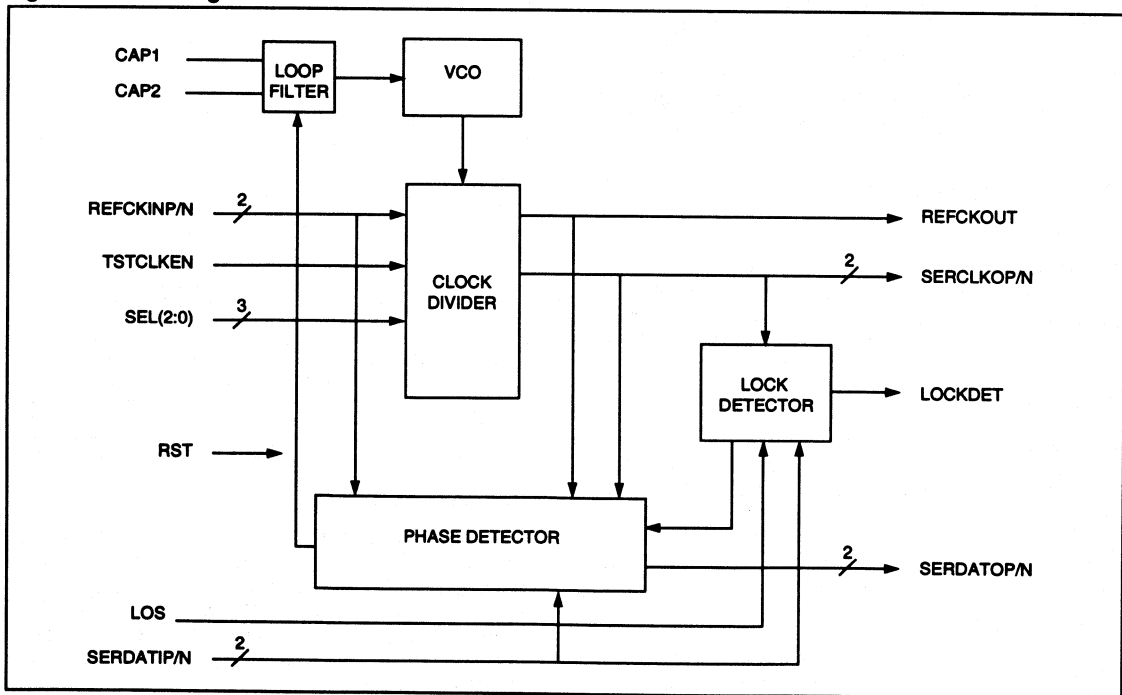
GENERAL DESCRIPTION

The function of the S3014 clock synthesis and recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S3014 is implemented using AMCC's proven Phase Locked Loop (PLL) technology.

In Clock Recovery mode, the S3014 receives either an STS-3/STM-1 or STS-12/STM-4 scrambled NRZ signal and recovers the clock from the data. The chip outputs a differential ECL bit clock and retimed data. In Clock Synthesis mode, the S3014 receives a 19.44, 51.84, or 155.52 MHz reference clock and outputs an STS-3/STM-1 or STS-12/STM-4 differential ECL clock.

The S3014 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the REFCLK input, a loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 1.

Figure 1. Block Diagram



S3014 OVERVIEW

Clock Recovery Mode

In the Clock Recovery mode, the S3014 supports clock recovery for the STS-3/STM-1 and STS-12/STM-4 rates. In this mode, ECL differential serial data is input to the chip at the rate specified by the three SEL pins, and clock recovery is performed on the incoming data stream. An external ECL differential reference clock (19.44, 51.84, or 155.52 MHz) is required to minimize the PLL lock time and provide a stable output clock source in the absence of serial input data. Retimed data and clock are output from the S3014.

Clock Synthesis Mode

In the Clock Synthesis mode, the S3014 synthesizes up to the STS-3/STM-1 and STS-12/STM-4 clock rates from either a 19.44 MHz, 51.84 MHz, or 155.52 MHz input reference frequency. STS-3/STM-1 jitter generation is compliant with the SONET/SDH requirement for 0.01 U.I. (rms) maximum, given 14.1 ps (rms) jitter on REFCLK in the 12 KHz to 1 MHz frequency band.

In this mode, a crystal oscillator is connected to the ECL differential reference input and synthesized up to the output frequency selected using the three SEL pins. The Clock Synthesis mode is recognized by the absence of data on the SERDATIP/N input pins. In this mode, tie the SERDATIP pin to ground and tie the SERDATIN pin to VTT (-2.0v) or to an ECL low level. A programmable internal divider outputs a TTL clock at the same frequency as the reference clock input via the REFCKOUT output. The lock detect output will remain consistently low in the Clock Synthesis mode.

CHARACTERISTICS

Performance

The S3014 PLL complies with the minimum jitter tolerance for clock recovery proposed for SONET/SDH equipment defined by the T1X1.6/91-022 document, when used with differential inputs and outputs as shown in Figure 2.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 2. The measurement condition is the input jitter amplitude which causes an equivalent of 1 dB power penalty.

Jitter Generation

Jitter generation is defined as the amount of jitter at the OC-N/STS-N output of a SONET equipment.

Jitter generation shall not exceed 0.01 UI rms in OC-3 mode and 0.03 UI rms in OC-12 mode when measured using a highpass filter with a 12 kHz cutoff frequency.

Serial Data Output Set-up and Hold Time

The output set-up and hold times are represented by the waveforms shown in Figure 3.

Figure 2. Input Jitter Tolerance Specification

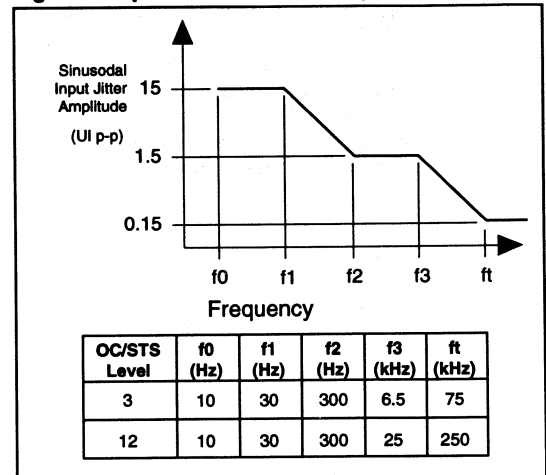
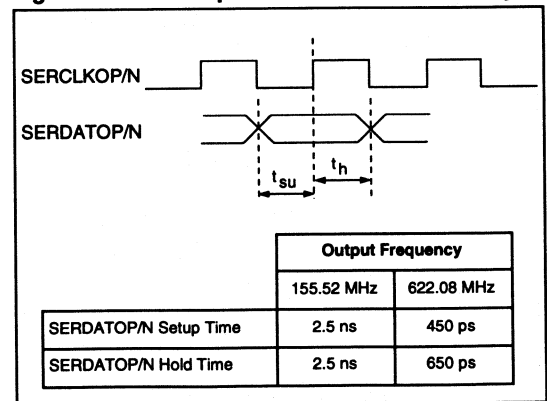


Figure 3. Clock Output to Data Transition Delay



Reference Clock Input

The required characteristics of the reference clock are outlined below. Unless otherwise noted, specifications refer to both Clock Recovery and Clock Synthesis modes of operation. While a single-ended ECL reference clock may be used, additional jitter due to edge movement related to threshold variations from DC offsets may be induced.

PIN DESCRIPTIONS

Inputs

Reference Clock [REFCKINP/N]—Differential ECL. Input used as the reference for the internal bit clock in frequency synthesis mode. Used as standby clock in the absence of data or during reset in clock recovery mode.

Serial Data In [SERDATIP/N]—Differential ECL. When the S3014 is used in the Clock Recovery mode, clock is recovered from the transitions on these inputs.

Test Clock Enable [TSTCLKEN]—TTL. Active High. Used during production test to bypass the VCO in the PLL. Tie to ground for normal operation.

Mode Select [SEL<2:0>]—TTL. Used to select output and input frequencies. Refer to Table 1 for explanation.

Reset [RST]—TTL. Active low. Initializes the device to a known state and forces the PLL to acquire to the reference clock. RST, when held low, also forces the REFCKOUT and LOCKDET outputs to the Hi-Z state. A reset of at least 16 ms should be applied at power-up and whenever it is necessary to reacquire to the reference clock. The S3014 will also reacquire to the reference clock if the serial data is held quiescent (constant ones or constant zeros) for at least 16 ms.

Loss of Signal [LOS]—ECL. Active low. A single-ended 10K ECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When LOS is low, the data on the Serial Data In (SERDATIP/N) pins will be internally forced to a constant zero, LOCKDET forced low, and the PLL forced to lock to the REFCKINP/N inputs.

This signal must be used to assure correct automatic reacquisition to serial data following an interruption and subsequent reconnection of the optical path. This will assure that the PLL does not “wander” out of reacquisition range by tracking the random phase/frequency content of the optical detector’s noise floor while monitoring “dark” fiber.

When LOS is high, data on the SERDATIP/N pins will be processed normally.

Loop Filter Capacitor [CAP1, CAP2]—The loop filter capacitor is connected to these pins. The capacitor value should be 0.1µf ±10% tolerance, X7R dielectric ceramic chip capacitor. 50 volt is recommended.

Outputs

Lock Detect [LOCKDET]—TTL. Active High. Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming datastream. LOCKDET is an asynchronous output. This output is deasserted when there is no incoming serial data input; in which case the PLL locks to the reference clock.

Serial Data Out [SERDATOP/N]—Differential ECL. In the Clock Recovery mode, this signal is the delayed version of the incoming data stream (SERDATI) updated on the falling edge of Serial Clock Out (SERCLKOP).

Serial Clock Out [SERCLKOP/N]—Differential ECL. This signal is phase aligned with Serial Data Out (SERDATO) when Lock Detect (LOCKDET) is high. When Lock Detect is low, Serial Clock Out is synchronous with Reference Clock (REFCKINP/N).

Reference Clock Out [REFCKOUT]—TTL. Single-ended TTL reference clock output. See Table 1.

Table 1. Mode Select.

SEL2	SEL1	SEL0	SERCLKO	REFCKOUT	REFCKIN
0	0	0	622.08 MHz	51.84 MHz	51.84 MHz
0	0	1	622.08 MHz	19.44 MHz	19.44 MHz
0	1	0	622.08 MHz	19.44 MHz	19.44 MHz
0	1	1	622.08 MHz	—	155.52 MHz
1	0	0	155.52 MHz	51.84 MHz	51.84 MHz
1	0	1	155.52 MHz	19.44 MHz	19.44 MHz

Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	Given REFCLK = SERCLK + 4, 12 or SERCLK + 32 per SEL <2:0> settings
Clock Synthesis Output Jitter OC-3/STS-3 OC-12/STS-12 ¹		.005 .015	.01 64 .03 48	UI(rms) ps (rms) UI(rms) ps (rms)	In CSU mode, given : • 56ps rms jitter on REFCLK in 12 KHz to 1 MHz band • 14.1 ps rms jitter on REFCLK in 12 KHz to 1 MHz band
Clock Recovery Output Jitter			.01	UI(rms)	rms jitter, in lock
Reference Clock Frequency Tolerance ^{2,3} Clock Synthesis Clock Recovery	-20 -100		20 100	ppm ppm	Required to meet SONET output frequency specification
OC-3/STS-3 OC-12/STS-12 Capture Range Lock Range Clock Output Duty Cycle		±200 +8,-12		ppm % %	With respect to fixed reference frequency Minimum transition density of 20%
Acquisition Lock Time ³ OC-3/STS-3 OC-12/STS-12			64 16	µsec	With device already powered up and valid REFCLK.
Reference Clock Input Duty Cycle	30		70	% of period	
Reference Clock Rise & Fall Times			2.0	ns	10% to 90% of amplitude
ECL Output Rise & Fall Times			850	ps	10% to 90%, 50Ω to -2V equivalent load, 5 pf cap

- 1 These specs can be achieved with either a 51.84 MHz or a 155.52 MHz Reference Clock.
- 2 Noise on REFCLK should be less than 14.1 ps rms in a jitter frequency band from 12 KHz to 1 MHz.
- 3 Specifications based on design values. Not tested.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature under Bias (industrial)	-40		85	°C
Ambient Temperature under Bias (commercial)	0		70	°C
Junction Temperature under Bias	-10		130	°C
Voltage on VCC with Respect to GND	4.75	5.0	5.25	V
Voltage on VEE with Respect to GND	-4.2	-4.5/-5.2	-5.46	V
Voltage on Any TTL Input Pin	0.0		VCC	V
Voltage on Any ECL Input Pin	-2.0		0	V
TTL/CMOS Output Sink Current			8	mA
TTL/CMOS Output Source Current			1	mA
ECL Output Source Current (50Ω to -2V)		14	25	mA
Supply Current	ICC		10	mA
	IEE		170	mA

V_{EE} (min) = -4.2V for Ambient Temperature ≥ 0°C, -4.5V for Ambient Temperature < 0°C.

Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Respect to GND	-0.5		7.0	V
Voltage on VEE with Respect to GND	-8.0		0.5	V
Voltage on Any TTL Input Pin	-0.5		+5.5	V
Voltage on Any ECL Input Pin	-3.0		0.0	V
TTL Output Sink Current			20	mA
TTL Output Source Current			10	mA
High Speed ECL Output Source Current			50	mA
Static Discharge Voltage		500		V

TTL Input/Output DC Characteristics¹

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{EE} = -4.5\text{ V} \pm 7\%$ or $-5.2 \pm 5\%$)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{IL}^2	Input LOW Voltage	Guaranteed Input LOW Voltage for all inputs		0.8	Volts
V_{IH}^2	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all inputs	2.0		Volts
I_{IL}	Input LOW Current	$V_{CC} = \text{MAX}$, $V_{IN} = 0.5\text{V}$	-400.0		μA
I_{IH}	Input HIGH Current	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7\text{V}$		50.0	μA
I_I	Input HIGH Current at Max VCC	$V_{CC} = \text{MAX}$, $V_{IN} = 5.25\text{V}$		1.0	mA
I_{OS}	Output Short Circuit Current	$V_{CC} = \text{MAX}$, $V_{OUT} = 0.5\text{V}$	-100.0	-25.0	mA
V_{IK}	Input Clamp Diode Voltage	$V_{CC} = \text{MIN}$, $I_{IN} = -18.0\text{mA}$	-1.2		Volts
V_{OL}	TTL Output LOW Voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 8\text{mA}$		0.5	Volts
V_{OH}	TTL Output HIGH Voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -1.0\text{mA}$	2.4		Volts

1. These conditions will be met with an airflow of 400 LFPM.
2. These input levels provide a zero-noise immunity and should only be tested in a static, noise-free environment.

ECL Input/Output DC Characteristics³

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{EE} = -4.5\text{ V} \pm 7\%$ or $-5.2 \pm 5\%$)

Symbol	Parameter	Test Conditions	Signal Name	Min	Max	Unit
V_{IL}^1	Input LOW Voltage	Guaranteed Input LOW Voltage for all single ended inputs		-2.00	-1.47	Volts
V_{IH}^1	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all single ended inputs		-1.18	-0.80	Volts
V_{IL}^2	Input LOW Voltage	Guaranteed Input LOW Voltage for all differential inputs		-2.00	-0.70	Volts
V_{IH}^2	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all differential inputs		-1.75	-0.45	Volts
$V_{ID}^{2,4}$	Input DIFF Voltage	Guaranteed Input DIFF Voltage for all differential inputs		0.25	1.40	Volts
I_{IL}	Input LOW Current	$V_{EE} = \text{MAX}$, $V_{IL} = -1.95\text{V}$	LOS	-0.50	20.00	μA
		$V_{EE} = \text{MAX}$, $V_{DIFF} = 0.5\text{V}$	SERDATIP, SERDATIN, REFCLKP, REFCLKN	-1.0	20.00	μA
I_{IH}	Input HIGH Current	$V_{EE} = \text{MAX}$, $V_{IH} = -0.80\text{V}$	LOS	-0.50	20.00	μA
		$V_{EE} = \text{MAX}$, $V_{DIFF} = 0.5\text{V}$	SERDATIP, SERDATIN, REFCLKP, REFCLKN	-1.0	20.00	μA
V_{OL}	Output LOW Voltage	50 Ω to -2V termination		-2.00	-1.50	Volts
V_{OH}	Output HIGH Voltage	50 Ω to -2V termination		-1.11	-0.62	Volts

1. Single Ended Inputs
2. Differential ECL Inputs
3. These conditions will be met with an airflow of 400 LFPM.
4. When not used, tie the negative differential input to ground (0V), and tie the positive differential input to -2.0V.

Figure 4. Differential ECL Input and Output Applications

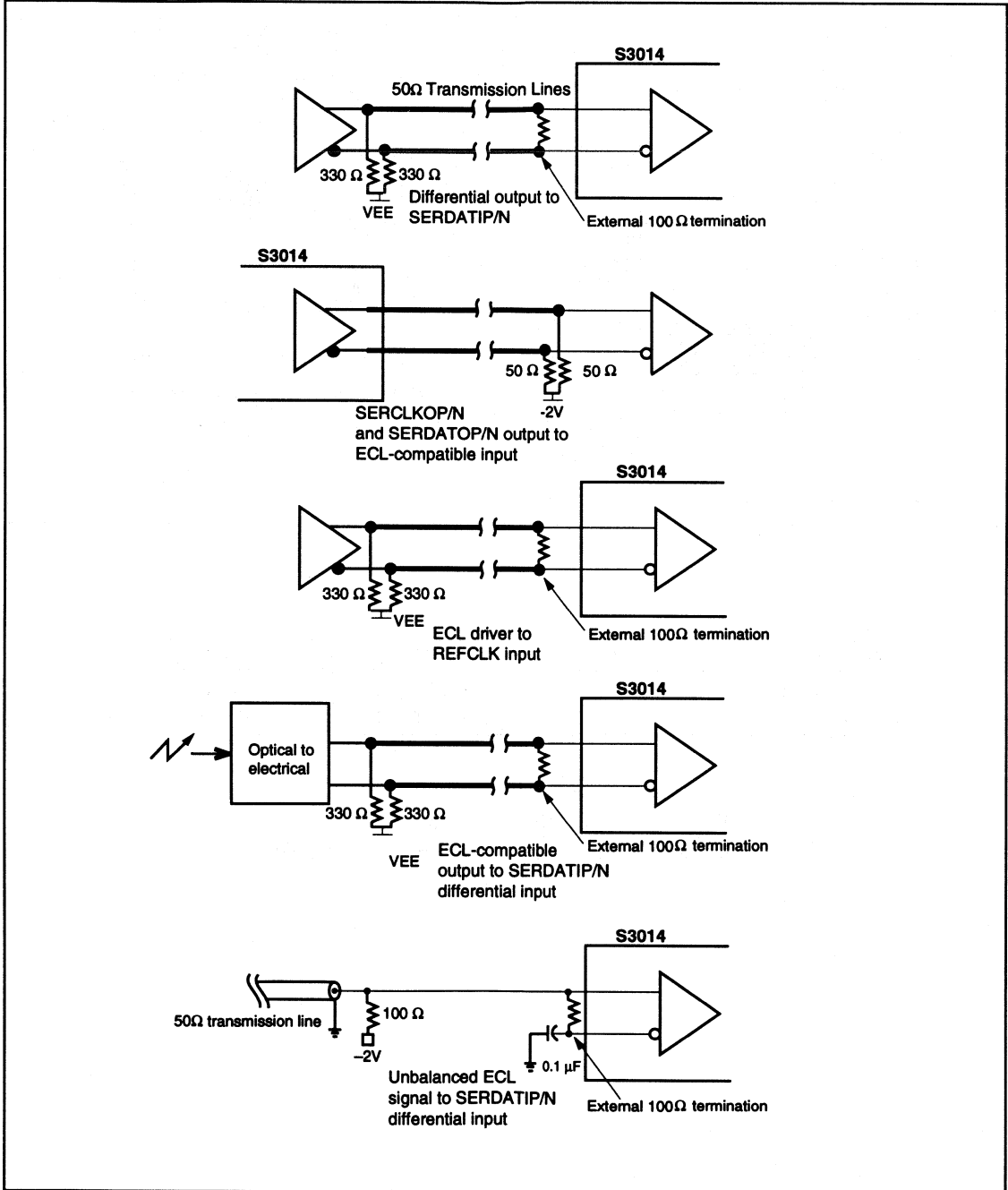
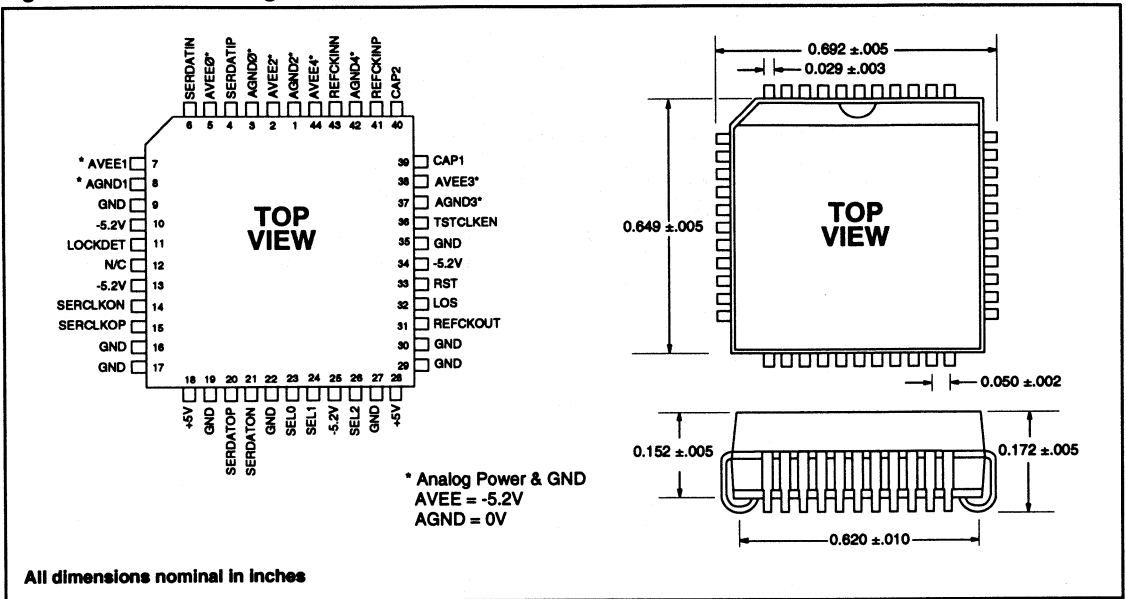


Figure 5. 44 PLCC Package and Pinout



Ordering Information

GRADE	PART	PACKAGE	SPEED GRADE
S-commercial/ Industrial	3014	A-44 PLCC D-44 PLCC TEP	1 – 155 Mbit/s 6 – 622 Mbit/s

X
Grade

XXXX
Part number

X
Package

- X
Speed Grade

EVALUATION BOARD DESCRIPTION

The S6003 Evaluation Board allows demonstration of AMCC's S3014 SONET clock synthesis and recovery unit. This data sheet provides information on board contents and layout. It should be used in conjunction with the S3014 data sheet, which contains full technical details on chip operation.

Figure 1 depicts the layout of the evaluation board, showing the location of connectors and components. Power is supplied to the board from external raw supplies connected through the on-board power connections. Coaxial SMA connectors are used for serial data link and external reference clock connections.

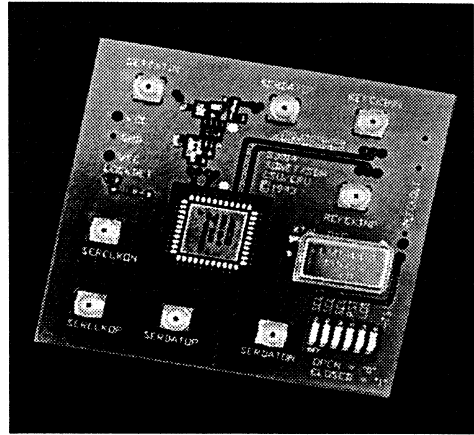
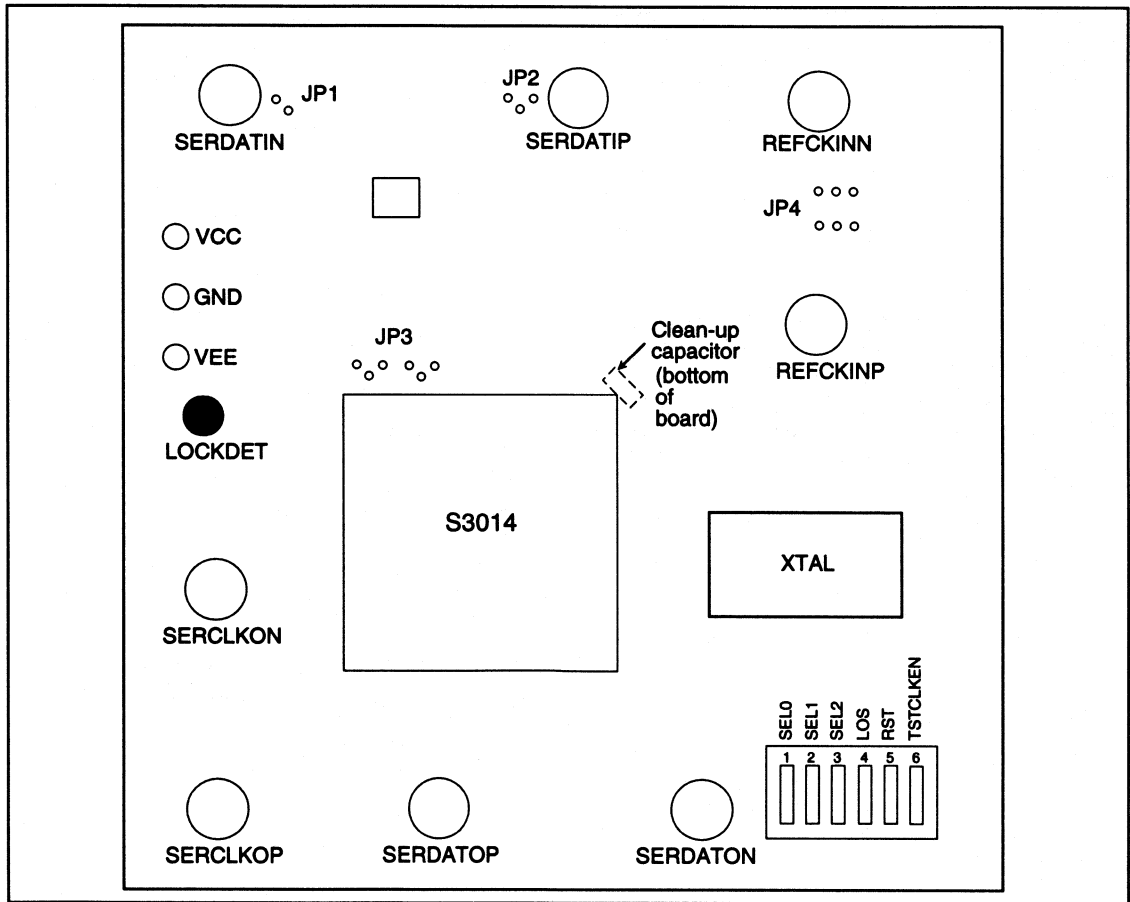


Figure 1. S6003 Board Layout



ELECTRICAL CONNECTIONS

Power Connections

Connections are provided on the board for ground, the TTL power supply (VCC), and the core and PLL supply (VEE). Refer to Table 1 for recommended operating conditions.

Table 1. Power Connection Recommended Operating Conditions

Power Supply	Nominal Input Voltage	Function
VCC	5 V	TTL Supply
Ground	0 V	
VEE	-5 V	PLL & Core Supply

SMA Connectors

Eight coaxial SMA connectors are provided for the differential serial data signals and the clock input/output signals. All connectors, components, and controls are labeled on the board by name. (See Figure 1 for locations.)

Serial Data In [SERDATIP/N]. Differential ECL. When the S3014 is used in the Clock Recovery Mode, the clock is recovered from the transitions on these inputs.

Reference Clock [REFCKINP/N]. Differential ECL. Input used as the reference for the internal bit clock frequency synthesizer.

Serial Clock Out [SERCLKOP/N]. Differential ECL. Output signal that is phase-aligned with Serial Data Out in the Clock Recovery Mode.

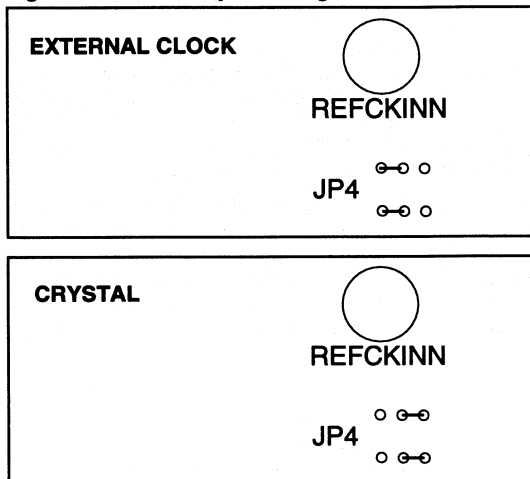
Serial Data Out [SERDATOP/N]. Differential ECL. In the Clock Recovery Mode, this signal is the delayed version of the incoming data stream, phase aligned with Serial Clock Out.

Note: All ECL outputs must be terminated 50Ω to -2V off-chip. When connecting the serial clock and serial data outputs to test equipment with a 50Ω to GND termination, an ECL terminator should be used to match the 50Ω to -2V termination requirement of the S6003 with the 50Ω to GND termination of the test equipment.

CRYSTAL REFERENCES

A 19.44, 51.84, or 155.52 MHz differential ECL crystal oscillator can be used for the reference clock. One 19.44 MHz crystal is provided. If a different reference frequency is needed, AMCC can recommend crystal vendors.

Figure 2. Clock Jumper Configurations



Alternatively, an external reference clock can be provided by configuring the JP4 jumpers located between the REFCKINN and REFCKINP connectors as shown in Figure 2, and connecting a differential clock to the appropriate SMA connectors.

The desired input frequency is selected using the SEL0 and SEL1 switches (see Table 2).

LED

The single on-board LED provides a display for the Lock Detect signal. This Active High TTL output is a clock recovery indicator. It is set high when the internal clock recovery circuitry has locked onto the incoming data stream.

DIP SWITCH

An on-board DIP switch provides control capability. The switch functions are described in the following sections.

SEL[1:0]. Mode select. TTL. These two switches are used to select the input (reference clock) frequencies, as shown in Table 2.

Table 2. SEL[1:0] Switch Function

SEL1	SEL0	INPUT FREQ
0	0	51.84 MHz
1	0	19.44 MHz
0	1	19.44 MHz
1	1	155.32 MHz

SEL2. Mode Select. TTL. This switch sets the output frequencies, as shown in Table 3.

Table 3. SEL2 Switch Function

SEL2	OUTPUT FREQ
0	622.08 MHz
1	155.52 MHz

RST. Reset. TTL. Active Low. Initializes the S3014 to a known state and forces the PLL to acquire to the reference clock.

TSTCLKEN. Test Clock Enable. TTL. Active High. Used to bypass the VCO in the PLL.

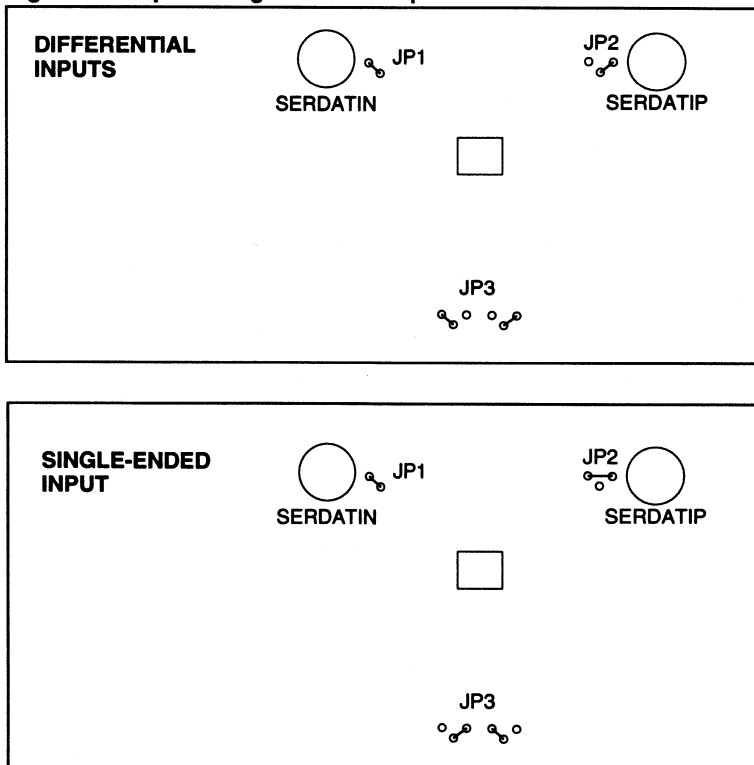
LOS. Loss of Signal. ECL. When this switch is set Low (0), the S3014 is locked to the reference clock. When it is set High (1), the S3014 is locked to data and data is processed normally.

JUMPER CONFIGURATION

The jumpers labeled JP4 in Figure 1 allow the user to control whether an onboard crystal reference or external clock reference is used (see Crystal References, Fig. 2).

In addition, the jumpers labeled JP1, JP2, and JP3 in Figure 1 must be properly configured for differential or single-ended data inputs. When providing single-ended data into the SERDATIP SMA connector, an on-board single-ended to differential converter provides clean full swing ECL levels to the S3014 device. Jumper configuration options are shown in Figure 3.

Figure 3. Jumper Configurations for Inputs



FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLL for clock generation and clock recovery
- On-chip analog circuitry for transformer driver and equalization
- Supports 139.264 Mbit/s (E4) and 155.52 Mbit/s (OC-3) transmission rates
- Supports 139.264 Mbit/s and 155.52 Mbit/s Coded Mark Inversion (CMI) interfaces
- Reference frequencies of 19.44 (OC-3) or 17.408 MHz (E4)
- Interface to both PECL and TTL logic
- Lock detect on clock recovery device
- Low jitter PECL interface
- 1.6W total typ power
- +5V only power supply
- Small 52 PQFP TEP package
- Supports both electrical and optical interfaces

APPLICATIONS

- ATM over SONET
- OC-3/STM-1 or E4-based transmission systems
- OC-3/STM-1 or E4 modules
- OC-3/STM-1 or E4 test equipment
- Section repeaters
- Add drop multiplexors
- Broadband cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3015 transmitter and S3016 receiver derive high speed timing signals for SONET/SDH or PDH-based equipment. These circuits are implemented using AMCC's proven Phase Locked Loop (PLL) technology. Figures 1a and 1b show typical network applications.

The S3015 and S3016 each have an on-chip VCO which can be synchronized directly to the incoming data stream. The chipset can be used with a 19.44 MHz reference clock when operated in the SONET/SDH OC-3 mode. In E4 mode the chipset can be operated with a 17.408 MHz reference clock in support of existing system clocking schemes. On-chip coded-mark-inversion (CMI) encoding and decoding is provided for 139.264 Mbit/s and 155.52 Mbit/s interfaces.

The low jitter PECL interface guarantees compliance with the bit-error rate requirements of the Bellcore, ANSI, and ITU-T standards. The S3015/S3016 chipset is packaged in a .65mm pitch, compact 52-pin PQFP, offering designers a small package outline.

The S3015 and S3016 provide the major components on-chip for a coaxial cable interface, including analog transformer driver circuitry and equalization interface circuitry.

Figure 1a. Electrical Interface

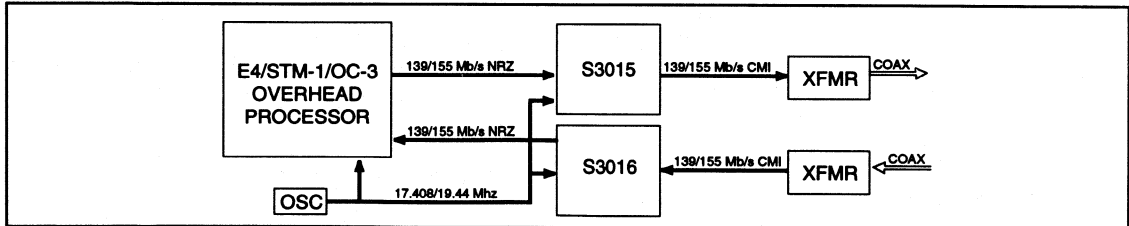
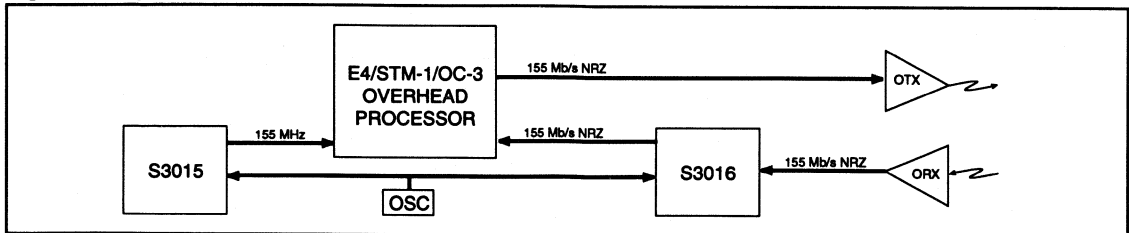


Figure 1b. Optical Interface



SONET/SDH OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, form a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for

transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3015/S3016 chipset supports OC-3 rates (155.52 Mbit/s).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-3 consists of nine transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 9 overhead and 261 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3)

For more details on SONET operations, refer to the ANSI SONET standard document.

Table 1. SONET Signal Hierarchy

Elec.	ITU-T	Optical	Data Rate (Mbit/s)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24		OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 2. SONET Structure

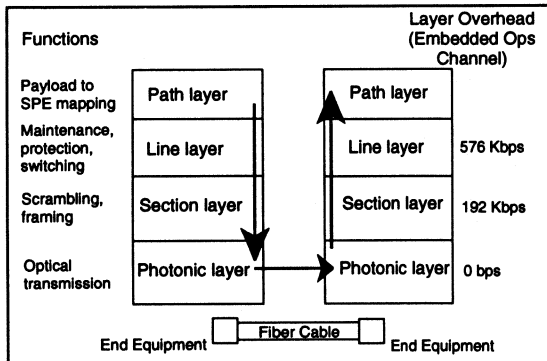
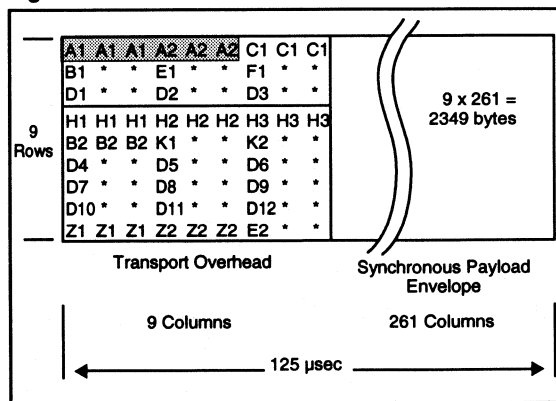


Figure 3. STS-3/OC-3 Frame Format



S3015/S3016 OVERVIEW

The S3015 transmitter and the S3016 receiver can be used to implement the front end of STS-3, OC-3 or E4 equipment. The block diagrams in Figures 4 and 11 show the basic operation of both chips.

When serial data is present at the input of the transmitter, the S3015 VCO synchronizes directly to the incoming data, which is retimed for the purpose of optional CMI encoding. In the absence of incoming serial data, the S3015 operates as a clock synthesizer. In this mode, a crystal oscillator is connected to the TTL reference input and synthesized up to the 155 MHz output frequency. The S3016 receiver performs clock recovery by synchronizing its on-chip VCO directly to the incoming data stream.

The S3015 provides a PECL output for an optical interface and two transformer driver outputs for an electrical interface. One of these drivers is a monitor output. The S3016 provides a PECL input for an optical interface and an analog input for an electrical interface.

When the chipset is used in an electrical interface, the PECL output of the transmitter can be connected to the PECL input of the receiver to implement a diagnostic loopback mode for test. When the chipset is used in an optical interface, a transformer driver output of the transmitter can be connected to the analog input of the receiver to implement the loopback mode.

S3015 TRANSMITTER ARCHITECTURE/FUNCTIONAL DESIGN

The S3015 transmitter chip performs the last stage of digital processing of a transmit SONET STS-3 or ITU-T E4 bit serial data stream. A Coded Mark Inversion (CMI) encoder can be enabled for encoding STS-3 electrical and E4 signals.

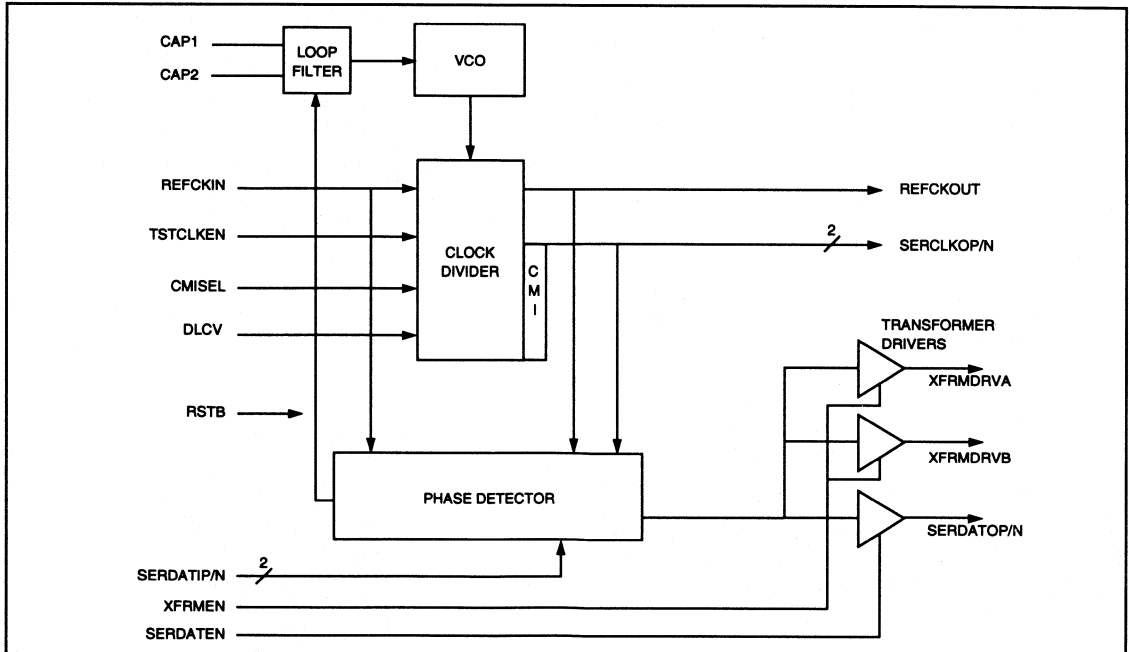
Clock Recovery

If serial data is present on the SERDATIP/N inputs, the clock is recovered from the serial data stream at 139.264 MHz or 155.52 MHz and synthesized to 278.528 MHz or 311.04 MHz to CMI encode the incoming data.

Optical and Electrical Interfaces

The digital data outputs (SERDATOP/N) are the PECL outputs for an optical interface and are to be connected to an electrical to optical converter, as shown in Figure 19. This data is also routed to two on-chip transformer drivers and sent out on XFRMDRVA and XFRMDRVB to drive the transformers of the electrical interface, as shown in Figure 20. These outputs are shut off when the reset is active, XFRMEN is active, or when the chip is in NRZ mode and the data inputs are in the logic zero state. The electrical characteristics for the transformer drivers are shown in Table 5.

Figure 4. S3015 OC3/STM-1/E4 Transmitter

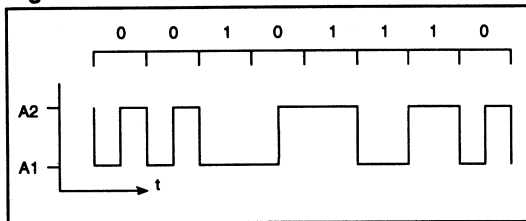


CMI Encoding

Coded Mark Inversion format (CMI) ensures at least one data transition per 1.5 bit periods, thus aiding the clock recovery process. Zeros are represented by a Low state for one half a bit period, followed by a High state for the rest of that bit period. Ones are represented by a steady Low or High state for a full bit period. The state of the ones bit period alternates at each occurrence of a one. Figure 5 shows an example of CMI-encoded data. The STS-3 electrical interface and the E4 interface are specified to have CMI-encoded data.

The CMI encoder on the S3015 accepts serial data from SERDATIP/N at 139.264 or 155.52 Mb/s. The data is then encoded into CMI format, and the result is shifted out with transitions at twice the basic data rate. The CMISEL input controls whether the CMI encoder is in the data path. A CMI code violation can be inserted for diagnostic purposes by activating the DLCV input. The DLCV input is sampled on every cycle of the serial clock to allow a single or multiple line code violations to be inserted. This violation is either an inverted zero code or an inversion of the alternating ones logic level, depending on the state of the data. Subsequent one codes take into account the induced violation to avoid error multiplication.

Figure 5. CMI Encoded Data



Jitter Generation

Jitter Generation is defined as the amount of jitter at the OC-3 or E-4 output of equipment. Jitter generation for OC-3 shall not exceed 0.01 UI rms when measured using a highpass filter with a 12 kHz cutoff frequency.

For STM-1 and E4, the jitter generated shall not exceed the specifications shown in Figure 6.

In order to meet the SONET, STM-1 E4 jitter specifications as shown in Figure 6, the SERDATIP/N serial data input must meet the jitter characteristics as shown in Figure 8. The jitter transfer characteristics of the S3015 SERDATIP/N to SERDATOP/N or XFRMDRVA/B are shown in Figure 7.

Figure 6. Jitter Generation Specifications Compliant to G.823 and G.825

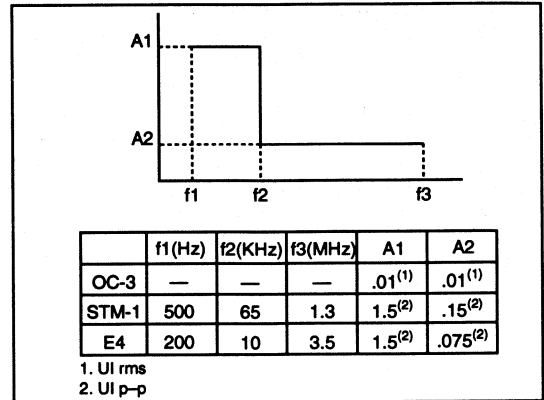


Figure 7. Jitter Transfer Characteristics

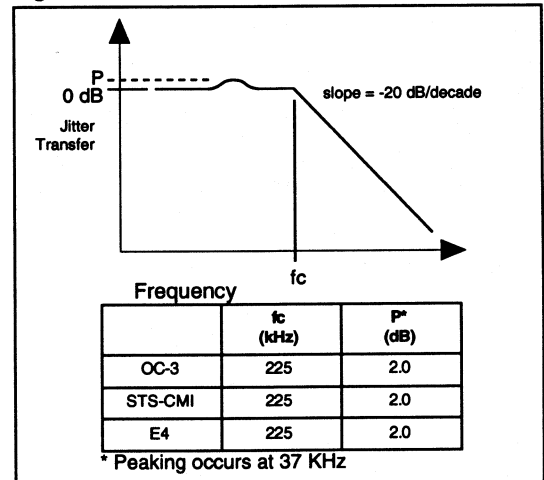


Figure 8. S3015 Maximum Allowable Input Jitter

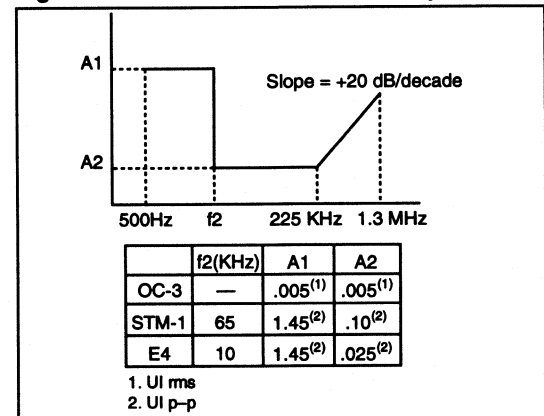


Figure 9. Mask of a pulse corresponding to a binary 0 Compliant to G.703

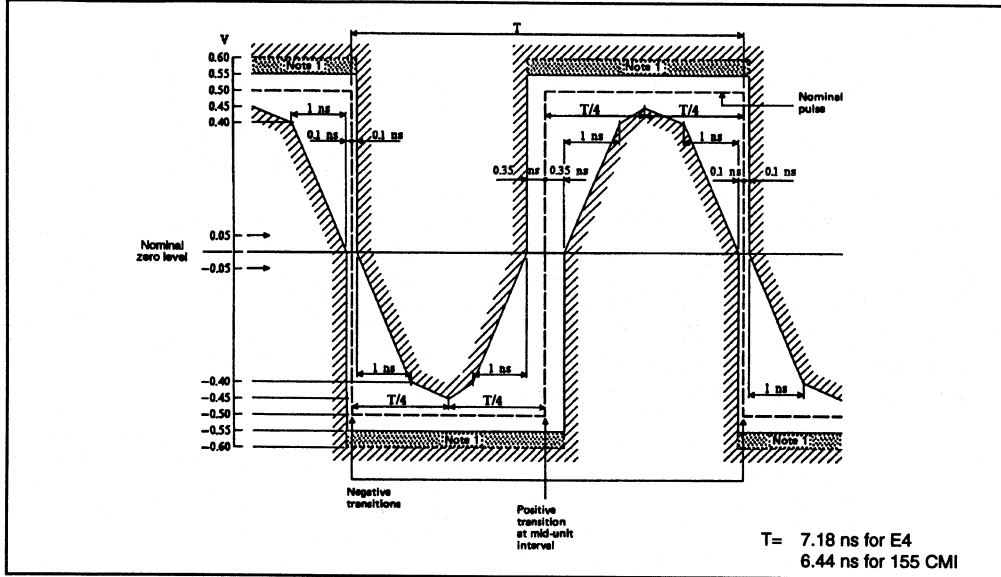
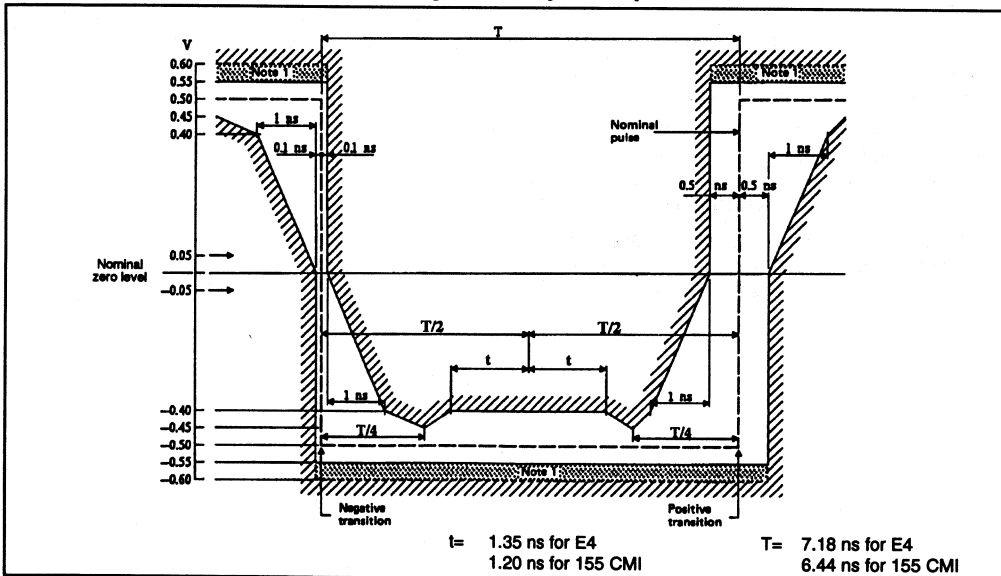


Figure 10. Mask of a pulse corresponding to a binary 1 Compliant to G.703



Notes:

1. The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.
2. For the purpose of these masks, the rise time and decay time should be measured between -0.4 V and 0.4 V, and should not exceed 2 ns.
3. The inverse pulse in Figure 10 will have the same characteristics, noting that the timing tolerances at the zero level of the negative and positive transitions are $\pm 0.1 \text{ ns}$ and $\pm 0.5 \text{ ns}$ respectively.

TRANSMITTER PIN DESCRIPTIONS

Input Signals

Reference clock [REFCKIN]—TTL. Input used as the reference for the internal bit clock frequency synthesizer.

Test Clock Enable [TSTCLKEN]—TTL. Active High. Enables the reference clock to be used in place of the VCO for testing. Allows a means of testing the functions of the chip without the use of the PLL.

Diagnostic Line Code Violation [DLCV]—Single-ended PECL. Set high to force a CMI line code violation. DLCV is only active in CMI mode. DLCV is sampled on the falling edge of SERCLKOP.

CMI Select [CMISEL]—TTL. Used to select CMI or NRZ. A logic high selects CMI mode. A logic low selects NRZ mode. Both the SERDATOP/N and the XFRMDRV outputs are controlled by CMISEL.

Reset [RSTB]—TTL. Active low. Initializes the device to a known state. When active, all data outputs are held low. Clock outputs are still active during reset.

Loop Filter Capacitor [CAP1, CAP2]—The loop filter capacitor is connected to these pins. The capacitor value should be $0.1\mu\text{f} \pm 10\%$ tolerance, X7R dielectric, 50 volt rating is recommended.

Serial Data In [SERDATIP/N]—Differential PECL. The clock is recovered from transitions on these inputs. No phase relationship to REFCKIN is required.

Transformer Driver Enable [XFRMEN]—TTL. Used to enable the transformer driver outputs. A logic low enables XFRMDRVA and XFRMDRVB. A logic high turns off the transformer driver outputs.

Serial Data Enable [SERDATEN]—TTL. Used to enable the serial data outputs. A logic low enables SERDATOP/N. A logic high turns off the serial data outputs.

Output Signals

Serial Data Out [SERDATOP/N]—Differential PECL. In NRZ mode, this signal is the delayed version of the incoming data stream (SERDATIP/N) updated on the falling edge of Serial Clock Out (SERCLKOP).

In CMI mode, this signal is the CMI-encoded version of SERDATIP/N.

Serial Clock Out [SERCLKOP/N]—Differential PECL. This signal is a 155 MHz clock that is phase-aligned with Serial Data Out (SERDATO) in NRZ mode.

In CMI mode, SERCLKOP/N cannot be used.

Reference Clock Out [REFCKOUT]—TTL. Single-ended TTL reference clock output.

Transformer Driver A [XFRMDRVA]—Analog. Used to drive the transformer of the electrical interface. For E4 operation this output should be connected per Figure 20 to provide the correct G.703 compatible output levels from the transformer when connected to the specified 75Ω cable.

Transformer Driver B [XFRMDRVB]—Analog. Used to drive the monitor transformer of the electrical interface. This output should be connected per Figure 20 to provide the correct output levels from the transformer when connected to the specified 75Ω cable.

S3016 RECEIVER ARCHITECTURAL/FUNCTIONAL DESIGN

The S3016 receiver provides the first stage of digital processing of a receive SONET STS-3 or ITU-T E4 serial bit stream. A Coded Mark Inversion (CMI) decoder can be enabled for decoding STS-3 electrical and E4 signals.

Clock recovery is performed on the incoming scrambled NRZ or CMI-coded data stream. A reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference frequency to the nominal bit rate.

Clock Recovery

The Clock Recovery function, as shown in the block diagram in Figure 11, generates a clock that is frequency matched to the incoming data baud rate at the SERDATIP/N differential inputs. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are

smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock. Frequency stability without incoming data is guaranteed by an alternate reference input (REFCKIN) to which the PLL locks when data is lost.

When the test clock enable (TSTCLKEN) input is set high, the clock recovery block is disabled. The reference clock (REFCKIN) is used as the bit rate clock input in place of the recovered clock. This feature is used for functional testing of the device.

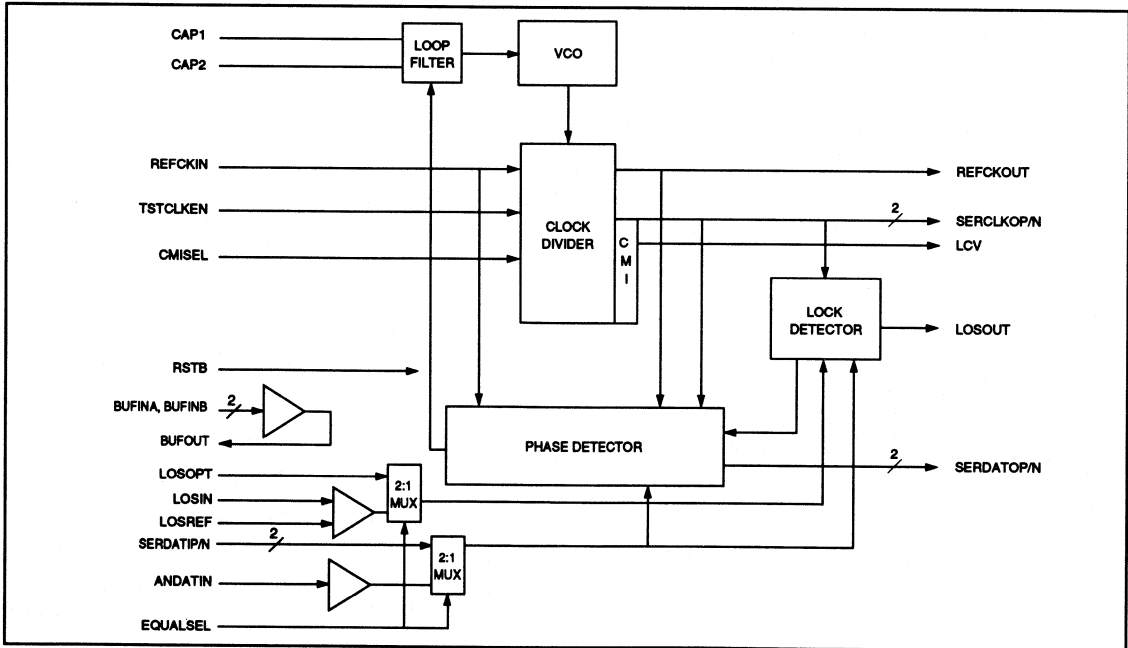
The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET or E4 data signal. This transfer function yields a typical capture time of 16 μ s for random incoming NRZ data.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for OC-3/STM-1/E4 equipment by the Bellcore and ITU-T documents, shown in Figure 14.

Optical and Electrical Interfaces

The digital data inputs (SERDATIP/N) are the PECL inputs from an optical to electrical converter, as shown in Figure 17. The data input for the coaxial interface is ANDATIN, which is the serial data input from the equalizer circuit and should be connected as shown in Figure 18. The EQUALSEL input is used to select either SERDATIP/N or ANDATIN.

Figure 11. S3016 OC-3/STM-1/E4 Receiver



CMI Decoding

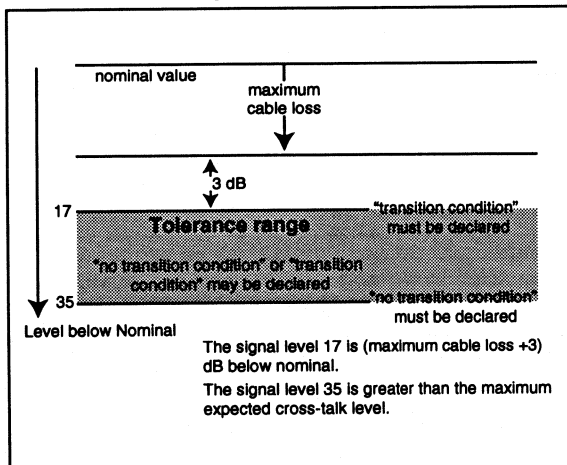
The CMI decoder block on the S3016 accepts serial data from the SERDATIP/N input at the rate of 139.264 or 155.52 Mb/s. The incoming CMI data, which has transitions that represent this data rate (the clock associated with this data would be running at twice this rate), is then decoded from CMI to NRZ format.

Loss of Signal

The clock recovery circuit monitors the incoming data stream for loss of signal. If the incoming encoded data stream has had no transitions continuously for 96 to 224 recovered clock cycles, loss of signal is declared and the PLL will switch from locking onto the incoming data to locking onto the reference clock per the requirements of G.775. Alternatively, the loss of signal (LOSIN) input can force a loss-of-signal condition. This signal is compared internally against the LOSREF input reference voltage. This input can be set to meet the conditions shown in Figure 12. If the zero to peak signal level drops below the LOSREF/20 voltage level for more than 96 to 224 bit intervals, a loss of signal condition will be indicated on the LOSOUT pin and the PLL will change its reference from the serial data stream to the reference clock. When the peak input voltage is greater than LOSREF/10, the loss of signal condition will be deasserted and the PLL will recover the clock from the serial data inputs.

In NRZ mode, a logic low level on the LOSOPT input will cause the PLL to change its reference to the reference clock. This pin should be driven by a PECL compatible level signal detect signal from the fiber optic receiver.

Figure 12. Criteria for determination of transition conditions. Compliant to G.775.



Serial Clock Output to Data Output Timing

The serial data is clocked out on the falling edge of SERCLKOP. (See Figure 13.) This timing is valid in both NRZ and CMI modes.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. OC-3 and E-4 input jitter tolerance requirements are shown in Figure 14.

The S3016 PLL complies with the minimum jitter tolerance for clock recovery proposed for SONET/SDH equipment defined by the Bellcore TA-NWT-000253 standard when used as shown in Figure 17. The S3016 PLL also complies with the minimum jitter tolerance for clock recovery as defined in the ITU-T E4 specification when used as shown in Figure 18.

Reference Clock Input

The reference clock input seen in Figure 11 provides backup reference clock signals to the clock recovery block when the clock recovery block detects a loss of signal condition. It contains a counter that divides the clock output from the clock recovery block down to the same frequency as the reference clock REFCKIN.

Figure 13. S3016 Clock to Data Timing

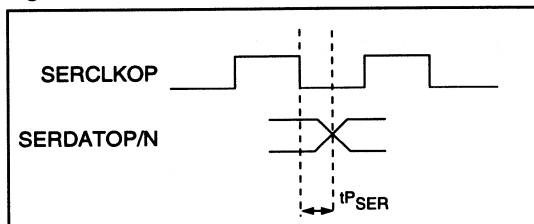
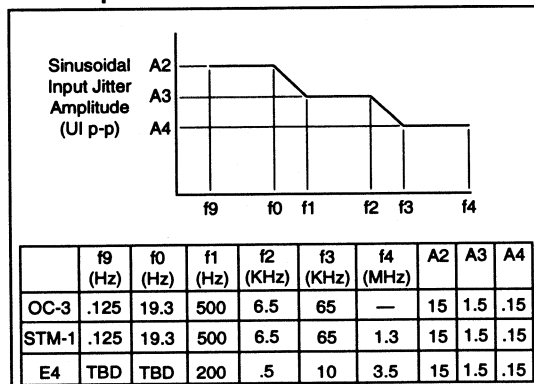


Figure 14. Clock Recovery Jitter Tolerance Compliant to G.823 and G.825



S3016 RECEIVER PIN DESCRIPTIONS

Input Signals

Buffer Inputs [BUFINA, BUFINB]—Analog. Inputs to the equalizer network buffer circuit. This circuit provides a high impedance load to the transformer termination network in order to comply with the required return loss specifications. These pins should be connected as shown in Figure 18. These pins are electrically equivalent.

Analog Data In [ANDATIN]—Analog. This is the serial data input from the equalizer circuit. It must be connected to the output of the equalizer circuit as shown in Figure 18. When the S3016 is used with a fiber optic receiver this input should be left open and the SERDATIP/N inputs should be used.

Equalization Select [EQUALSEL]—TTL. Used to select SERDATIP/N or ANDATIN. A logic high selects ANDATIN.

Reference Clock [REFCKIN]—Single-ended TTL. Input used as the reference for the VCO when the input data signal is lost.

Serial Data In [SERDATIP/N]—Differential PECL. Clock is recovered from transitions on these inputs when selected by EQUALSEL.

Test Clock Enable [TSTCLKEN]—TTL. Active High. Enables the reference clock to be used in place of the VCO for testing. Allows a means of testing the functions of the chip without the use of the PLL.

CMI Select [CMISEL]—TTL. Used to select CMI or NRZ. A logic high selects CMI mode. Either ANDATIN or SERDATIN may be used as inputs to the CMI decoder.

Reset [RSTB]—TTL. Active Low. Initializes the device to a known state, shuts off SERCLKOP/N, and forces the PLL to acquire to the reference clock. A reset of at least 16 ms should be applied at power-up and whenever it is necessary to reacquire to the reference clock. The S3016 will also reacquire to the reference clock if the serial data is held quiescent (constant ones or constant zeros) or LOSIN or LOSOPT are activated for at least 224 bit intervals.

Loss of Signal In [LOSIN]—Analog. A single-ended input that indicates a loss of received signal. When the signal level at LOSIN drops below the voltage level set by LOSREF for greater than 96 to 224 bit intervals, the data on Serial Data Out (SERDATOP/N) will be forced to a constant low, and the PLL will change its reference from the serial data stream to the reference clock. This input is to be driven by the external bandpass filter and peak detect circuit as shown in Figure 18.

This signal must be used to assure correct automatic reacquisition to serial data following an interruption and subsequent reconnection of the data path. This will assure that the PLL does not “wander” out of reacquisition range when no signal is applied.

When LOSIN is inactive, data on the SERDATIP/N pins will be processed normally.

Loss of Optical Signal [LOSOPT]—PECL. Active Low. This input has the same functionality as LOSIN, except that it is used in optical mode instead of electrical. It should be driven by the external optical receiver module to indicate a loss of received optical power.

Loss of Signal Reference [LOSREF]—Analog. Sets the comparator levels for LOSIN. (See Table 7.)

Loop Filter Capacitor [CAP1, CAP2]—The loop filter capacitor is connected to these pins. The capacitor value should be $0.1\mu\text{f} \pm 10\%$ tolerance, X7R dielectric, 50 volt rating is recommended.

Output Signals

Loss of Signal Out [LOSOUT]—TTL. Active Low. Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming datastream. LOSOUT is an asynchronous output. This output is deasserted when there is no incoming serial data input or when the received signal has dropped below the reference voltage set by LOSREF for more than 96 to 224 bit intervals. In this case the PLL locks to the reference clock.

Serial Data Out [SERDATOP/N]—Differential PECL. This signal is the NRZ data output. It can be either a delayed version of the NRZ data input (NRZ mode) or the decoded CMI data (CMI mode). SERDATOP/N is updated on the falling edge of SERCLKOP/N per Figure 13.

Serial Clock Out [SERCLKOP/N]—Differential PECL. This signal is phase-aligned with Serial Data Out (SERDATOP). (See Figure 13 and Table 3 for timing.)

Line Code Violation [LCV]—Single-ended PECL. Set high to indicate that the current bit contains a CMI line code violation in CMI mode. LCV is updated on the falling edge of SERCLKOP/N per Figure 13. In NRZ mode, this is a test output.

Buffer Output [BUFOUT]—Analog. Output of the equalizer network buffer circuit. This circuit provides a low impedance driver to the equalizer circuit. This pin should be connected as shown in Figure 18 to drive the equalizer network.

Reference Clock Out [REFCKOUT]—TTL. Single-ended TTL reference clock output (19.44 MHz).

OTHER OPERATING MODES

Diagnostic Loopback

When the chipset is used in an electrical interface, the serial data output (SERDATOP/N) of the transmitter can be connected the serial data input (SERDATIP/N) of the receiver to implement a loopback test for diagnostic purposes, as shown in Figure 15. In this mode, SERDATEN on the transmitter and EQUALSEL on the receiver are both held low. LOSOPT on the receiver is held high or not connected.

Test Mode

The Test Clock Enable (TSTCLKEN) inputs on both chips provide access to the PLL.

The PLL-generated clock source on both the S3015 and S3016 can be bypassed by setting TSTCLKEN high. In this mode, an externally generated clock source must be applied at the REFCLKIN input.

Clock Synthesis

In the Clock Synthesis mode, the S3015 synthesizes the E4 (139.264 MHz) clock from a 17.408 MHz crystal oscillator or the STS-3/STM-1 (155.52 MHz) clock from a 19.44 MHz crystal oscillator. In this mode, a crystal oscillator is connected to the TTL reference input and synthesized up to the output frequency.

The S3015 PLL complies with jitter generation for clock synthesis proposed for SONET/SDH equipment defined by the Bellcore TA-NWT-000253 standard, when used with a crystal reference source as defined in Table 4.

Figure 15. Diagnostic Loopback Interface

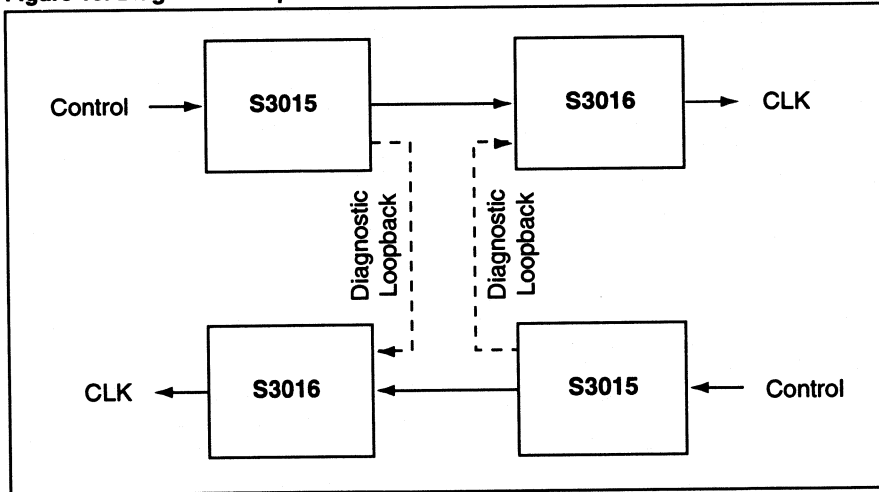
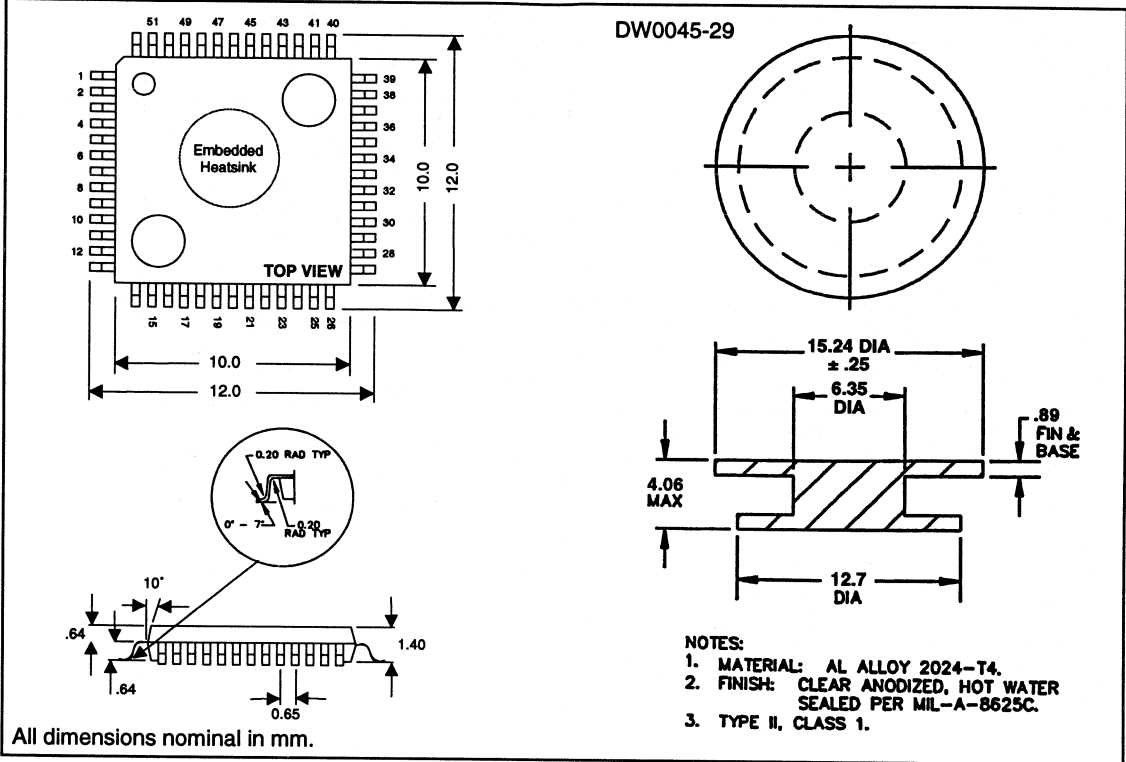


Figure 16. 52-Pin PQFP Package and Heatsink



S3015 Transmitter Pinouts

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	CAP1	14	TTLVCC	27	TTLGND	40	AVCC0
2	AVEE3	15	ECLVCC	28	ECLVCC	41	N.C.
3	AVCC3	16	N.C.	29	SERCLKOP	42	AVEE0
4	ECLVCC	17	N.C.	30	SERCLKON	43	AVEE2
5	SERDATEN	18	N.C.	31	ECLVCC	44	N.C.
6	SERDATON	19	AVCC4	32	ECLVEE	45	SERDATIP
7	SERDATOP	20	XFRMDRVA	33	CMISEL	46	SERDATIN
8	ECLVEE	21	XFRMDRVB	34	DLCV	47	N.C.
9	ECLVCC	22	AVEE4	35	TSTCLKEN	48	AVCC2
10	REFCKIN	23	XFRMEN	36	ECLVEE	49	N.C.
11	REFCKOUT	24	RST	37	ECLVCC	50	N.C.
12	ECLVCC	25	ECLVCC	38	AVCC1	51	N.C.
13	TTLGND	26	TTLVCC	39	AVEE1	52	CAP2

S3016 Receiver Pinouts

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	CAP1	14	TTLVCC	27	TTLGND	40	AVCC0
2	AVEE3	15	AVCC4	28	SERCLKOP	41	N.C.
3	AVCC3	16	ANDATIN	29	SERCLKON	42	AVEE0
4	LOSOPT	17	AVEE4	30	ECLVCC	43	AVEE2
5	LOSOUT	18	LOSIN	31	LCV	44	N.C.
6	SERDATOP	19	LOSREF	32	CMISEL	45	SERDATIP
7	SERDATON	20	BUFOUT	33	EQUALSEL	46	SERDATIN
8	ECLVEE	21	AVEE5	34	RST	47	N.C.
9	ECLVCC	22	BUFINA	35	TSTCLKEN	48	AVCC2
10	REFCKIN	23	BUFINB	36	ECLVEE	49	N.C.
11	REFCKOUT	24	AVCC5	37	ECLVCC	50	N.C.
12	ECLVCC	25	ECLVCC	38	AVCC1	51	N.C.
13	TTLGND	26	TTLVCC	39	AVEE1	52	CAP2

Power Supply Connections:

AVCC0, AVCC1, AVCC2, AVCC3, AVCC4	=	ANALOG +5V
AVEE0, AVEE1, AVEE2, AVEE3, AVEE4	=	ANALOG 0V
ECLVCC, TTLVCC	=	DIGITAL +5V
ECLVEE, TTLGND	=	DIGITAL 0V
N.C.	=	NOT CONNECTED

Table 3. S3015/S3016 Clock Recovery Mode Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	Given REFCKIN = VCO + 32
OC-3/STS-3 Lock Range		+8, -12		%	With respect to fixed reference frequency
Acquisition Lock Time ¹			64	μsec	With device already powered up and valid REFCLK
Reference Clock Input Duty Cycle	30		70	% of UI	
Reference Clock Rise & Fall Times			5.0	ns	10% to 90% of amplitude
PECL Output Rise & Fall Times			850	ps	10% to 90%, 50Ω load, 5 pf cap
Reference Clock Frequency Tolerance	-100		100	ppm	
^{IP} _{SER} SERCLKOP Falling to SERDATO Valid Prop Delay	100		500	ps	See Figure 13

1. Specification based on design values. Not tested.

Table 4. S3015 Clock Synthesis Mode Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
PECL Data Output Jitter (S3015 SERDATOP/N) OC-3/STS-3 E4-STS-3 CMI			64 32	ps (rms)	In CSU mode, given <ul style="list-style-type: none"> • 56 ps rms jitter on REFCKIN in 12KHz to 1 MHz band • 28 ps rms jitter on REFCKIN in 12KHz to 1 MHz band
Reference Clock Frequency Tolerance Clock Synthesis	-20		+20	ppm	Required to meet SONET output jitter generation specification

Table 5. Electrical Characteristics for Transformer Driver

(V_{cc} = +5V, T_A = +25°C, input AC coupled unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Condition
Operating Frequency		155		MHz	270 Ω 3pF load
Trise Tfall		1.0 1.0	1.7 1.7	ns ns	270 Ω 3pF load
Duty Cycle	45	50	55	%	270 Ω 3pF load
Vp-p	1.8	2.1	2.4	V	270 Ω 3pF load
DC midpoint		V _{cc} -2.0		V	270 Ω 3pF load
Overshoot		50	100	mV	270 Ω 3pF load
VSWR (1)		1.3:1	1.5:1		75 Ω A.C. Coupled Termination

1. Up to 250 MHz

Table 6. Electrical Characteristics for ANDATIN Input

($V_{CC} = +5V$, $T_A = +25^\circ C$, input AC coupled unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak to Peak Input Voltage Range	V_{Iptp}				1.3	V
Common-Mode Rejection Ratio	CMRR ⁽¹⁾		40			dB
Power-Supply Rejection Ratio	PSRR ⁽¹⁾		40			dB
Input Resistance	R_{IN}		5.5	8	10.4	K Ω
Input Capacitance	C_{IN}		1.5	2	3	pF
Input Sensitivity	S_{IN}	$T_A = \text{MIN to MAX}$	90			mV
Toggle Rate	F	$T_A = \text{MIN to MAX}$ 40mV Overdrive	600			MHz
Toggle Rate	F	$T_A = \text{MIN to MAX}$ 20mV Overdrive	200			MHz
DC offset at input ⁽²⁾				$V_{CC} - 1V$		V

1. Up to 300 KHz
2. Signal is undefined if left floating

Table 7. Electrical Characteristics for LOSIN Input

($V_{CC} = +5V$, $T_A = +25^\circ C$, input AC coupled unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak to Peak Input Voltage Range	V_{Iptp}				1.1	V
Common-Mode Rejection Ratio	CMRR ⁽¹⁾		40			dB
Power-Supply Rejection Ratio	PSRR ⁽¹⁾			35		dB
Input Resistance	R_{IN}		6000	8000		Ω
Input Capacitance	C_{IN}		1.5	2.0	3.0	pF
Signal Level for LOS detected		$T_A = \text{MIN to MAX}$	LOS-REF/22	LOS-REF/20	LOS-REF/18	V/V
Signal Level for LOS cleared		$T_A = \text{MIN to MAX}$	LOS-REF/11	LOS-REF/10	LOS-REF/9	V/V
Hysteresis between "trans. cond." and "no trans. cond." ⁽²⁾			4	6		dB
Offset of comparators					4.5	mV
Offset between comparators					6	mV
LOSREF input resistance			6000	9000		Ω

1. Up to 300 KHz
2. LOSREF >0.5 volts

Below are typical operating conditions:

Voltage Applied at LOSREF	Compare Voltage #1	Compare Voltage #2	Hysteresis
1.4 Volts	140 mV \pm 0.6dB	70 mV \pm 1dB	6dB +1.6 -1.4dB
0.7 Volts	70 mV \pm 1dB	35 mV \pm 1.6dB	6dB +2.7 -2.0dB
0.3 Volts	30 mV \pm 1.6dB	15 mV \pm 3.5dB	6dB +6.0 -3.7dB

Table 8. Electrical Characteristics for BUFIN, BUFOUT

At $V_{CC} = +5VDC$, $R_{LOAD} = 75\Omega$ a.c. coupled and $T_A = 25^\circ C$ unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS (BUFOUT) Voltage Output			± 0.6	± 0.8		V
Output Resistance			1	3	8	Ω
TRANSFER CHARACTERISTICS Gain (BUFIN to BUFOUT) ⁽¹⁾			.85	.93	1	V/V
INPUT CHARACTERISTICS Impedance (BUFIN) ⁽¹⁾			8 4	12 3	16 1.5	K Ω pF
Bandwidth	BW	Input = 0.2V p-p Input = 0.6V p-p Input = 1.2V p-p	800 700 500	900 800 600		MHz MHz MHz
Gain Flatness		Input = 0.2V p-p to 500 MHz Input = 0.6V p-p to 400 MHz Input = 1.2V p-p to 300 MHz		0.5 0.5 0.5	1.0 1.0 1.0	dB dB dB
Group Delay		From 10 MHz to 500 MHz Input = 0.3V p-p Input = 0.6V p-p Input = 1.2V p-p		400 400 400	500 500 500	ps ps ps
Group Delay Variation		From 10 MHz to 500 MHz Input = 0.3V p-p Input = 0.6V p-p Input = 1.2V p-p		200 200 200	300 300 300	ps ps ps
VSWR ⁽²⁾	VSWR	With 75 ohm AC coupled termination		1.3:1	1.5:1	
Harmonic Distortion ⁽²⁾	HD	Input = 0.3V p-p Input = 0.6V p-p Input = 1.2V p-p	35 30 25	40 35 30		dBc
DC Input Bias		Input externally AC coupled		$V_{CC} - 0.85$		V
DC Output Bias		Output externally AC coupled		$V_{CC} - 2.5$		V

1. Up to 300 KHz

2. Up to 250 MHz

Thermal Management

Device	Power	Θ_{ja} Still Air w/DW0045-29	Max Still Air ¹ w/DW0045-29
S3015/S3016	1.25W	37.5°C/W	85°C

1. Max ambient temperature permitted in still air to maintain $T_j < 130^\circ C$.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	TYP	MAX	UNIT
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Respect to GND	-0.5		+7.0	V
Voltage on Any TTL Input Pin	-0.5		+5.5	V
Voltage on Any PECL Input Pin	VCC-3		VCC	V
TTL Output Sink Current			20	mA
TTL Output Source Current			10	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage		500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Ambient Temperature under Bias	-40		85	°C
Junction Temperature under Bias	-10		+125	°C
Voltage on VCC with Respect to GND	4.75	5.0	5.25	V
Voltage on Any TTL Input Pin	0		VCC	V
Voltage on Any PECL Input Pin	VCC-2		VCC	V
S3015 ICC		141	240	mA
S3016 ICC		180	240	mA

TTL INPUT/OUTPUT DC CHARACTERISTICS
 $(T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, V_{CC} = 5\text{ V} \pm 5\%)$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}^1	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}^1	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
I_{IL}	Input LOW Current	-400.0			μA	$V_{CC} = \text{MAX}, V_{IN} = 0.5\text{V}$
I_{IH}	Input HIGH Current			50.0	μA	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$
I_I	Input HIGH current at Max. VCC			1.0	mA	$V_{CC} = \text{MAX}, V_{IN} = 5.5\text{V}$
I_{OS}	Output Short Circuit Current	-100.0		-25.0	mA	$V_{CC} = \text{MAX}, V_{OUT} = 0.5\text{V}$
V_{IK}	Input Clamp Diode Voltage	-1.2			Volts	$V_{CC} = \text{MIN}, I_{IN} = -18\text{ ma}$
V_{OL}	Output LOW Voltage			0.5	Volts	$V_{CC} = \text{MIN}, I_{OL} = 8\text{ ma}$
V_{OH}	Output HIGH Voltage	2.7			Volts	$V_{CC} = \text{MIN}, I_{OH} = -1\text{ ma}$

1. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

PECL INPUT/OUTPUT DC CHARACTERISTICS^{1,2}
 $(T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, V_{CC} = 5\text{ V} \pm 5\%)$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}	Input LOW Voltage	$V_{CC} - 2.000$		$V_{CC} - 1.441$	Volts	Guaranteed Input LOW Voltage for single-ended inputs
V_{IH}	Input HIGH Voltage	$V_{CC} - 1.225$		$V_{CC} - 0.570$	Volts	Guaranteed Input HIGH Voltage for single-ended inputs
V_{iL}	Input LOW Voltage	$V_{CC} - 2.000$		$V_{CC} - 0.700$	Volts	Guaranteed Input LOW Voltage for differential inputs
V_{iH}	Input HIGH Voltage	$V_{CC} - 1.750$		$V_{CC} - 0.450$	Volts	Guaranteed Input HIGH Voltage for differential inputs
V_{ID}	Input Diff. Voltage	0.250	0.500	1.400	Volts	Differential Input Voltage
I_{IH}	Input High Current	-0.500		20.000	μA	$V_{ID} = 500\text{mV}$
I_{iL}	Input Low Current	-0.500		20.000	μA	$V_{ID} = 500\text{mV}$
V_{OL}	Output LOW Voltage	$V_{CC} - 2.000$		$V_{CC} - 1.500$	Volts	50 ohm termination to $V_{CC} - 2\text{V}$
V_{OH}	Output HIGH Voltage	$V_{CC} - 1.110$		$V_{CC} - 0.670$	Volts	50 ohm termination to $V_{CC} - 2\text{V}$
V_{OD}	Output Diff. Voltage	0.390		1.330	Volts	Differential Output Voltage

- These conditions will be met with no airflow.
- When not used, tie the positive differential PECL pin to V_{CC} and the negative differential ECL pin to ground via a 3.9K resistor.

Figure 17. Differential ECL Input and Output Applications

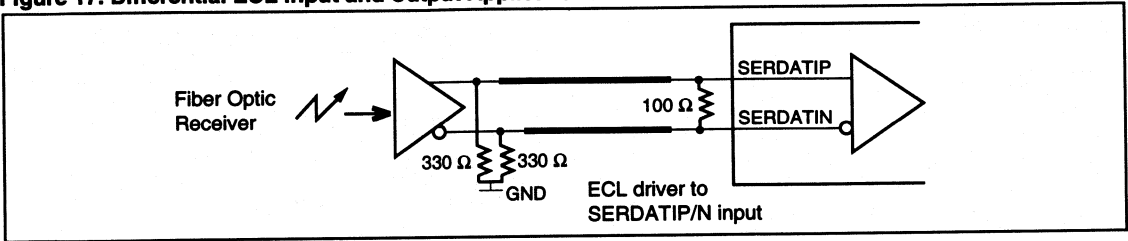


Figure 18. S3016 Transformer Input Application

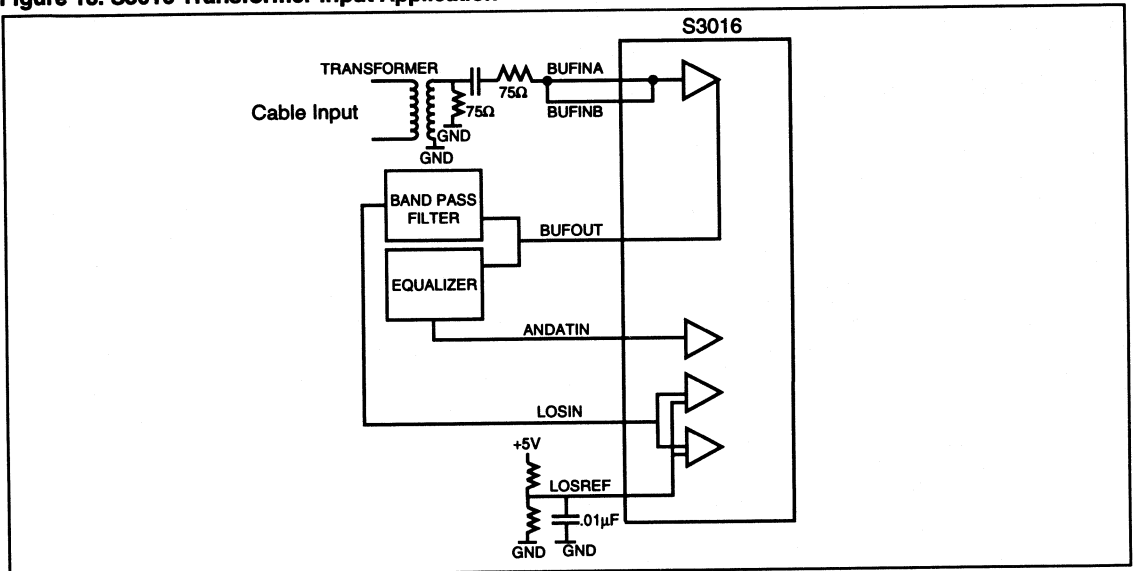


Figure 19. S3015 Differential ECL Output Application

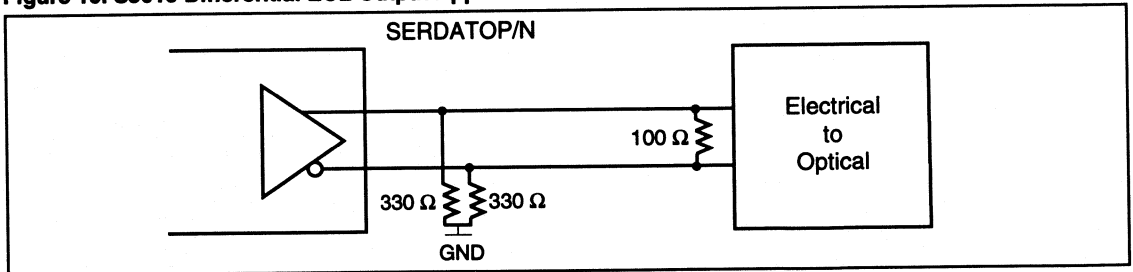


Figure 20. S3015 Transformer Output Application

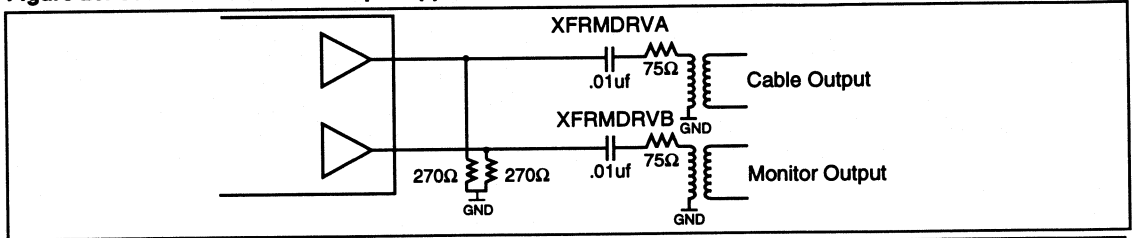


Figure 21. OC3 Application

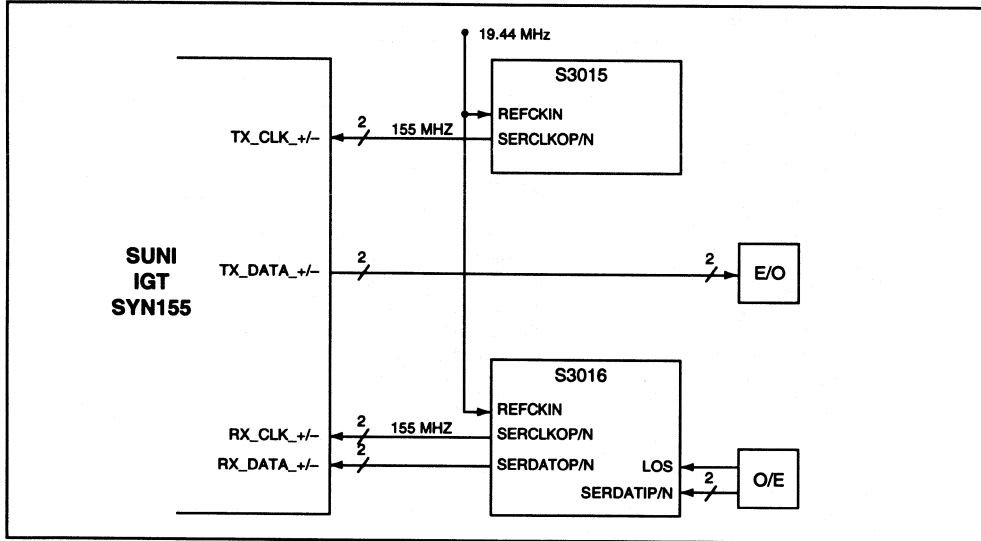
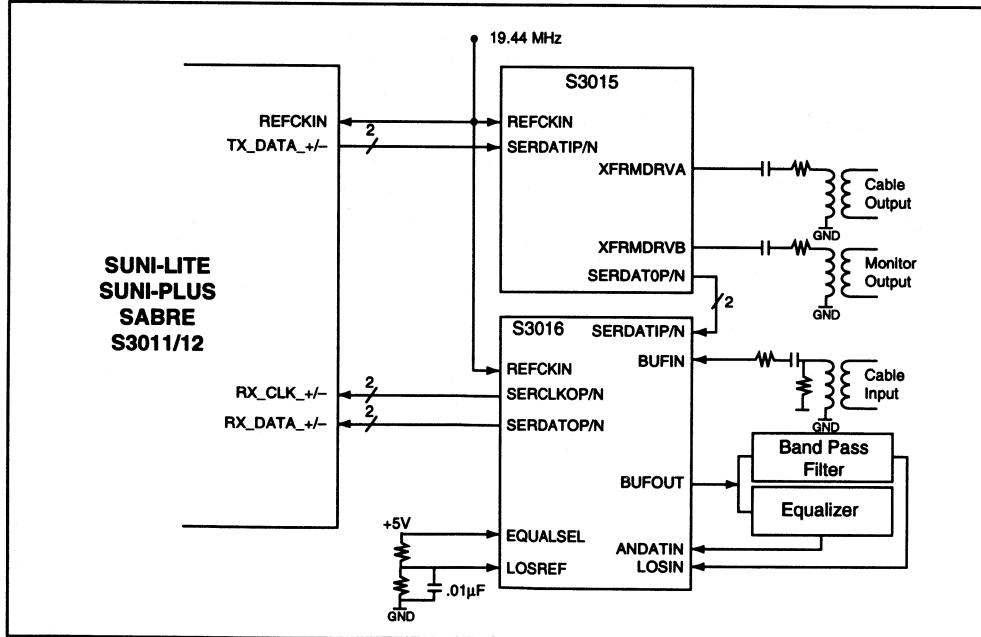


Figure 22. STM-1 CMI, E4 Application



7

Table 9. Suggested Interface Devices

Processor Interface		
PMC PM5345	SUNI	Saturn User Network Interface
PMC PM5346	SUNI-Lite	Saturn User Network Interface
PMC PM5347	SUNI-Plus	Saturn User Network Interface
IGT WAC-013-A		SONET LAN ATM Processor
TRANSWITCH SYN155		155 Mbit/s Synchronizer
TI SABRE TDC 1500		155 Mbit/s Processor
AMCC S3011/12		SONET/SDH/ATM OC3 Transmitter & Receiver
Electrical Interface		
Mini-Circuits	MCL TXI-R5	Wideband RF Transformer (Surface Mount)
Mini-Circuits	MCL TO-75	Wideband RF Transformer (Through-Hole)
Optical Interface		
HP HFBR-520x	155 Mbit/s	Fiber Optic Transceiver
CTS ODL-1408X	155 Mbit/s	Fiber Optic Transceiver
Sumitomo SDM4123-XC	155 Mbit/s	Fiber Optic Transceiver
AMP 269039-1	155 Mbit/s	Fiber Optic Transceiver

Ordering Information

GRADE	TRANSMITTER	
S – Industrial/ commercial	3015	A – 52 PQFP TEP w/DW0045-29 heatsink unattached

GRADE	RECEIVER	
S – Industrial/ commercial	3016	A – 52 PQFP TEP w/DW0045-29 heatsink unattached

X **XXXX** **X**
 Grade Part number Package

EVALUATION MANUAL

The S6006 Evaluation Manual describes two evaluation boards that allow demonstration of AMCC's S3015/S3016 E4/STM-1/OC-3 SONET/SDH/ATM interface circuits. This document provides information on board contents and layout. It should be used in conjunction with the S3015/S3016 data sheet, which contains full technical details on chip operation.

Figure 1 depicts a block diagram of circuit functionality. Power is supplied to the boards from external raw supplies connected through the on-board power connections. Connectors allow easy access to all of the interface signals on the S3015/S3016 chips. All required external circuitry, including transformers and passive components, are provided on the boards. For additional detail on the interface circuitry or for applications examples, contact AMCC for the S3015/S3016 "Systems Interface Application Note".

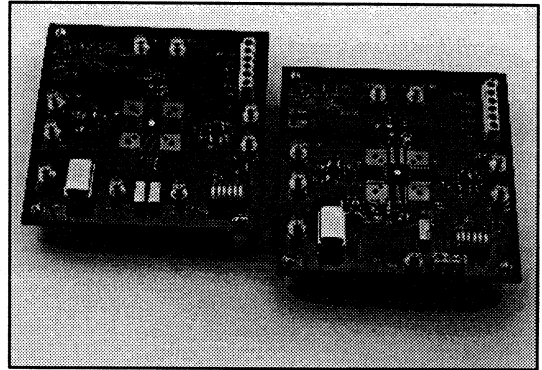
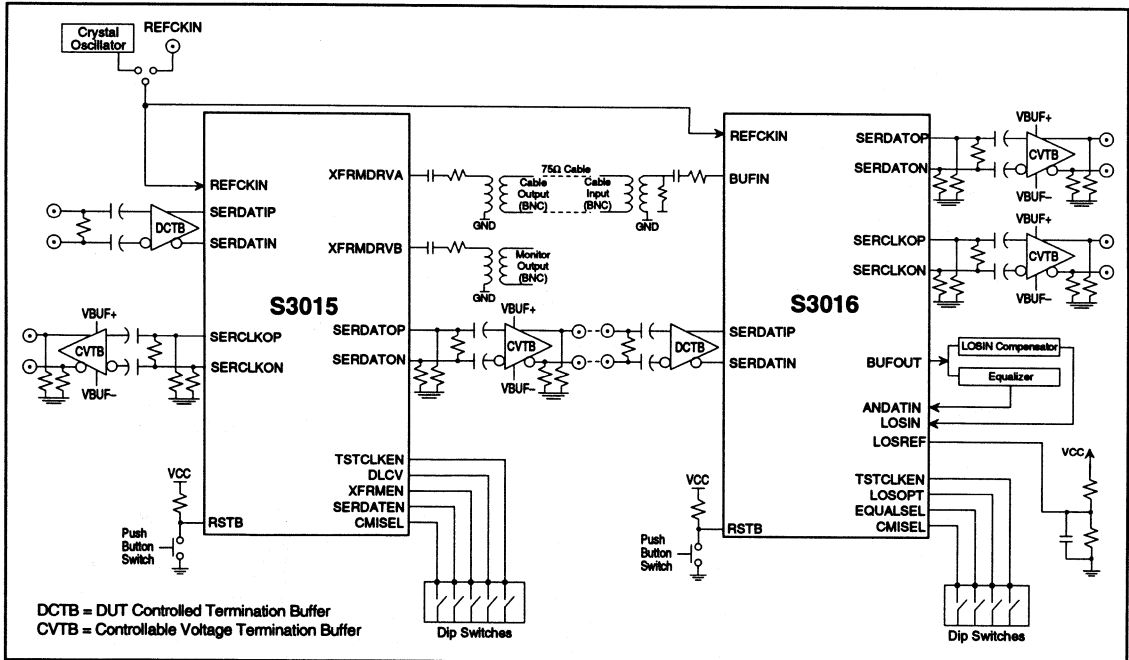


Figure 1. Functional Block Diagram



ELECTRICAL CONNECTIONS

Separate boards are provided for the S3015 and the S3016 chips. Layouts for both boards are depicted in Figures 2 and 3, showing the location of connectors and components. The various connections are described in the following sections.

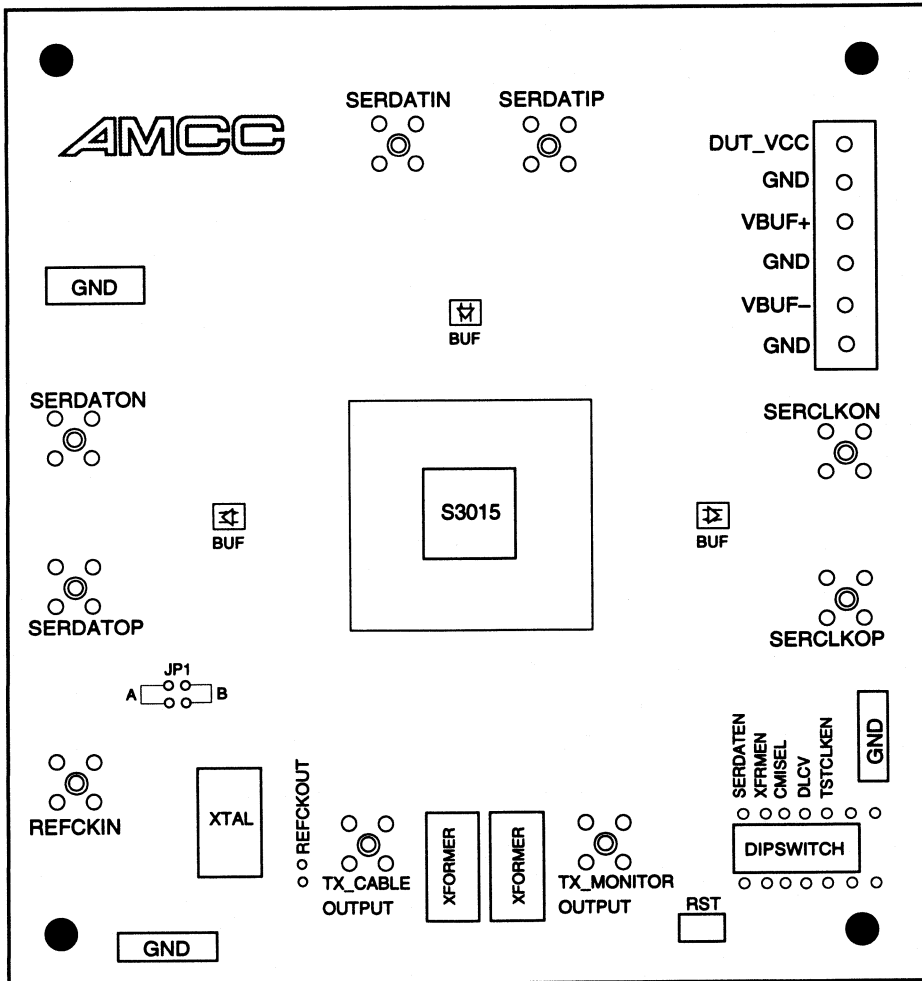
Power Connections

Connections are provided on the board for ground and VCC. Refer to Table 1 for recommended operating conditions.

Table 1. Power Connection Recommended Operating Conditions

Power Supply	Nominal Input Voltage
VCC	5 V
Ground	0 V

Figure 2. S3015 Board Layout



Cable Connections - Transmitter

Two BNC connectors allow connection to the following two output signals. (See Figure 2 for locations.)

TX_OUT. Transformer Output. Drives the G.703 specified 75-ohm cable. The G.703 output mask can be measured at this point.

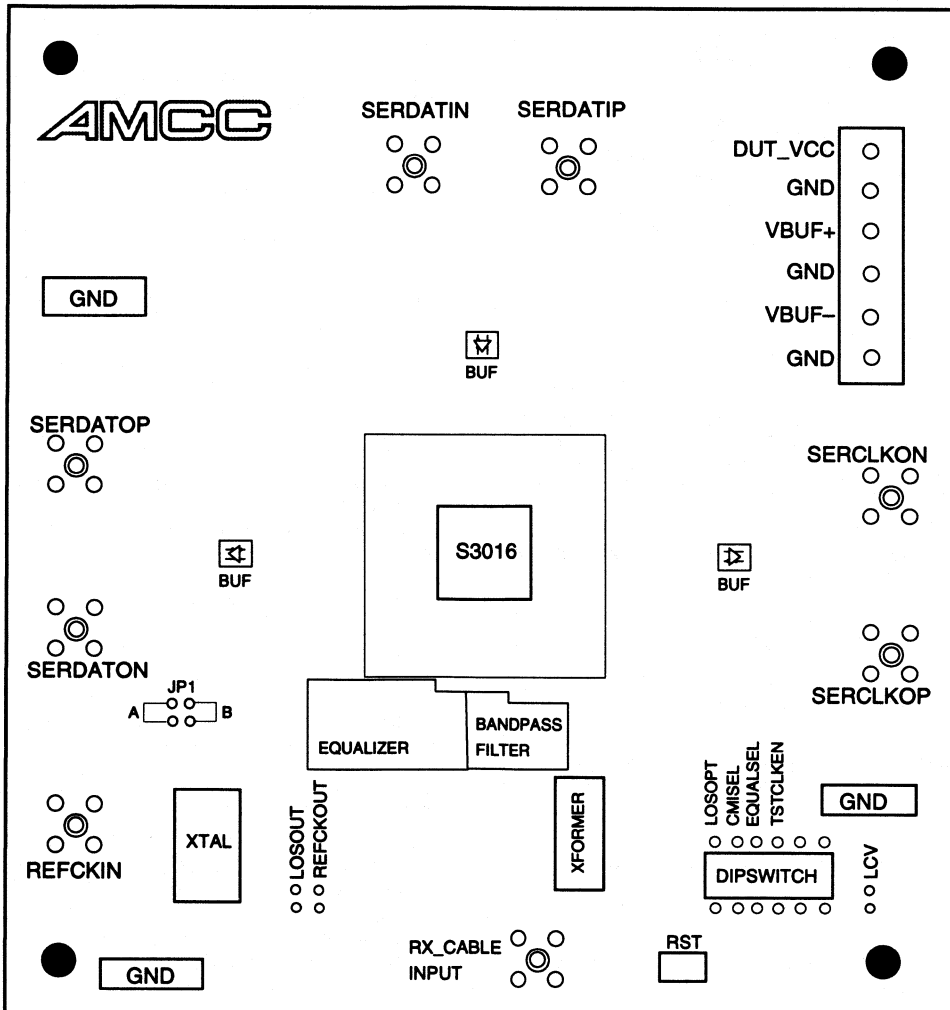
MON_OUT. Transformer Output. Drives the monitor point as specified in G.703. This output is identical to the TX_OUT signal.

Cable Connections - Receiver

A BNC connector allows connection to the following input signal. (See Figure 3 for location.)

RX_IN. Transformer Input. Receives the G.703 compliant signal. The G.703 input waveforms and loss-of-signal detection levels are specified at this connector.

Figure 3. S3016 Board Layout



Overhead Processor Connections - Transmitter

RESET. TTL Input. Initializes the S3015 to a known logic state.

SERDATIP/N. Differential AC-coupled PECL. SMA connector that drives the serial data inputs to the CMI encoder circuit. This input should be supplied with NRZ data at the appropriate data rate. (See Table 2.)

REFCKIN. TTL input. SMA connector that must be supplied with the correct reference clock frequency. (See Table 2.) Used by the S3015 to synthesize the serial clock.

SERDATOP/N. Differential PECL. This output is the delayed version of the incoming data stream updated on the falling edge of SERCLKOP/N.

SERCLKOP/N. Differential PECL. This output is phase-aligned with SERDATOP/N.

Table 2. Operating Frequencies

MODE	REF CLK FREQ (REFCKIN/P) MHz	SERIAL DATA RATE (SERDATIP/N, TX_OUT) Mbits/s
STS-3 CMI	19.44	155.52
E4 CMI	17.408	139.264

DIP Switch - Transmitter

An onboard DIP switch provides additional control capability on the transmitter board. The following five signals are controlled by means of the DIP switch:

SERDATEN. TTL input. Enables the loopback path from the S3015 to the S3016. The data from the SERDATIP/N inputs will be CMI-encoded and sent to the S3016, where it will be decoded and output on the SERDATOP/N pins.

XFRMEN. TTL input. Enables the transformer outputs TX_OUT and MON_OUT.

CMISEL. TTL input. Selects CMI or NRZ. Logic High selects CMI mode, and Logic Low selects NRZ mode.

DLCV. Singled-ended PECL input. Only active in CMI mode. Set High to force a CMI line code violation.

TSTCLKEN. TTL input. Enables the reference clock to be used instead of the VCO for testing, allowing a means of testing chip functions without the use of the PLL.

Overhead Processor Connections - Receiver

RESET. TTL Input. Initializes the S3016 to a known logic state.

SERDATIP/N. Differential PECL. Clock is recovered from transitions on these inputs.

REFCKIN. TTL input. SMA connector that must be supplied with the correct reference clock frequency. (See Table 2.) Used by the S3016 to initialize the receive clock recovery PLL. The reference clock must be present during reset to guarantee initialization of the PLL circuits.

SERDATOP/N. Differential AC-coupled PECL output. SMA connector that drives the decoded CMI data to the overhead processor.

SERCLKOP/N. Differential PECL. This output is phase-aligned with SERDATOP/N.

LOSOUT. TTL output. When High, this signal indicates that the clock recovery PLL is detecting valid data at the serial data inputs and is attempting to lock to it. When Low, the clock recovery PLL is locked to REFCKIN.

REFCKOUT. TTL input. Clock output that is at the same frequency as the REFCKIN input.

DIP Switch - Receiver

An onboard DIP switch provides additional control capability on the receiver board. The following four signals are controlled by means of the DIP switch:

LOSOPT. PECL. Active Low. This input is driven by the external optical receiver module to indicate a loss of received optical power.

CMISEL. TTL input. A Logic High selects CMI mode; a Logic Low selects NRZ.

EQUALSEL. TTL input. A Logic High selects ANDATIN. A Logic Low selects SERDATIP/N.

TSTCLKEN. TTL. Active High. Enables the reference clock to be used in place of the VCO for testing. Allows a way to test the chip without the use of the PLL.

CRYSTAL REFERENCE

A 19.44 MHz or a 17.408 MHz differential ECL crystal oscillator can be used for the reference clock. One 19.44 MHz crystal is provided on each board. If a 17.408 MHz reference frequency is needed, AMCC can recommend crystal vendors.

JUMPER CONFIGURATION

The jumpers labeled JP1 on both boards allow the user to control whether an onboard crystal reference or external clock reference is used (see Crystal Reference above). Jumper A is installed when an external reference is used, and Jumper B is installed when the onboard crystal reference is used.

FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLL for clock generation and clock recovery
- Supports 622.08 Mbit/s (OC-12/STM-4)
- Reference frequency of 77.76 MHz
- Interface to both PECL and TTL logic
- 8-bit TTL datapath
- Compact 52 PQFP TEP package
- Diagnostic loopback mode
- Lock detect
- Low jitter PECL interface
- < 2.0 Watt per set typically

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add drop multiplexors
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

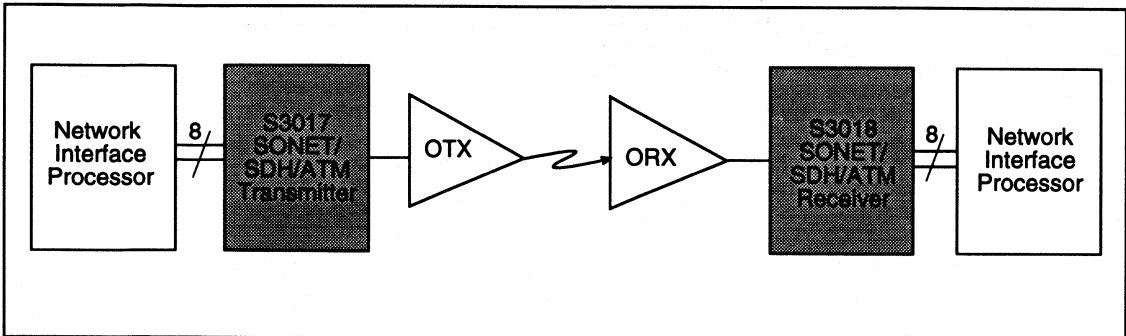
GENERAL DESCRIPTION

The S3017/S3018 SONET/SDH/ATM transmitter and receiver chips are fully integrated serialization/deserialization SONET OC-12 (622.08 Mbit/s) interface devices. With architecture developed by PMC-Sierra, Inc., the chipset performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The devices are suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3017 transmitter chip allowing the use of a slower external transmit clock reference. Clock recovery is performed on the S3018 receiver chip by synchronizing its on-chip VCO directly to the incoming data stream. The S3018 also performs SONET/SDH frame detection. The chipset can be used with a 19.44 or 77.76 MHz reference clock, in support of existing system clocking schemes.

The low jitter PECL interface guarantees compliance with the bit-error rate requirements of the Bellcore, ANSI, and ITU-T standards. The S3017 and S3018 are packaged in a compact 52 PQFP, offering designers a small package outline.

Figure 1. Link Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

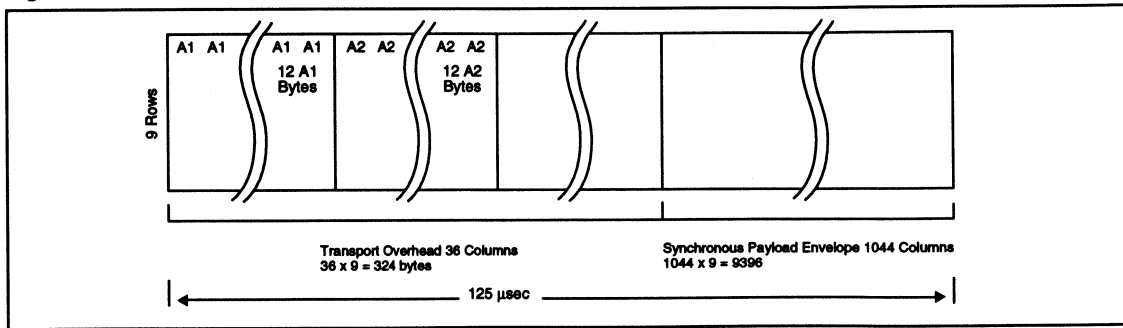
- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3017/S3018 chipset supports OC-12 rates (622.08 Mbit/s).

Figure 3. STS-12/OC-12 Frame Format



Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-12 consists of 36 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 36 overhead and 1044 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the ANSI SONET standard document.

Figure 2. SONET Structure

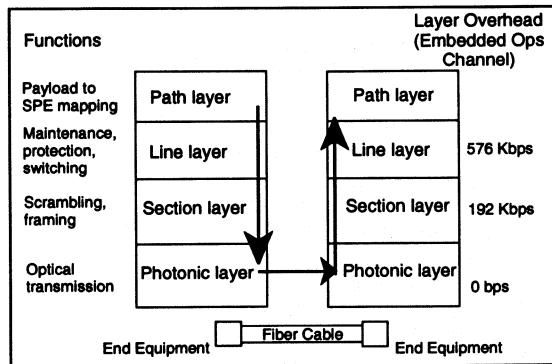


Table 1. SONET Signal Hierarchy

Elec.	ITU-T	Optical	Data Rate (Mbit/s)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24		OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

S3017/S3018 OVERVIEW

The S3017 transmitter and S3018 receiver implement SONET/SDH serialization/deserialization, transmission, and frame detection/recovery functions. The block diagrams in Figures 4 and 5 show basic operation of both chips. These chips can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface (S3017) and the serial receive interface (S3018). The chipset handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation and recovery, and system timing. The system timing circuitry consists of management of the datastream, framing, and clock distribution throughout the front end.

Operation of the S3017/S3018 chips is straightforward. The sequence of operations is as follows:

Transmitter

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver

1. Clock and data recovery from serial input
2. Frame detection
3. Serial-to-parallel conversion
4. 8-bit parallel output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 9 through 14.

A lock detect feature is provided on the S3018, which indicates that the PLL is locked (synchronized) to the data stream, and facilitates continuous down-stream clocking in the absence of data.

Suggested Interface Devices

PMC PM5312	STTX	SONET/SDH Transport Term. Transceiver
PMC PM5355	SUNI-622	Satum User Network Interface
AT&T ASTROTEC 1227/1230	650 Mbit/s	Fiber Optic Transmitter
Mitsubishi MF-622DF-T12-XXX	622 Mbit/s	Fiber Optic Transmitter
Sumitomo ES-9304-TD	622 Mbit/s	Fiber Optic Transmitter
AT&T ASTROTEC 1310	650 Mbit/s	Fiber Optic Receiver
Mitsubishi MF-622DS-R1X-XXX	622 Mbit/s	Fiber Optic Receiver
Sumitomo ES-9216-RD	622 Mbit/s	Fiber Optic Receiver
Finisar	1000 Mbit/s	Fiber Optic Transceiver

Figure 4. S3017 Transmitter

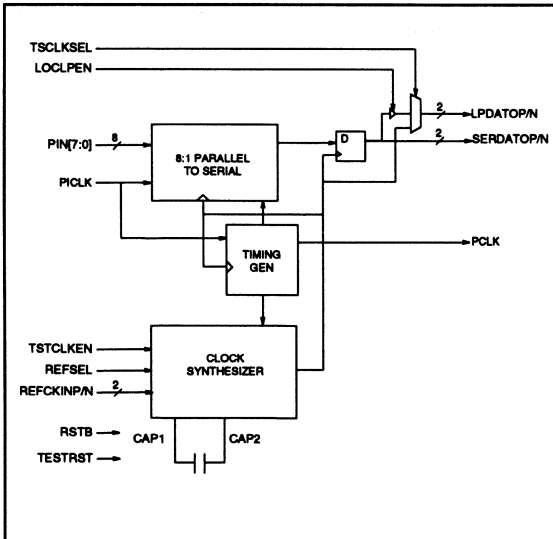
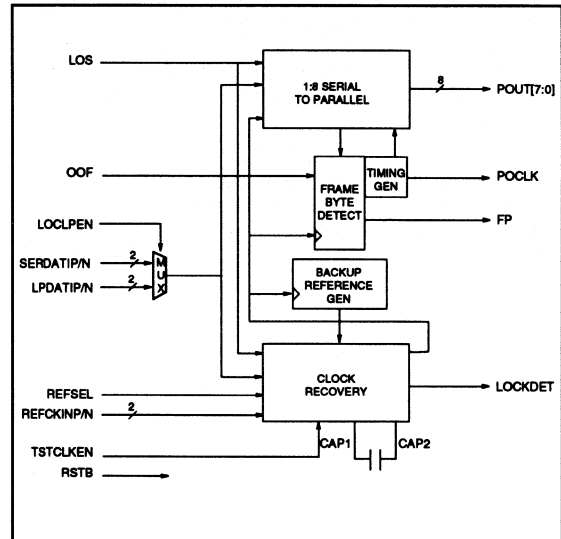


Figure 5. S3018 Receiver



S3017 TRANSMITTER ARCHITECTURE/FUNCTIONAL DESIGN

The S3017 transmitter chip performs the serializing stage in the processing of a transmit SONET STS-12 bit serial data stream. It converts the byte serial 77.76 Mbyte/sec data stream to bit serial format at 622.08 Mbit/sec.

A high-frequency bit clock can be generated from a 77.76 MHz frequency reference by using an integral frequency synthesizer consisting of a phase-locked loop circuit with a divider in the loop.

Diagnostic loopback is provided (transmitter to receiver) when used with the compatible S3018. (See Other Operating Modes.)

Clock Synthesizer

The Clock Synthesizer, shown in the block diagram in Figure 4, is a monolithic PLL that generates the serial output clock phase synchronized with the input reference clock (REFCKINP/N).

The REFCKINP/N input must be generated from a differential PECL crystal oscillator which has a frequency accuracy of better than 20 ppm in order for the TSCLK frequency to have the same accuracy required for operation in a SONET system. Lower accuracy crystal oscillators may be used in applications less demanding than SONET/SDH.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCKINP/N input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

Timing Generator

The Timing Generation function, seen in Figure 4, provides a byte rate version of the transmit serial clock. This circuitry also provides an internally generated load signal, which transfers the PIN[7:0] data from the parallel input register to the serial shift register.

The PCLK output is a byte rate version of transmit serial clock at 77.76 MHz. PCLK is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3017 device.

Parallel-to-Serial Converter

The Parallel-to-Serial converter shown in Figure 4 is comprised of two byte-wide registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PCLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

The load signal, which latches the data from the parallel to the serial shift register, has a fixed relationship to PCLK. If PCLK is tied to PCLK, the PIN[7:0] data latched into the parallel register will meet the timing specifications with respect to the load signal. If PCLK is not tied to PCLK, the delay must meet the timing requirements shown in Figure 9, and PCLK must be frequency locked to the reference clock input.

TRANSMITTER PIN DESCRIPTIONS

Input Signals

Parallel Data Input [PIN]<7:0>. TTL. A 77.76 Mbyte/sec word, aligned to the PICKL parallel input clock. PIN<7> is the most significant bit (corresponding to the first bit transmitted). PIN<0> is the least significant bit (corresponding to the last bit transmitted). PIN<7:0> is sampled on the rising edge of PICKL.

Parallel Input Clock [PICKL]. TTL. A 77.76 MHz nominally 50% duty cycle input clock, to which PIN<7:0> is aligned. PICKL is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PICKL samples PIN<7:0>.

Test Clock Enable [TSTCLKEN]. TTL. Active High. Enables the reference clock to be used in place of the VCO for testing. Allows a means of testing the functions of the chip without the use of the PLL. Set low for normal operation.

Reference Clock [REFCKINP/N]. Differential PECL. Input used as the reference for the internal bit clock frequency synthesizer.

Local Loopback Enable [LOCLPEN]. TTL. Enables the LPDATO output when low and TSCLKSEL is low. When LOCLPEN is high, the LPDATO output is held in the inactive state to prevent interference between the transmit and receive devices.

Master Reset [RSTB]. TTL. Reset input for the device, active low. During reset, PCLK does not toggle.

Transmit Clock Select [TSCLKSEL]. TTL. Active high input which when enabled directs the transmit serial clock through the LPDATOP/N output.

Test Reset [TESTRST]. TTL. Used to reset portions of the clock recovery PLL during production testing. Held low for normal operation.

Reference Select [REFSEL]. TTL. Used to select the reference clock frequency. Set low to select 77.76 MHz. Set high to select 19.44 MHz for applications less demanding than SONET/SDH.

Loop Filter Capacitor [CAP1, CAP2]. The loop filter capacitor is connected to these pins. The capacitor value should be $0.01\mu\text{f} \pm 10\%$ tolerance, X7R dielectric. 50 volt is recommended (16 volt is acceptable).

Output Signals

Serial Data Out [SERDATOP/N]. High-speed, source-terminated differential PECL. Serial data stream signals, normally connected to an optical transmitter module.

Loopback Data [LPDATOP/N]. Differential PECL. Serial data stream signals, normally connected to a companion S3018 device for diagnostic loopback purposes. They are held inactive when LOCLPEN is high and TSCLKSEL is low. The serial data stream is output when LOCLPEN is low and TSCLKSEL is low. When enabled by the TSCLKSEL input the transmit serial clock will be output through this pin. The transmit serial clock is a buffered version of the internal frequency synthesizer clock, which is phase-aligned with the SERDATO output signal. The SERDATO is updated on the falling edge of the transmit serial clock.

Parallel Clock [PCLK]. TTL. A reference clock generated by dividing the internal bit clock by eight. It is normally used to coordinate byte-wide transfers between upstream logic and the S3017 device.

S3018 RECEIVER ARCHITECTURAL/FUNCTIONAL DESIGN

The S3018 receiver chip provides the first stage of digital processing of a receive SONET STS-12 bit-serial stream. It converts the bit-serial 622.08 Mbit/sec data stream into a 77.76 Mbyte/sec byte-serial data format.

Clock recovery is performed on the incoming scrambled NRZ data stream. A 77.76 MHz reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference to the nominal bit rate.

A loopback mode is provided for diagnostic loopback (transmitter to receiver), when used with the compatible S3017 device.

Clock Recovery

The Clock Recovery PLL, as shown in the block diagram in Figure 5, generates a clock that is at the same frequency as the incoming data bit rate at the SERDATI or LPDATI inputs. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock. Frequency stability without incoming data is guaranteed by an alternate reference input (REFCKIN) that the PLL locks onto when data is lost.

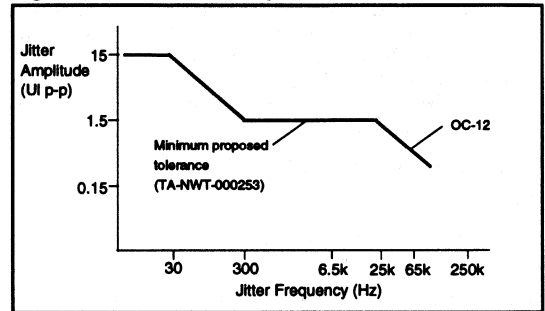
The clock recovery circuit monitors the incoming data stream for loss of signal. If the incoming data stream has had no transitions for between 96 and 224 bit times (depending upon the state of an internal counter at the time of last transition), loss of signal is declared and the PLL will switch from locking onto the incoming data to locking onto the reference clock. Alternatively, the loss-of-signal (LOS) input can be used to force a loss-of-signal condition. When set high, LOS squelches the incoming data stream, and thus causes the PLL to switch its source of reference within 128 bit times. Loss-of-signal condition is removed when LOS is low, and good data, with acceptable pulse density and run length, returns on the incoming data stream.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields a typical capture time of 16 μ s for random incoming NRZ data. A

single external clean-up capacitor is utilized as part of the loop filter.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which meets, with ample margin, the minimum tolerance proposed for SONET equipment by the Bellcore TA-NWT-000253 standard, shown in Figure 6.

Figure 6. Clock Recovery Jitter Tolerance



Backup Reference Generator

The Backup Reference Generator seen in Figure 5 provides backup reference clock signals to the clock recovery block when the clock recovery block detects a loss of signal condition. It contains a counter that divides the clock output from the clock recovery block down to the same frequency as the reference clock REFCKINP/N.

Frame and Byte Boundary Detection

The Frame and Byte Boundary Detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. Framing pattern detection is enabled and disabled by the out-of-frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration that OOF is set high. It is disabled when a framing pattern is detected and OOF is no longer set high. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (SERDATI or LPDATI). The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). The frame boundary is reported on the frame pulse (FP) output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an STS-12 stream will generate the 48-bit framing pattern is extremely small. It is highly improbable that a mimic pattern would occur within one frame of data. Therefore, the time to match the first frame pattern and to verify it with down-stream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 μ s, even for extremely high bit error rates.

Once down-stream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input can be set low to disable the frame search process from trying to synchronize to a mimic frame pattern.

Serial to Parallel Converter

The Serial to Parallel Converter consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the clock recovery block. The second is an 8-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the Serial to Parallel converter can vary from 1.5 to 2.5 byte periods (12 to 20 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries, with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial to parallel converter is that POCLK is neither truncated nor extended during reframe sequences.

S3018 RECEIVER PIN DESCRIPTIONS

Input Signals

Receive Serial Data [SERDATIP/N]. Differential PECL. Serial data stream signals normally connected to an optical receiver module. A clock is recovered from transitions on the SERDATI inputs.

Diagnostic Loopback Data [LPDATIP/N]. Differential PECL. Serial data stream signal, normally connected to a companion S3017 device for diagnostic loopback purposes. Clock is recovered from transitions on the LPDATI inputs while in diagnostic loopback.

Local Loopback Enable [LOCLPEN]. TTL. Selects diagnostic loopback. When LOCLPEN is high, the S3018 device uses the primary data (SERDATI) input. When low, the S3018 device uses the diagnostic loopback data (LPDATI) input.

Test Clock Enable [TSTCLKEN]. TTL. Active High. Enables the reference clock to be used in place of the VCO for testing. Allows a means of testing the functions of the chip without the use of the PLL. Set low for normal operation.

Out of Frame [OOF]. TTL. Indicator used to enable framing pattern detection logic in the S3018. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set low, whichever is longer. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. (See Figures 13 and 14.)

Loss of Signal [LOS]. PECL. Active high. A single-ended 10K ECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When LOS is high, the data on the Serial Data In (SERDATIP/N) pins will be internally forced to a constant zero, LOCKDET will be forced low, and the PLL will lock to the REFCKINP/N inputs.

This signal must be used to assure correct automatic reacquisition to serial data following an interruption and subsequent reconnection of the optical path. This will assure that the PLL does not "wander" out of reacquisition range by tracking the random phase/frequency content of the optical detector's noise floor while monitoring "dark" fiber.

When LOS is low, data on the SERDATIP/N pins will be processed normally.

Reference Clock [REFCKINP/N]. Differential PECL. Input normally used as the reference for the integral clock recovery PLL.

Master Reset [RSTB]. TTL. Reset input for the device, active low. Initializes the device to a known state and forces the PLL to acquire to the reference clock. A reset of at least 16 ms should be applied at power-up and whenever the user wishes to force the PLL to re-acquire to the reference clock. The S3018 will also re-acquire to the reference clock if the serial data input is held quiescent for at least 16 ms.

Reference Select [REFSEL]. TTL. Used to select the reference clock frequency. Set low to select 77.76 MHz. Set high to select 19.44 MHz for applications less demanding than SONET/SDH.

Loop Filter Capacitor [CAP1, CAP2]. The loop filter capacitor is connected to these pins. The capacitor value should be 0.1 μ f \pm 10% tolerance, X7R dielectric. 50 volt is recommended (16 volt is acceptable).

Output Signals

Parallel Output [POUT]<7:0>. TTL. Parallel data bus, a 77.76 Mbyte/sec word, aligned to the parallel output clock (POCLK). POUT<7> is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT<0> is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). POUT<7:0> is updated on the falling edge of POCLK.

Frame Pulse [FP]. TTL. Indicates frame boundaries in the incoming data stream (SERDATI). If framing pattern detection is enabled, as controlled by the OOF input, FP pulses high for one POCLK cycle when a 48 bit sequence matching the framing pattern is detected on the serial data inputs. When framing pattern detection is disabled, FP pulses high when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK.

Parallel Output Clock [POCLK]. TTL. A 77.76 MHz nominally 50% duty cycle, byte rate output clock, that is aligned to POUT<7:0> byte serial output data. POUT<7:0> and FP are updated on the falling edge of POCLK.

Lock Detect [LOCKDET]. TTL. Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming data stream. LOCKDET is an asynchronous output.

OTHER OPERATING MODES

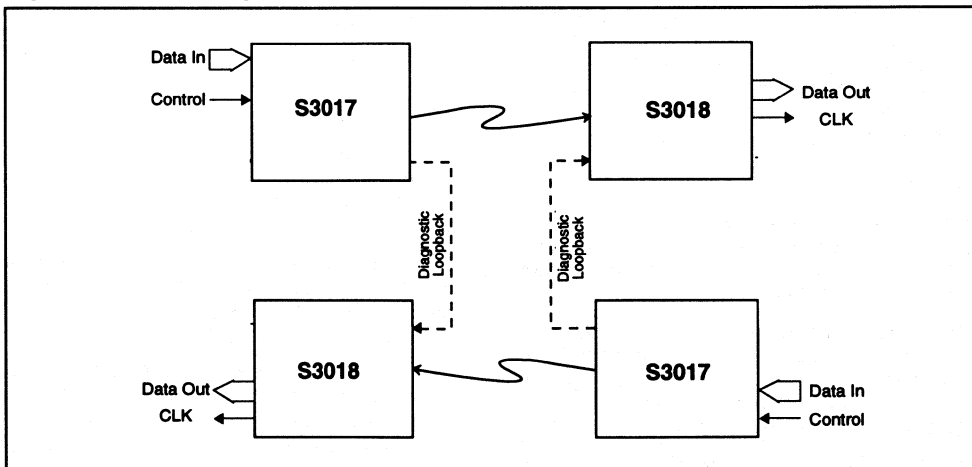
Diagnostic Loopback

The Diagnostic Loopback consists of alternate serial data outputs (in the case of the S3017) and inputs (in the case of the S3018).

On the S3017, the differential PECL output LPDATO provides Diagnostic Loopback serial data. When the Local Loopback Enable (LOCLPEN) input and TCLKSEL are low, this data output is a replica of SERDATO. When LPDATO is connected to the S3018, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. When LOCLPEN is high and TCLKSEL is low, LPDATO is held in the inactive state, with the positive output high and the negative output low. In the inactive state, there will be no interference from the transmitter to the receiver.

On the receiver side, the differential PECL input LPDATI is the Diagnostic Loopback serial data input. When the Local Loopback Enable (LOCLPEN) input is set low, the LPDATI input is routed in place of the normal data stream (SERDATI).

Figure 7. Interface Diagram



PERFORMANCE SPECIFICATIONS

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	
PECL Data Output Jitter OC-12/STS-12			16	ps (rms)	In CSU mode, given 14 ps rms jitter on REFCKIN in 12KHz to 5 MHz band
Reference Clock Frequency Tolerance Clock Synthesis Clock Recovery	-20 -100		+20 +100	ppm ppm	Required to meet SONET output frequency specification
OC-12/STS-12 Capture Range Lock Range		±200ppm +2,-8%			With respect to fixed reference frequency Minimum transition density of 20%
Acquisition Lock Time			16	μsec	With device already powered up and valid reference clock
Reference Clock Input Duty Cycle	30		70	% of period	
Reference Clock Rise & Fall Times			2.0	ns	10% to 90% of amplitude
PECL Output Rise & Fall Times (S3017 LPDATOP/N)			600	ps	20% to 80%, 50 Ω to Vcc -2V equivalent load, 5pF cap
Source Terminated Diff. PECL Compatible Output Rise & Fall Times (S3017 SERDATOP/N)			450	ps	20% to 80%, 100 Ω line to line

7

ABSOLUTE MAXIMUM RATINGS

PARAMETER	Min	Typ	Max	Unit
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Respect to GND	-0.5		+7.0	V
Voltage on Any TTL Input Pin	-0.5		+5.5	V
Voltage on Any PECL Input Pin	VCC-3		VCC	V
TTL Output Sink Current			20	mA
TTL Output Source Current			10	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage		500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	Min	Typ	Max	Unit
Ambient Temperature under Bias	-40		85	°C
Junction Temperature under Bias	-10		+125	°C
Voltage on VCC with Respect to GND	4.75	5.0	5.25	V
Voltage on Any TTL Input Pin	0		VCC	V
Voltage on Any PECL Input Pin	VCC-2		VCC	V
S3017 ICC		178	238	mA
S3018 ICC		216	260	mA

TTL INPUT/OUTPUT DC CHARACTERISTICS
 $(T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, V_{CC} = 5\text{ V } \pm 5\%)$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}^1	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}^1	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
I_{IL}	Input LOW Current	-400.0			μA	$V_{CC} = \text{MAX}, V_{IN} = 0.5\text{V}$
I_{IH}	Input HIGH Current			50.0	μA	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$
I_I	Input HIGH current at Max. VCC			1.0	mA	$V_{CC} = \text{MAX}, V_{IN} = 5.5\text{V}$
I_{OS}	Output Short Circuit Current	-100.0		-25.0	mA	$V_{CC} = \text{MAX}, V_{OUT} = 0.5\text{V}$
V_{IK}	Input Clamp Diode Voltage	-1.2			Volts	$V_{CC} = \text{MIN}, I_{IN} = -18\text{ ma}$
V_{OL}	Output LOW Voltage			0.5	Volts	$V_{CC} = \text{MIN}, I_{OL} = 8\text{ ma}$
V_{OH}	Output HIGH Voltage	2.7			Volts	$V_{CC} = \text{MIN}, I_{OH} = -1\text{ ma}$

1. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

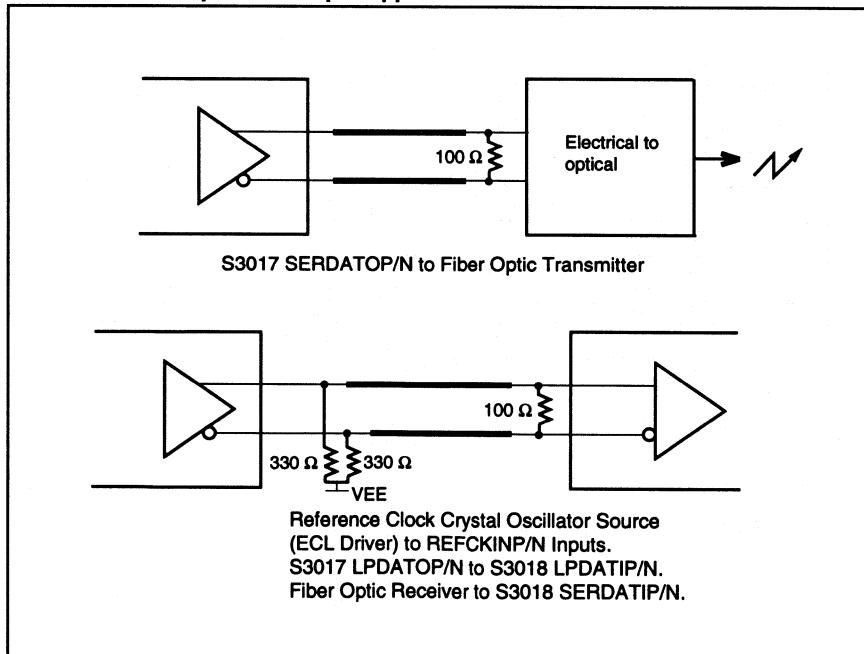
PECL INPUT/OUTPUT DC CHARACTERISTICS^{1,2}

($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}	Input LOW Voltage	$V_{CC} - 2.000$		$V_{CC} - 1.441$	Volts	Guaranteed Input LOW Voltage for single-ended inputs
V_{IH}	Input HIGH Voltage	$V_{CC} - 1.225$		$V_{CC} - 0.570$	Volts	Guaranteed Input HIGH Voltage for single-ended inputs
V_{IL}	Input LOW Voltage	$V_{CC} - 2.000$		$V_{CC} - 0.700$	Volts	Guaranteed Input LOW Voltage for differential inputs
V_{IH}	Input HIGH Voltage	$V_{CC} - 1.750$		$V_{CC} - 0.450$	Volts	Guaranteed Input HIGH Voltage for differential inputs
V_{ID}	Input Diff. Voltage	0.250	0.500	1.400	Volts	Differential Input Voltage
I_{IH}	Input High Current	-0.500		20.000	μA	$V_{ID} = 500\text{mV}$
I_{IL}	Input Low Current	-0.500		20.000	μA	$V_{ID} = 500\text{mV}$
V_{OL}	Output LOW Voltage	$V_{CC} - 2.000$		$V_{CC} - 1.500$	Volts	50 ohm termination to $V_{CC} - 2\text{V}$
V_{OH}	Output HIGH Voltage	$V_{CC} - 1.110$		$V_{CC} - 0.670$	Volts	50 ohm termination to $V_{CC} - 2\text{V}$
V_{OD}	Output Diff. Voltage	0.390		1.330	Volts	Differential Output Voltage

1. These conditions will be met with no airflow.
2. When not used, tie the positive differential PECL pin to V_{CC} and the negative differential ECL pin to ground via a 3.9K resistor.

Differential ECL Input and Output Applications



S3017 Pinouts

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	CAP1	14	TTLVCC	27	TTLGND	40	AVCC0
2	AVEE3	15	ECLVCC	28+	ECLVCC	41	AVEE0
3	AVCC3	16	PCLK	29	PIN4	42	AVEE2
4	TSTCLKEN	17	TTLGND	30	PIN5	43	LPDATON
5	ECLVCC	18	ECLVEE	31	PIN6	44	LPDATOP
6	ECLVEE	19	PIN0	32	ECLVEE	45	SERDATON
7	REFSEL	20	PIN1	33	PIN7	46	AVCC2
8	LOCLPEN	21	ECLVEE	34	NC	47	SERDATOP
9	RSTB	22	PIN2	35	TCLKSEL	48	REFCKINN
10	ECLVEE	23	PIN3	36	ECLVEE	49	REFCKINP
11	TESTRST	24	TTLVCC	37	ECLVCC	50	AVCC4
12	PICLK	25	ECLVCC	38	AVCC1	51	AVEE4
13	TTLGND	26	TTLVCC	39	AVEE1	52	CAP2

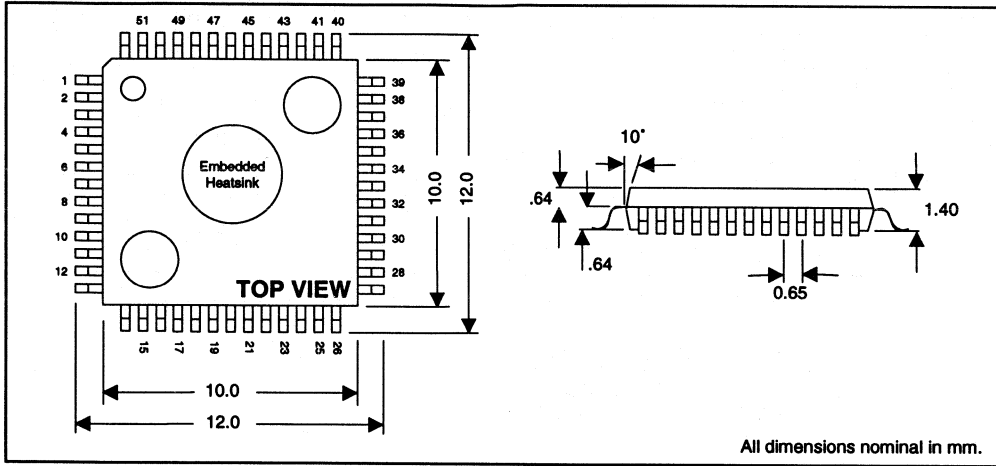
S3018 Pinouts

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	CAP1	14	TTLVCC	27	TTLGND	40	AVCC0
2	AVEE3	15	ECLVCC	28	ECLVCC	41	AVEE0
3	AVCC3	16	POUT1	29	POUT6	42	LPDATIP
4	TSTCLKEN	17	TTLGND	30	POUT7	43	AVEE2
5	ECLVCC	18	ECLVEE	31	OOF	44	LPDATIN
6	ECLVEE	19	POUT2	32	ECLVEE	45	SERDATIP
7	REFSEL	20	POUT3	33	RSTB	46	SERDATIN
8	LOCLPEN	21	ECLVEE	34	LOS	47	AVCC2
9	POCLK	22	POUT4	35	LOCKDET	48	REFCKINN
10	ECLVEE	23	POUT5	36	ECLVEE	49	REFCKINP
11	FP	24	TTLVCC	37	ECLVCC	50	ECLVCC
12	POUT0	25	ECLVCC	38	AVCC1	51	NC
13	TTLGND	26	TTLVCC	39	AVEE1	52	CAP2

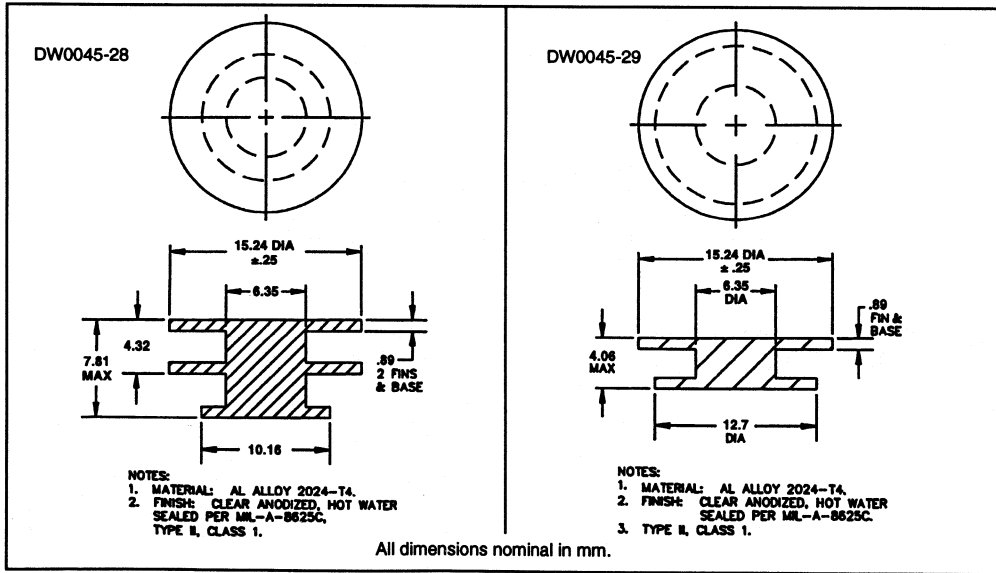
Power Supply Connections:

AVCC0, AVCC1, AVCC2, AVCC3, AVCC4	=	ANALOG+5V
AVEE0, AVEE1, AVEE2, AVEE3, AVEE4	=	ANALOG 0V
ECLVCC, TTLVCC	=	DIGITAL +5V
ECLVEE, TTLGND	=	DIGITAL 0V
N.C.	=	NOT CONNECTED

Figure 8. 52-pin PQFP Package



Heatsinks DW0045-28 and DW0045-29



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Thermal Management

Device	Power	Θ _{ja} Still Air w/ DW0045-28 Heatsink	Max Still Air ¹ w/ DW0045-28 Heatsink	Required Air ² w/ DW0045-29 Heatsink
S3017	1.25W	32.7°C/W	89°C	100 LFPM
S3018	1.36W	32.7°C/W	85°C	100 LFPM

Notes:

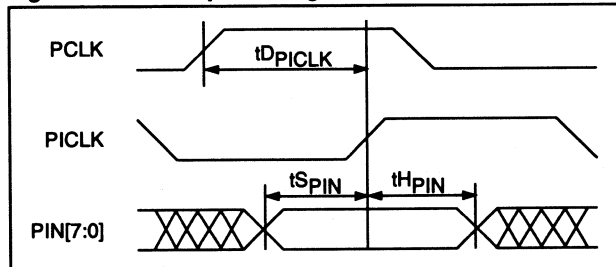
1. Max ambient temperature permitted in still air to maintain T_J <130°C.
2. Airflow required in 85°C ambient conditions to maintain T_J <130°C.

Table 2. S3017 AC Timing Characteristics

($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Symbol	Description	Min	Typ	Max	Units
t_{DPICK}	PICKL Delay from PCLK	0		5.5	ns
t_{SPIN}	PIN [7:0] Set-up Time w.r.t. PICKL	2			ns
t_{HPIN}	PIN [7:0] Hold Time w.r.t. PICKL	1			ns
$t_{D_{SER}}$	Serial Clock (LPDATOP) Low to SERDATOP/N Valid Prop Delay	0		500	ps
	Serial Clock (LPDATOP) Duty Cycle	40		60	%
t_{DRP}	REFCKINP High to PCLK High Valid Prop Delay	7.0		11.0	ns

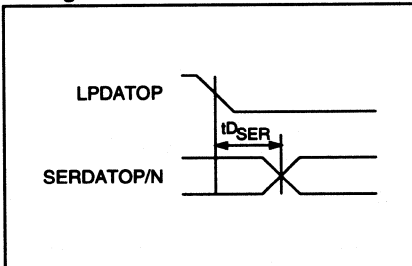
Figure 9. PIN AC Input Timing



Notes on TTL Output Timing:

1. When a set-up time is specified on TTL signals between an input and a clock, the set-up time is the time in nanoseconds from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on TTL signals between an input and a clock, the hold time is the time in nanoseconds from the 50% point of the clock to the 50% point of the input.

Figure 10a. Clock and Data Output Timing with TSCLKSEL Asserted



Notes on PECL Output Timing:

1. Output propagation delay time of high speed PECL outputs is the time in nanoseconds from the cross-over point of the reference signal to the cross-over point of the output.

Figure 10b. REFCKIP High to PCLK High Valid Prop Delay

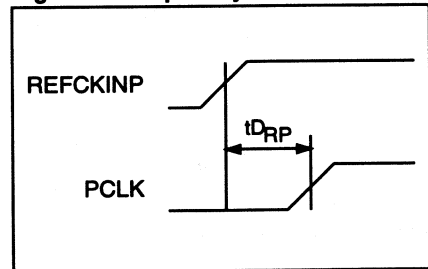
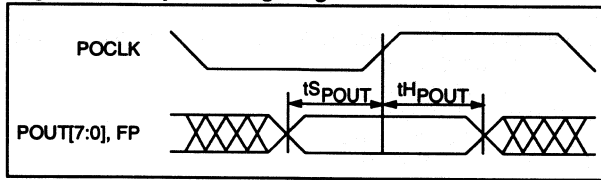


Table 3. S3018 AC Timing Characteristics

($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Symbol	Description	Min	Typ	Max	Units
	POCLK Duty Cycle	40		60	%
$t_{S_{POUT}}$	POUT[7:0] and FP Set-up Time w.r.t. POCLK	3			ns
$t_{H_{POUT}}$	POUT[7:0] and FP Hold Time w.r.t. POCLK	2			ns
	SERDATIP/N Minimum Pulse Width	400			ps

Figure 11. Output Timing Diagram



Notes on TTL Output Timing:

1. Output propagation delay time of TTL outputs is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays and duty cycles of TTL outputs are measured with a 15 pF load and 500 ohms to ground on the outputs.

RECEIVER FRAMING

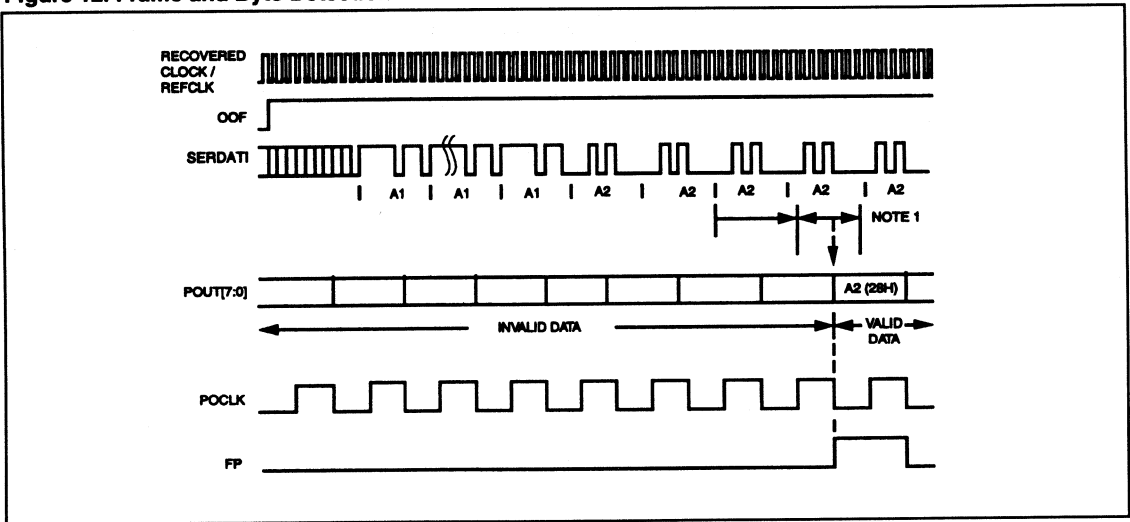
Figure 12 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is high. Realignment occurs upon receipt of the first A1 byte. The frame boundary is recognized upon receipt of the third A2 byte, which is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUT[7:0]). Concurrently, the frame pulse is set high for one POCLK cycle.

When interfacing with a section terminating device, the OOF input remains high for one full frame after the first frame pulse while the section terminating device verifies internally that the frame and byte alignment are correct, as shown in Figure 13. Since at least one framing pattern has been detected since the rising edge of OOF, boundary detection is disabled when OOF is set low.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse or until OOF goes low, whichever occurs last. Figure 13 shows a typical OOF timing pattern which occurs when the S3018 is connected to a down stream section terminating device. OOF remains high for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes low.

Figure 14 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 12. Frame and Byte Detection



NOTE 1: Range of input to output delay can be 1.5 to 2.5 POCLK cycles

Figure 13. OOF Operation Timing with PM5312 STTX or PM5355 SUNI-622

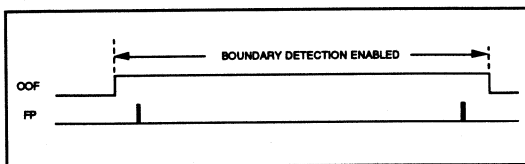
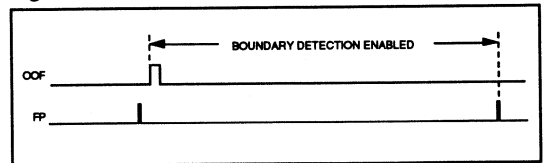


Figure 14. Alternate OOF Timing



S3017 WITH DATA CLOCK SYNCHRONOUS TO REFERENCE CLOCK

INTRODUCTION

In some applications it is necessary to “forward clock” the data in a SONET/SDH system. In this application the reference clock from which the high speed serial clock is synthesized and the parallel data clock both originate from the same (usually TTL/CMOS) clock source. This application note explains how the AMCC S3017 can be configured to operate in this mode.

Clock Control Logic Description

The timing control logic in the S3017 automatically generates an internal load signal which has a fixed relationship to the reference clock. The logic takes into account the variation of the reference clock to the internal load signal over temperature and voltage.

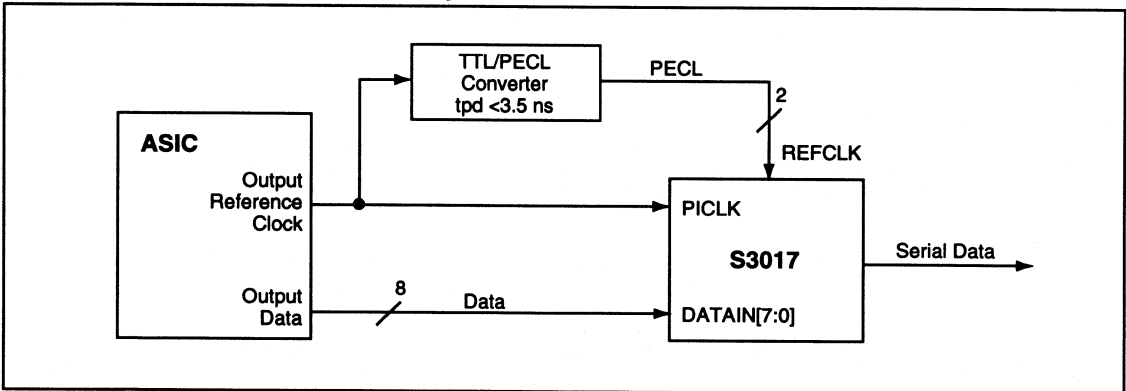
The connections required to implement the design are shown in Figure 15, and the timing specifications are

shown in Figure 16. The setup and hold times for the PICKLK to the data must be met by the controller ASIC. We recommend latching the data on the falling edge of the output reference clock in order to meet the required specifications.

Possible Problems

In order to meet the jitter generation specifications required by SONET, the jitter of the reference clock must be minimized. It may be difficult to meet the SONET jitter generation specifications using a reference clock input with a TTL reference source.

Figure 15. S3017 with Data Clocked by Reference Clock



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Figure 16. Data Timing with Respect to PICKLK

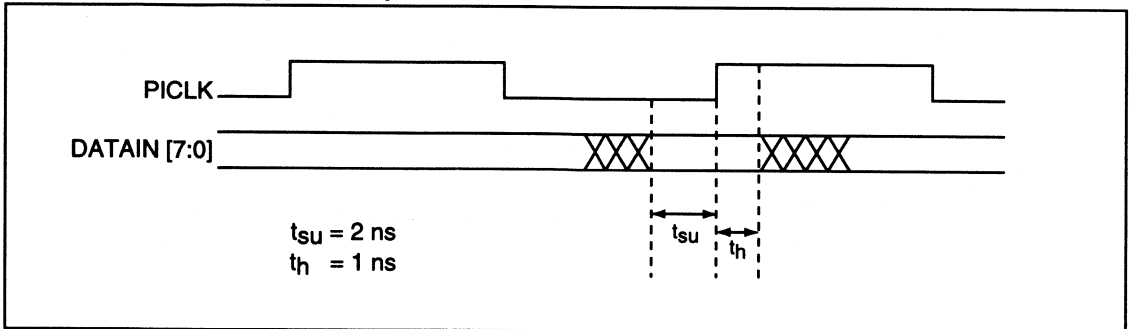
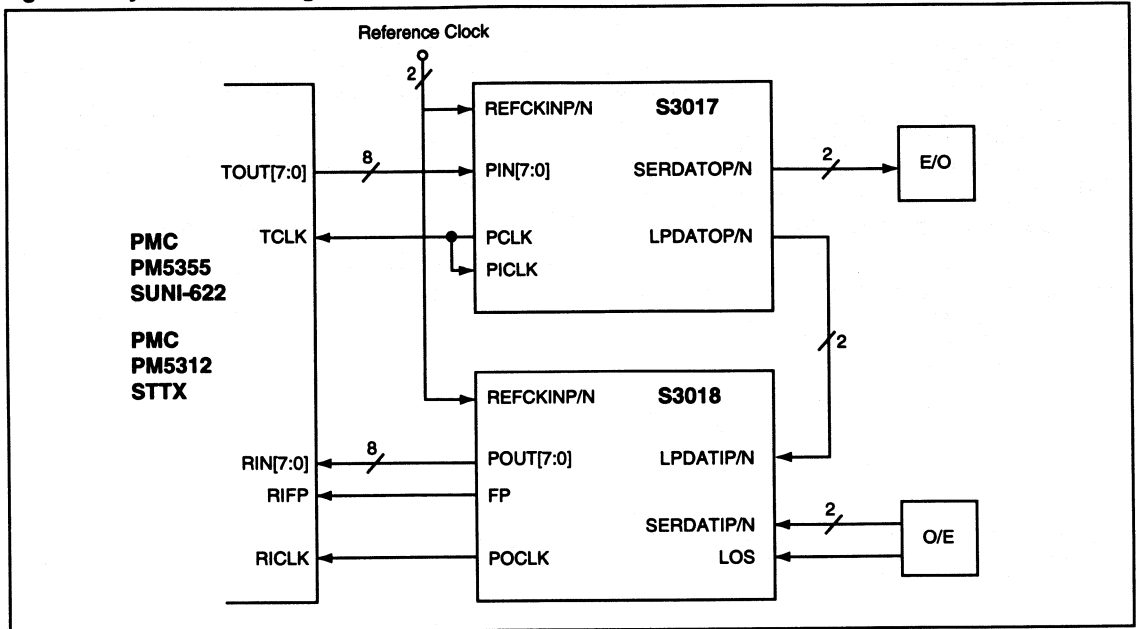


Figure 17. System Block Diagram



Ordering Information

GRADE	TRANSMITTER	PACKAGE	HEATSINK
S – Commercial/ Industrial	3017	A – 52 PQFP TEP	H1 – w/DW0045-28 heatsink unattached
		C – Bare Die	H2 – w/DW0045-29 heatsink unattached

GRADE	RECEIVER	PACKAGE	HEATSINK
S – Commercial/ Industrial	3018	A – 52 PQFP TEP	H1 – w/DW0045-28 heatsink unattached
		C – Bare Die	H2 – w/DW0045-29 heatsink unattached

X XXXX X / XX
 Grade Part number Package Heatsink (Heatsink identifier not marked on part)

OVERVIEW

The S6007 Evaluation Manual describes two evaluation boards that allow demonstration of AMCC's S3017 and S3018 STM-4/OC-12 SONET/SDH/ATM interface circuits. This document provides information on board contents and layout. It should be used in conjunction with the S3017/S3018 data sheet, which contains full technical details on chip operation.

Figure 1 depicts a block diagram of board connectivity for parallel input to parallel output evaluation, while Figure 2 illustrates the connectivity required for serial input to serial output evaluation. Power is supplied to the boards from external supplies connected through the on-board power connectors. Connectors and dip switches allow easy access to all of the interface signals on the S3017/S3018 chips. All required external circuitry, including translation buffers and all passive components, are included on the boards.

Separate boards are provided for the S3017 and the S3018 chips. Layouts for both boards are depicted in Figures 3 and 4, showing the location of connectors, dip switches and components.

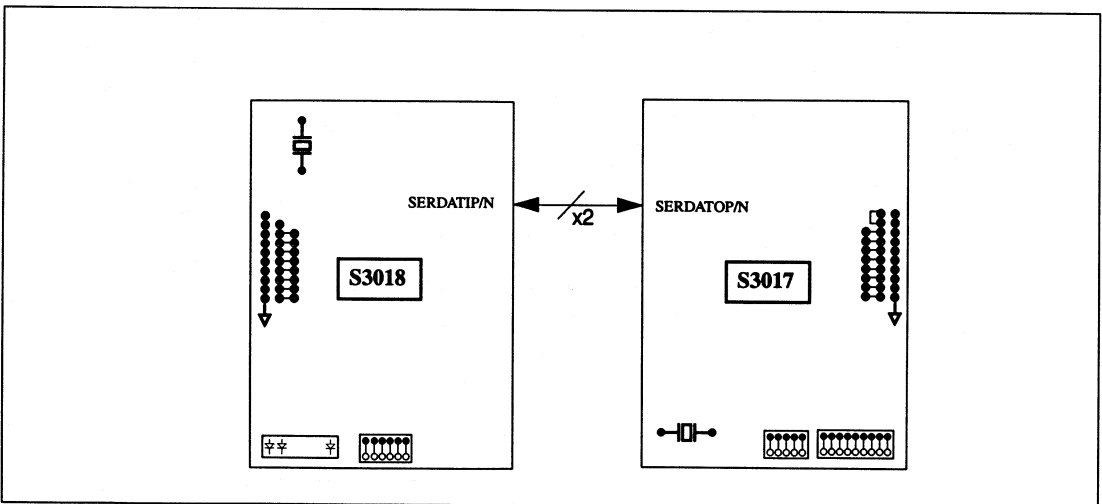
Power Connections

Connections are provided on the board for VCC, ground (GND) and output buffer supplies VCC016 and VEE016. VCC016 and VEE016 are used for level translation between the S3017 device and external test equipment or other standard ECL or +5V Referenced ECL interface circuitry. The buffers that interface to the S3017 and S3018 inputs AC couple and translate between standard ECL and/or +5V referenced ECL to supply the correct +5v referenced ECL levels to the devices. Table 1 illustrates the nominal input voltages for VCC and GND, and gives three possible configurations (vertically aligned) for powering up VCC016 and VEE 016.

Table 1. Power Connections for Test Equipment Interface

Power Supply	Nominal Input Voltage
VCC	5.0V
GND	0.0V
VCC016	2.0V 5.0V 0.0V
VEE016	-3.0V 0.0V -5.0V

Figure 1. S3017 In/S3018 Out Parallel Interface Setup Block Diagram



S3017 Signals

A top level view of the S3017 board is illustrated in Figure 3. The dip switch labeled S1 provides access to all of the S3017 control signals, while Header H1 and dip switch S2 provide access to the TTL input signals PIN[7:0], the parallel input clock PCLK and the output clock PCLK. The OFF position on the dip switches corresponds to a logic 0, while the ON position corresponds to a logic 1.

When it is desired to evaluate the S3017 in a stand-alone mode, jumper H1-A to H1-B for signals PIN[7:0] and jumper PCLK (H1-B) to PCLK (H1-B). In this configuration, the PIN[7:0] inputs can be controlled using the dip switch S2.

When it is desired to interface the S3017 to the S3018 for testing parameters such as jitter tolerance (serial into the S3018, parallel out fed back to the parallel inputs of the S3017 and then monitoring the serial output of the S3017), connect the QC-1 jumper block that is included with the board, as shown in Figure 2.

When the RSTB push button switch is depressed, the S3017 goes into RESET mode and the part will remain in this mode until the button is released.

S3018 Signals

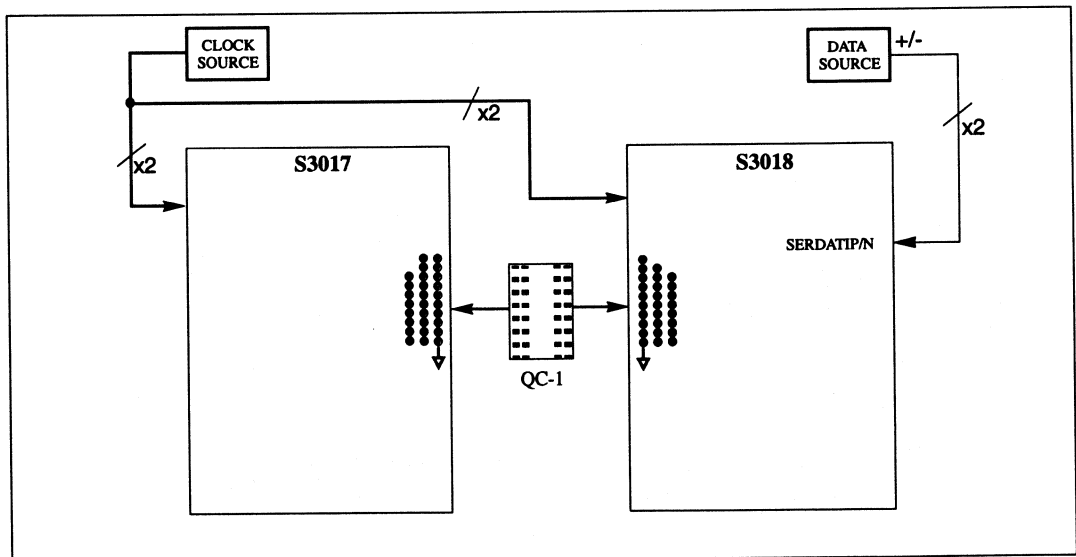
A top level view of the S3018 board is illustrated in Figure 4. The dip switch labeled S3 provides access to all of the S3018 control signals, while Header H2 and LED bank U1 provide access to the TTL output signals POUT[7:0], the output clock POCLK and the LOCKDET output.

When it is desired to evaluate the S3018 in a stand-alone mode, jumper header pins H2-B to H2-C for all of the POUT pins and the LEDs will turn on for each occurrence of a 1 and off for each occurrence of a 0. Another option is to create a ribbon cable or to use single discrete cables attached to the header H2-B pins and then connect the TTL outputs to a SONET analyzer or a standard logic analyzer.

When it is desired to interface the S3018 to the S3017 for testing parameters such as jitter tolerance (serial into the S3018, parallel out fed back to the parallel inputs of the S3017 and then monitoring the serial outputs of the S3017), connect the QC-1 jumper block that is included with the board, as shown in Figure 2.

When the RSTB push button switch is depressed, the S3017 goes into RESET mode and the part will remain in this mode until the button is released.

Figure 2. S3018 In - S3017 Out Serial Interface Setup - Block Diagram

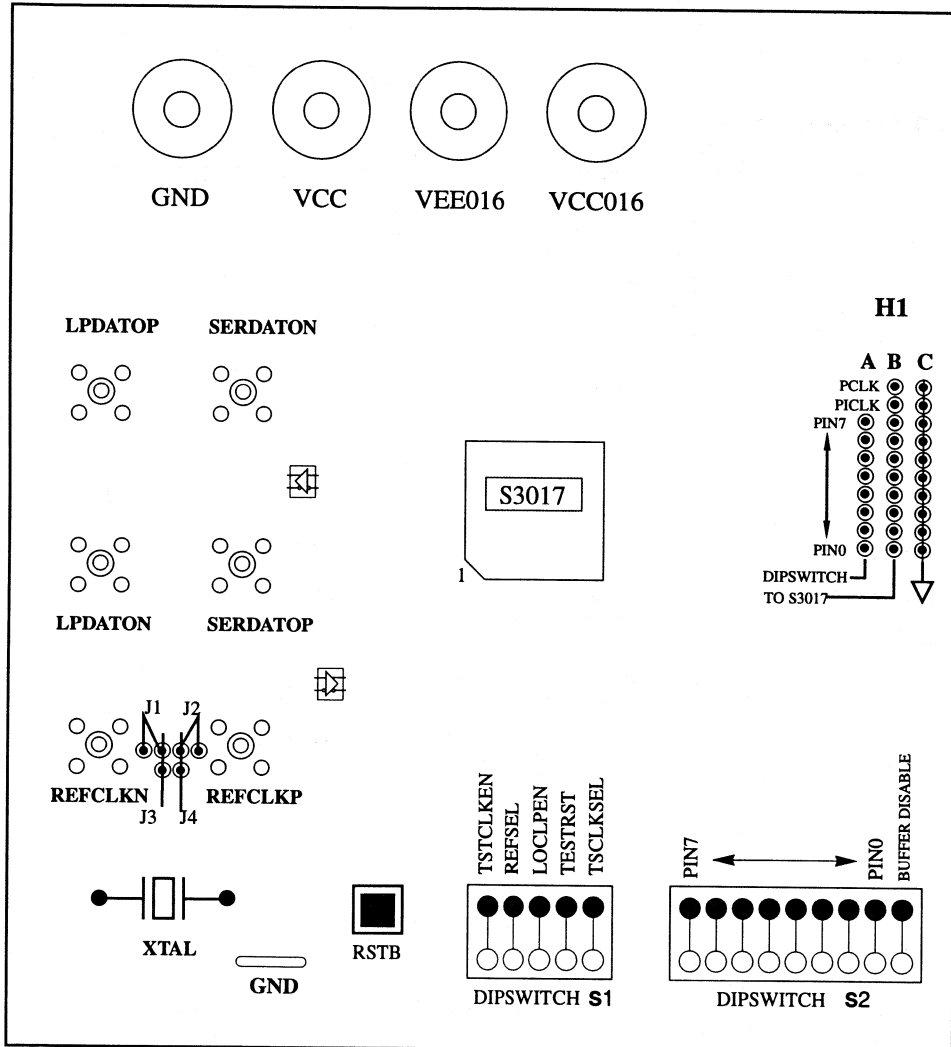


CRYSTAL REFERENCES AND CLOCK GENERATION

One 77.76 MHz crystal is provided for each board. If 19.44 MHz crystals are needed, AMCC can recommend crystal vendors.

19.44 MHz or 77.76 MHz differential ECL crystal oscillators with 100-ppm stability should be used for the reference clocks.

Figure 3. S3017 Board Layout



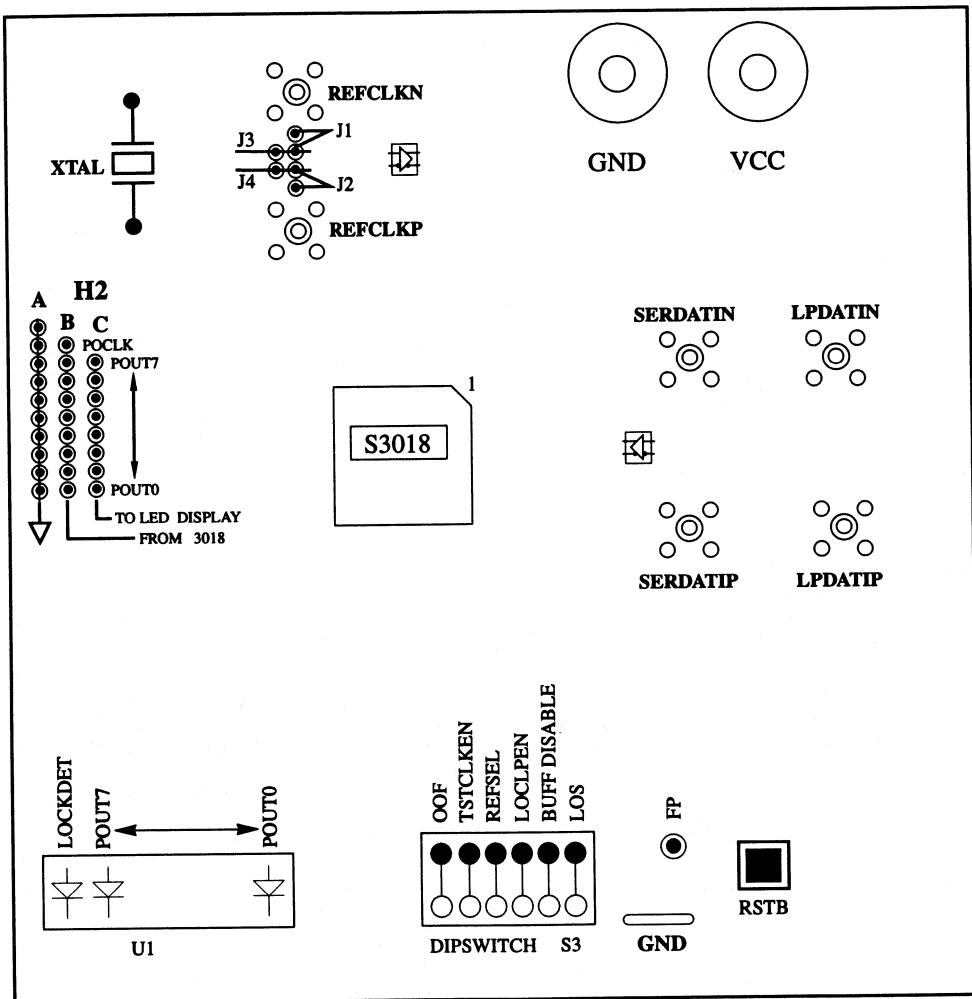
JUMPER CONFIGURATION

The jumpers labeled J1 - J4 on both boards allow the user to control whether an on-board crystal reference or external clock reference is used. Jumpers J1 and J2 must be installed when an external reference is used (input into the REFCLKP/N SMAs), while jumpers J3 and J4 must be installed to use the on-board crystal reference.

SMA CONNECTIONS

SMA connections provide input/output capability for a number of signals, including all serial data I/O and the reference clocks. All of these connectors are labeled on the boards and are also shown in Figures 3 and 4.

Figure 4. S3018 Board Layout



FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLLs for clock generation and clock recovery
- Supports 155.52 MHz (OC-3) and 622.08 Mbit/s (OC-12)
- Selectable reference frequencies of 19.44 or 77.76 MHz
- Interface to both PECL and TTL/CMOS logic
- 8-bit TTL/CMOS datapath
- Compact 52 PQFP package
- Diagnostic loopback mode
- Lock detect
- Low jitter PECL interface
- < .65 watt typically

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add drop multiplexors
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3019 SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET OC-12 (622.08 Mbit/s) and OC-3 (155.52 Mbit/s) interface device. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3019 transceiver chip allowing the use of a slower external transmit clock reference. Clock recovery is performed on the device by synchronizing its on-chip VCO directly to the incoming data stream. The S3019 also performs SONET/SDH frame detection. The chip can be used with a 19.44 or 77.76 MHz reference clock, in support of existing system clocking schemes.

The low jitter PECL interface guarantees compliance with the bit-error rate requirements of the Bellcore, ANSI, and ITU-T standards. The S3019 is packaged in a 52 PQFP, offering designers a small package outline.

Figure 1. Link Diagram

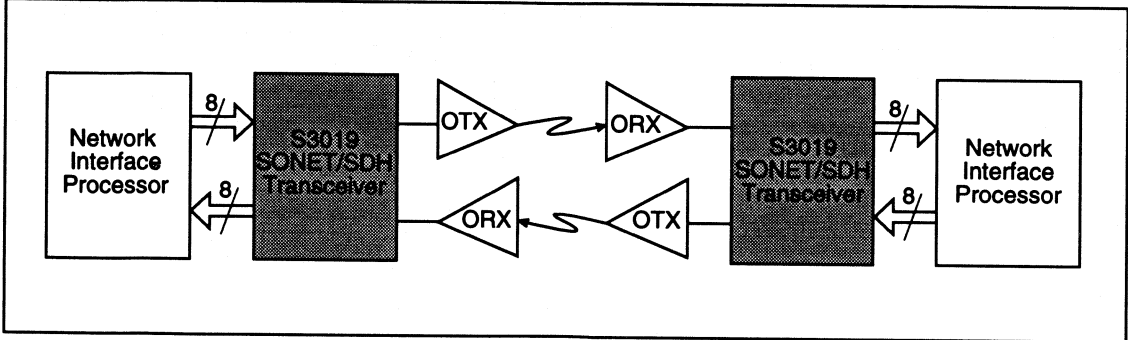
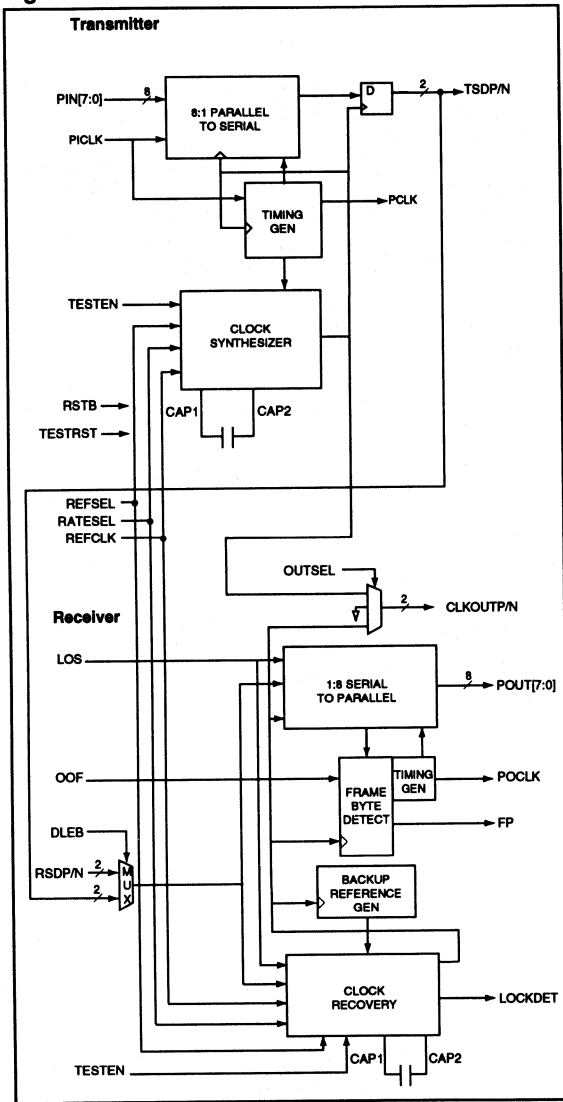


Figure 4. S3019 Transceiver



S3019 OVERVIEW

The S3019 transceiver implements SONET/SDH serialization/deserialization, transmission, and frame detection/recovery functions. The block diagram in Figure 4 shows basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation and recovery, and system timing. The system timing circuitry consists of management of the datastream, framing, and clock distribution throughout the front end.

The S3019 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:

1. 8-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

1. Clock and data recovery from serial input
2. Frame detection
3. Serial-to-parallel conversion
4. 8-bit parallel output

A lock detect feature is provided on the S3019, which indicates that the PLL is locked (synchronized) to the incoming data stream, and facilitates continuous down-stream clocking in the absence of data.

Suggested Interface Devices

PMC PM5312	STTX	SONET/SDH Tranport Term.	Transceiver
PMC PM5355	SUNI-622	Satum User Network Interface	
AT&T ASTROTEC1227/1230		650 Mbit/s	Fiber Optic Transmitter
Mitsubishi MF-622DF-T12-XXX		622 Mbit/s	Fiber Optic Transmitter
Sumitomo ES-9304-TD		622 Mbit/s	Fiber Optic Transmitter
AT&T ASTROTEC 1310		650 Mbit/s	Fiber Optic Receiver
Mitsubishi MF-622DS-R1X-XXX		622 Mbit/s	Fiber Optic Receiver
Sumitomo ES-9216-RD		622 Mbit/s	Fiber Optic Receiver

FEATURES

- Performs serial to parallel conversion for SONET STS-12 or STS-3 data streams.
- Operates at equivalent SDH data rates for processing STM-4 or STM-1 data streams.
- Converts a 622 Mbit/s or 155 Mbit/s bit serial stream into a 78 Mbyte/s or 19 Mbyte/s 8-bit byte serial data stream, respectively.
- Performs partial framing to A1 and A2 bytes.
- Checks for three A1 bytes followed by three A2 bytes as required for SONET/SDH or optionally checks for a single A1 byte followed by a single A2 byte as required for 139 Mbit/s ATM interfaces.
- Selectable Coded Mark Inversion (CMI) line decoding for STS-3 electrical interfaces at 155 Mbit/s and 139 Mbit/s ATM interfaces.
- Performs parallel to serial conversion for SONET STS-12 or STS-3 data streams.
- Operates at equivalent SDH data rates for processing STM-4 or STM-1 data streams.
- Converts a 78 Mbyte/s or 19 Mbyte/s 8-bit byte serial data stream into a 622 Mbit/s or 155 Mbit/s bit serial stream, respectively.
- Selectable Coded Mark Inversion (CMI) line encoding for STS-3 electrical interfaces at 155 Mbit/s and 139 Mbit/s ATM interfaces.
- Supports diagnostic (transmit to receive) loopback and line (receive to transmit) loopback modes.
- Directly interfaces to the PMC-Sierra PM5301 SSTX SONET/SDH Section Terminating Transceiver device, the PM5312 STTX SONET/SDH Transport Terminating Transceiver, and the PM5355 SUNI-622 Saturn User Network Interface devices.
- Simple TTL/CMOS-level interface on the low speed side, ECL-level (100K) on the high speed side.
- +5 Volt, -4.5 Volt power supplies.
- 120-pin Thermally Enhanced Package (TEP).

APPLICATIONS

- Section Repeaters
- Add-Drop Multiplexers
- Broadband Cross-Connects
- ATM Switching Systems
- Fiber Optic Terminals
- Fiber Optic Test Equipment

Figure 1. S3022 Block Diagram

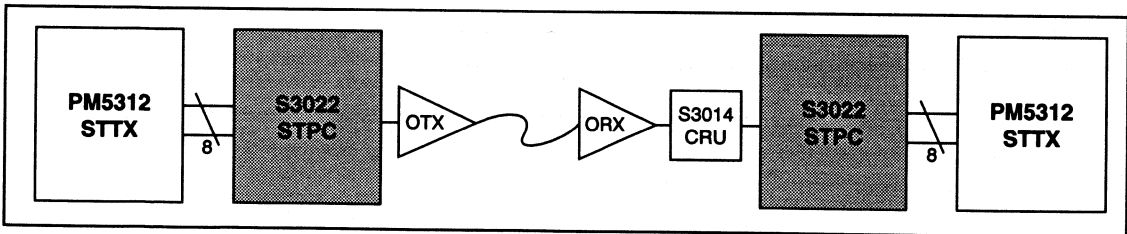
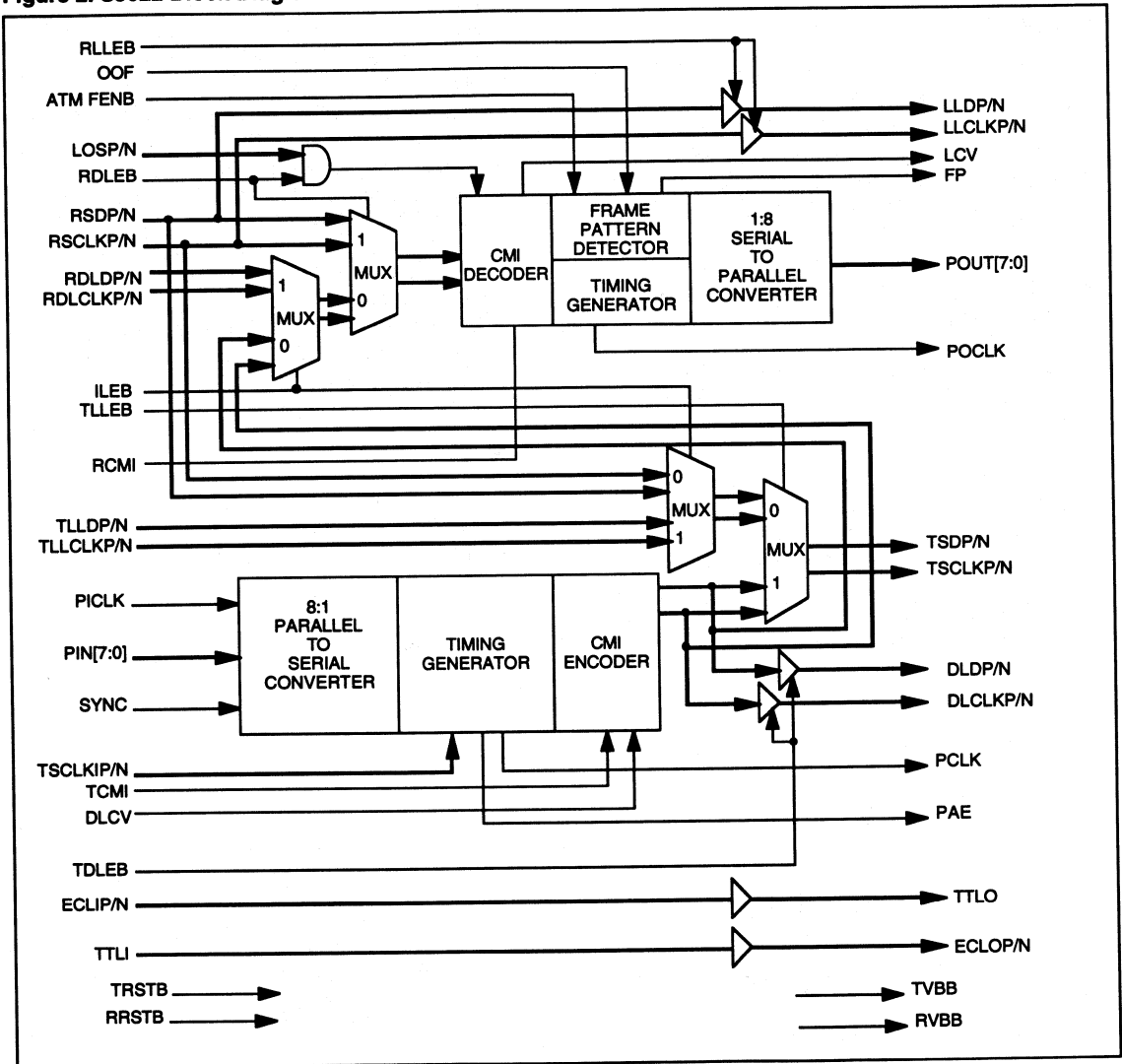


Figure 2. S3022 Block Diagram



GENERAL DESCRIPTION

The S3022 STPC SONET/SDH Serial to Parallel/Parallel to Serial Converter is a fully integrated high speed Synchronous Optical Network (SONET) compatible front and back end. It is also fully compatible with the CCITT Synchronous Digital Hierarchy (SDH) standards for STM-4 and STM-1 operation.

The STPC serial to parallel converter section provides the first stage of digital processing of a receive SONET STS-12 or STS-3 bit-serial stream. The STPC converts the bit-serial 622 Mbit/s or 155 Mbit/s data stream into a 78 Mbyte/s or 19 Mbyte/s byte-serial data format. A Coded Mark Inversion (CMI) decoder can be enabled during 155 Mbit/s operation for decoding STS-3 or 139 Mbit/s ATM electrical signals. CMI mode is selected by an input pin.

The STPC parallel to serial converter section provides the last stage of digital processing of a transmit SONET STS-12 or STS-3 bit-serial stream. The STPC converts the 78 Mbyte/s or 19 Mbyte/s byte-serial data stream into a bit-serial 622 Mbit/s or 155 Mbit/s data format. A Coded Mark Inversion (CMI) encoder can be enabled during 155 Mbit/s or 139 Mbit/s ATM for encoding STS-3 electrical signals. CMI mode is selected by an input pin.

The STPC is designed to interface with the PMC-Sierra PM5301 SSTX SONET/SDH Section Terminating Transceiver which performs frame confirmation, descrambling, and other processing of the receive data stream and performs frame insertion, scrambling, and other processing of the transmit data stream.

Clock recovery is performed external to the STPC device and the recovered clock must be provided to the STPC serial to parallel converter section. High speed clock generation is also performed external to the STPC device and the high speed transmit clock must be provided to the STPC parallel to serial converter section.

Loopback mode enable and signal pins are provided for diagnostic loopback (transmitter to receiver) and line loopback (receiver to transmitter) functions. These signal paths may be implemented internally or external pins may be utilized to implement such loopbacks.

FUNCTIONAL DESCRIPTION

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format consists of three transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 3 overhead and 87 SPE bytes is repeated 9 times in each frame. The first byte in the frame is the overhead A1 (F6H) framing byte. The next is the A2 (28H) framing byte. All bytes, except for A1, A2, and one subsequent overhead byte, are scrambled.

For STS-3 or STM-1, the number of bytes is tripled, so that there are 9 overhead bytes followed by 261 SPE bytes, repeated 9 times per frame. The frame signature becomes three A1 bytes followed by three A2 bytes. For STS-12 or STM-4, the frame signature becomes twelve A1 bytes followed by twelve A2 bytes.

The Frame and Byte Boundary Detection block searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. This pattern occurs in both STS-3 and STS-12. Framing pattern detection is enabled and disabled by the out of frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration OOF is set high. It is disabled when a framing pattern is detected and OOF is no longer set high. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (RSD or DLD). The timing generator block takes the byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). The frame boundary is reported on the frame pulse (FP) output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an STS-3 or STS-12 stream will generate the 48-bit framing pattern is extremely small. It is very improbable for a mimic pattern to occur within one frame of data. Therefore, the time to find the first frame pattern and to verify it with downstream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 μ s, even for extremely high bit error rates.

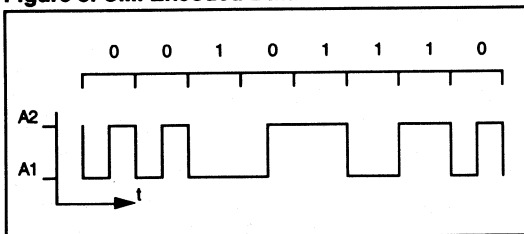
Once downstream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input should be set low to disable the frame search process from trying to synchronize to a mimic frame pattern.

Serial To Parallel Converter

The Serial To Parallel Converter block consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the receive serial clock. The second is an 8-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the Serial to Parallel converter can vary from 1.5 to 2.5 byte periods (12 to 20 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial to parallel converter is that POCLK is neither truncated nor extended during reframe sequences.

Figure 3. CMI Encoded Data



CMI Decoder

The Code Mark Inversion (CMI) Decoder block converts CMI encoded data to NRZ data. The CMI format ensures at least one data transition per bit period, thus aiding the clock recovery process. Zeros are represented by a Low state for one half a bit period, followed by a High state for the next half bit period. Ones are represented by a steady Low or High state for a full bit period. The state of the one's bit period alternates at each occurrence of a one. The STS-3 electrical interface is specified to have CMI coded data. Figure 3 shows an example of CMI encoded data.

The CMI decoder accepts serial data from the receive stream at a rate of 311.04 MHz, decodes the data from CMI format to NRZ format, and shifts it out at a rate of 155.52 Mbit/s. The decoder is only in the data path when the STS-3 CMI mode is selected.

CMI coding violations, such as a corrupted bit represented by a high logic level followed by a low logic level, or two consecutive ones represented by the same logic level, result in a pulse on the LCV output. Each LCV pulse is asserted for one POCLK period and is aligned to the byte on POUT[7:0] containing the line code violation.

The CMI decoder assumes one of two phase alignments as required to correctly process CMI encoded data. If an excessive number of closely spaced line code violations occur, the CMI decoder assumes that it is incorrectly phase aligned to bit boundaries and switches to the alternate phase alignment for subsequent decoding. At bit error rates below 10^{-3} , the error multiplication incurred is negligible.

Note that there will be four LCV's reported when a phase adjustment is made.

Diagnostic Loopback

The Diagnostic Loopback circuitry consists of alternate serial data inputs which can be connected to the serial output of a SONET transmitter, or connected internally to set up a transmit to receive loopback.

The differential ECL input RDLD is the Diagnostic Loopback serial data input. When the Receive Diagnostic Loopback Enable (RDLEB) input is set low and Internal Loopback Enable (ILEB) is set high, the RDLD input is routed in place of the normal data stream (RSD). Similarly, the RDLCLK input replaces the RSCLK input. When DLD and DLCLK outputs are connected to the RDLD and RDLCLK inputs and TDLEB and RDLEB are low, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes.

When the Receive Diagnostic Loopback Enable (RDLEB) input is set low, and Internal Loopback Enabled (ILEB) is set low, the output of the parallel to serial converter section is routed in place of the normal data stream (RSD). Similarly, the STPC transmit serial clock replaces the RSCLK input. An internal loopback from the transmitter to receiver at the serial data rate is set up for diagnostic purposes, without any external connections necessary.

When TDLEB is set high, RDLD and RDLCLK outputs are inactive.

Line Loopback

The Line Loopback circuitry consists of alternate clock and data output drivers. The Line Loopback Clock (LLCLK) and Line Loopback Data (LLD) outputs may be connected to the Line Loopback inputs of a SONET receiver device or internally to establish a receive to transmit loopback.

The differential ECL input TLLD is the Line Loopback serial data input. When the Transmit Line Loopback Enable (TLLEB) input is set low and with the Internal Loopback disabled (ILEB set high), the TLLD inputs are routed in place of the normal internal data stream. Similarly, the TLLCLK inputs replaces the TSCLKI inputs. When the LLD and LLCLK outputs are connected to the TLLD and TLLCLK inputs with the TLLEB set low and ILEB set high, a loopback from the receiver to transmitter at the serial data rate can be set up for line loopback purposes.

When the Transmit Line Loopback Enable (TLLEB) input is set low, with the Receive Line Loopback enabled (RLLEB set low), and Internal Loopback enabled (ILEB set low), the receive serial data (RSD) input is routed in place of the normal internal data stream. Similarly, the receive clock (RSCLK) input replaces the TSCLKI input. When TLLEB and ILEB are low, a loopback from the receiver to transmitter at the serial data rate can be set up for line loopback purposes, without any external connections necessary.

When RLLEB is low, LLD and LLCLK outputs are enabled. When RLLEB is high, LLD and LLCLK outputs are disabled.

Timing Generation

The Timing Generation block provides three separate functions. It generates a byte rate version of TSCLKI, generates an internal byte rate clock which loads the parallel to serial shift register, and provides a mechanism for aligning the phase between the incoming byte clock and the clock which loads the parallel to serial shift register.

The PCLK output is a byte rate version of TSCLKI. In normal mode, PCLK is equal to TSCLKI divided by eight, and in CMI mode, PCLK is equal to TSCLKI divided by sixteen. PCLK is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits, such as the PM5301 SSTX SONET/SDH Section Terminating Transceiver. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the STPC device. PCLK is generated by a free running divider that is clocked by TSCLKI.

In the parallel to serial conversion process, the incoming data is passed from the PCLK byte clock timing domain to the internally generated byte clock timing domain, which is phase aligned to TSCLKI. Although the frequency of PCLK and the internally generated byte clock must be identical, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PCLK and the internally generated byte clock. Should the magnitude of the phase difference be less than one TSCLKI bit period, and if the SYNC input is high, the timing block inverts the internal byte clock.

Since the inversion of the internal byte clock will corrupt one byte of data, SYNC should be held low except when a phase correction is desired. When a timing domain phase difference of less than one bit period is detected, the Phase Alignment Event output (PAE) pulses high for one PCLK clock period. If the condition persists, PAE will remain high. When PAE conditions occur, SYNC should be activated until the condition is no longer present. Upon reset, the internal byte clock is aligned to be 180° out of phase with respect to PCLK.

Parallel To Serial Converter

The Parallel to Serial converter block is comprised of two byte-wide registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PCLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

An internally generated byte clock, which is phase aligned to TSCLKI as described in the Timing Generator block description, activates the parallel data transfer between registers. In normal mode, the serial data shifts out of the second register and into the output selection logic at the TSCLKI rate. In CMI mode, the serial data shifts out of the register and into the CMI encoder at one half the TSCLKI rate (normally 155.52 Mbit/s). The data from the CMI encoder shifts into the output selection logic at the TSCLKI rate (normally 311.04 Mbit/s). The CMI input controls whether the CMI encoder is in the data path.

CMI Encoder

The CMI encoder accepts serial data from the Parallel To Serial Converter block at 155.52 bit/s, encodes the data into CMI format, and shifts the result out at the 311.04 MHz rate of TSCLKI. The encoder is only in the data path when CMI mode is selected. A single CMI violation can be inserted for diagnostic purposes by applying a low to high transition on DLCV. This violation is either an inverted zero code or an inversion of the alternating ones logic level, depending on the state of the data. Subsequent one codes take into account the induced violation to avoid error multiplication.

FUNCTIONAL TIMING

Figure 4 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is high. Both boundaries are recognized upon receipt of the third A2 byte which is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUT[7:0]). Concurrently, the frame pulse is set high for one POCLK cycle.

When interfacing with a PM5301 SSTX device, the OOF input remains high for one full frame after the first frame pulse while the SSTX verifies internally that the frame and byte alignment are correct, as shown in Figure 4. Since at least one framing pattern has been detected since the rising edge of OOF, boundary detection is disabled when OOF is set low.

OOF Operation Timing

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse or until OOF goes low, whichever occurs last. Figure 5 shows a typical OOF timing pattern which occurs when the SPTC is connected to a down stream PM5301 SSTX device. OOF remains high for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes low.

Alternate OOF Timing

Figure 6 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 7 shows the input timing between the parallel input clock (PCLK) and the parallel input data (PIN[7:0]). PIN[7:0] data is sampled on the rising edge of the PCLK.

Pin[7:0] Input Timing

The timing relationship between the input line/diagnostic loopback clock (TLLCLK/RDLCLK) and the line/diagnostic loopback data (TLLD/RDL) is shown in Figure 8a. TLLD is sampled on the rising edge of the TLLCLK clock input and RDL is sampled on the rising edge of the RDLCLK clock input.

Figure 4. Frame and Byte Detection Timing

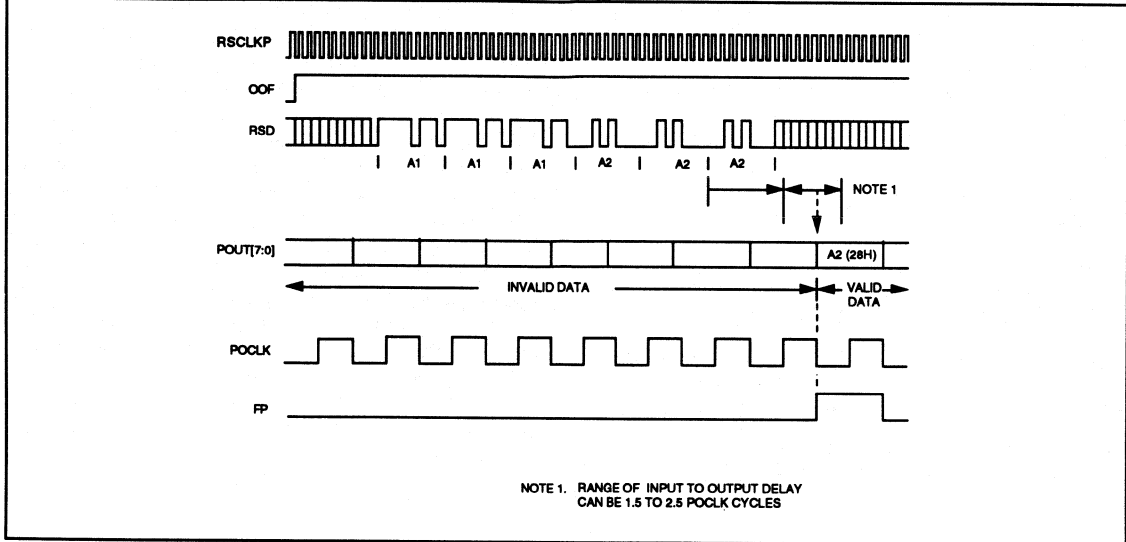
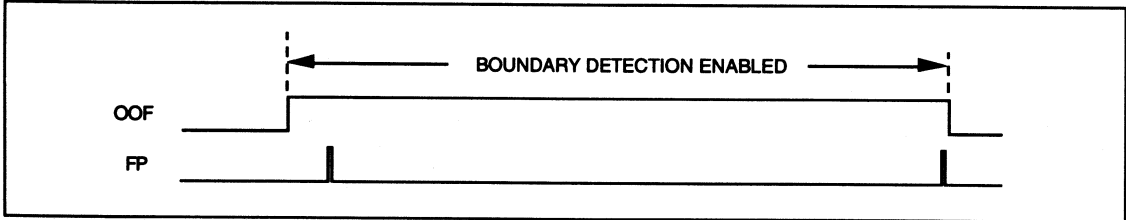


Figure 5. OOF Operation Timing



7

Figure 6. Alternate OOF Timing

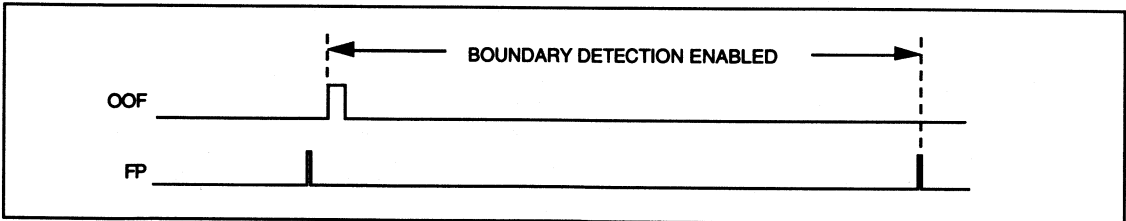


Figure 7. Pin[7:0] Input Timing

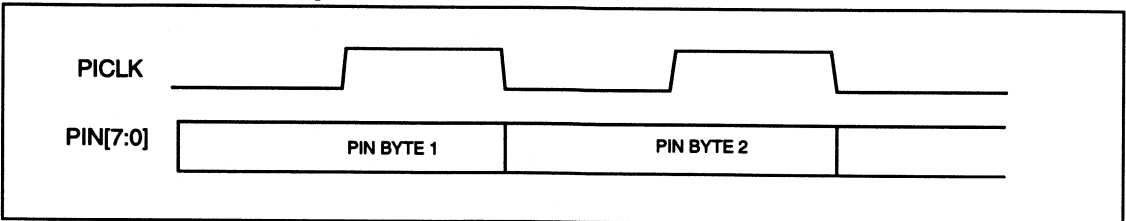


Figure 8b shows the output timing of the line/diagnostic loopback data (LLD/DLD) in relation to the line/diagnostic loopback clock (LLCLK/DLCLK). LLD is updated on the falling edge of LLCLKP and DLD is updated on the falling edge of DLCLKP. DLDP is held at a logic low and DLCLKP is held at a logic high when diagnostic loopback is disabled (TDLEB high). LLDP is held at a logic low and LLCLKP is held at a logic high when line loopback is disabled (RLLEB high).

Figure 9a shows the output timing of the transmit serial data (TSD) in relation to the transmit output clock (TSCLK). TSD is updated on the falling edge of TSCLKP.

Figure 9b shows the input timing of the receive serial data (RSD) in relation to the receive output clock (RSCLK). RSD is sampled on the rising edge of RSCLKP.

As shown in Figure 10 the phase alignment error (PAE) signal is updated on the falling edge of the parallel clock (PCLK).

The parallel input data (PIN[7:0]) is sampled into a holding register on the rising edge of the parallel input clock (PICKL). The data is periodically transferred from the holding register to a parallel-in, serial-out shift register. The delay from PICKL to the transmit serial data (TSD) output ranges from 1 to 9 TSCLK periods depending on the alignment of PICKL and the transfer point. If PICKL rises within one bit period (lead or lag) of the transfer point, a phase alignment error alarm is raised by setting PAE high for one parallel clock (PCLK) period. In NRZ mode, the bit period and the TSCLK period are identical. In CMI mode, the bit period is twice the TSCLK period. The internal transfer point is realigned if a phase alignment error is detected and the synchronization enable (SYNC) signal is active. Figure 11a shows the effect of the realignment of the transfer point when PICKL leads the transfer point by less than one bit period. Figure 11b shows the effect of the realignment when PICKL lags.

Figure 8a. Loopback Input Timing

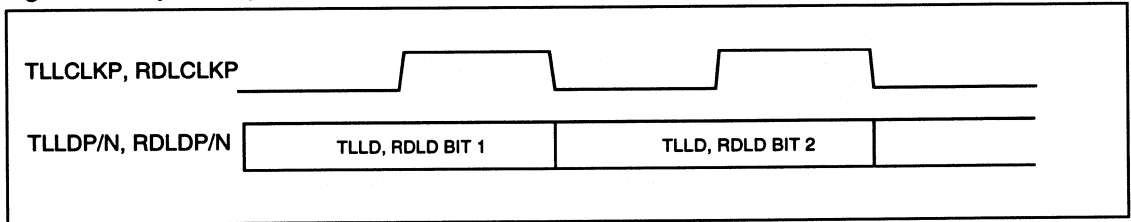


Figure 8b. Loopback Output Timing

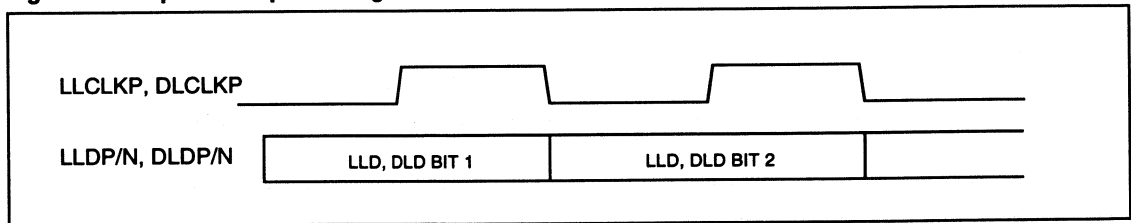


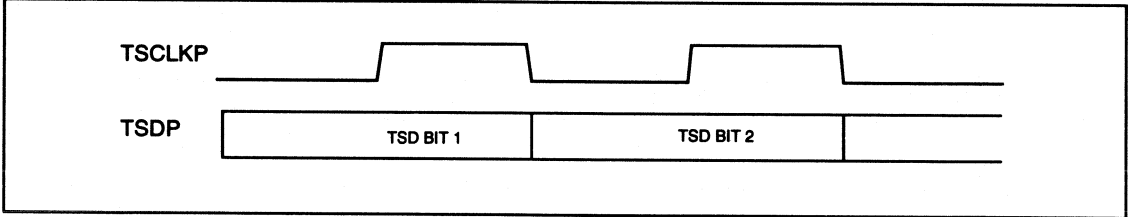
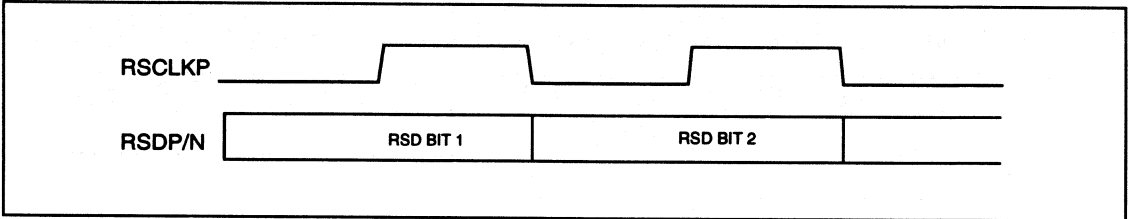
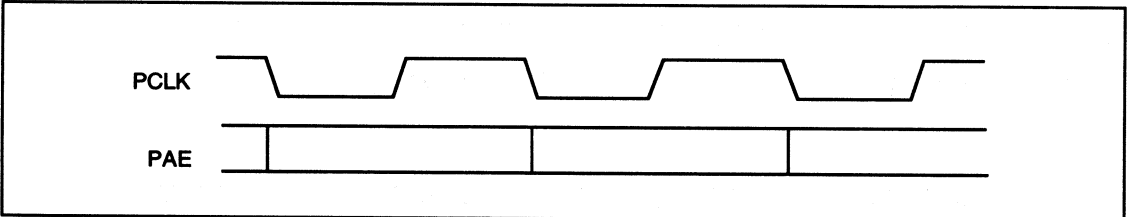
Figure 9a. TSD Output Timing**Figure 9b. RSD Input Timing****Figure 10. PCLK & PAE Output Timing**

Figure 11a. Data Delay and Phase Correction Operation (PICLK leading)

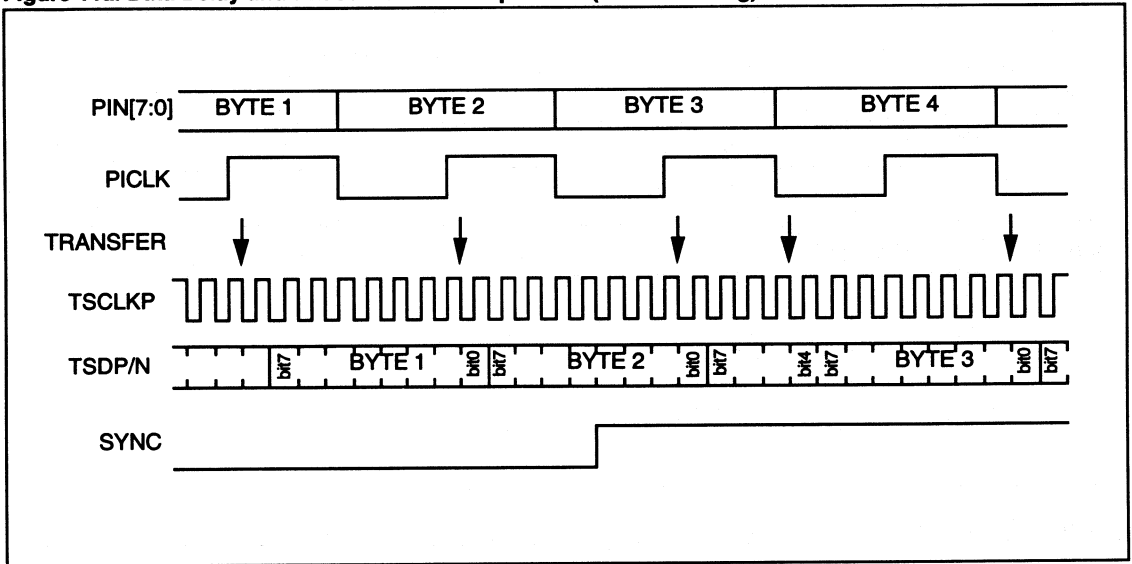
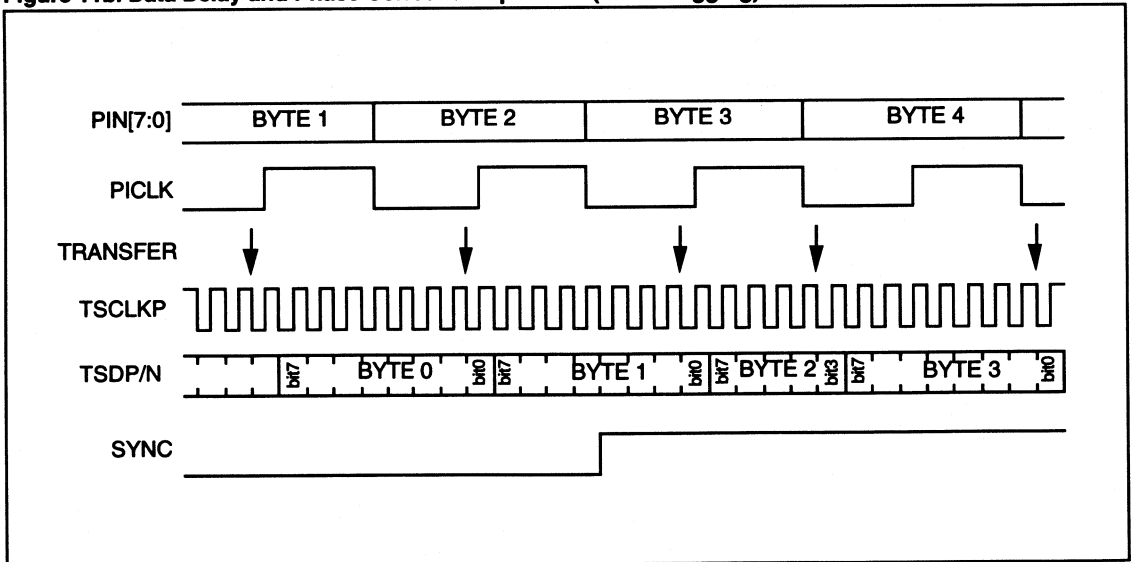


Figure 11b. Data Delay and Phase Correction Operation (PICLK lagging)

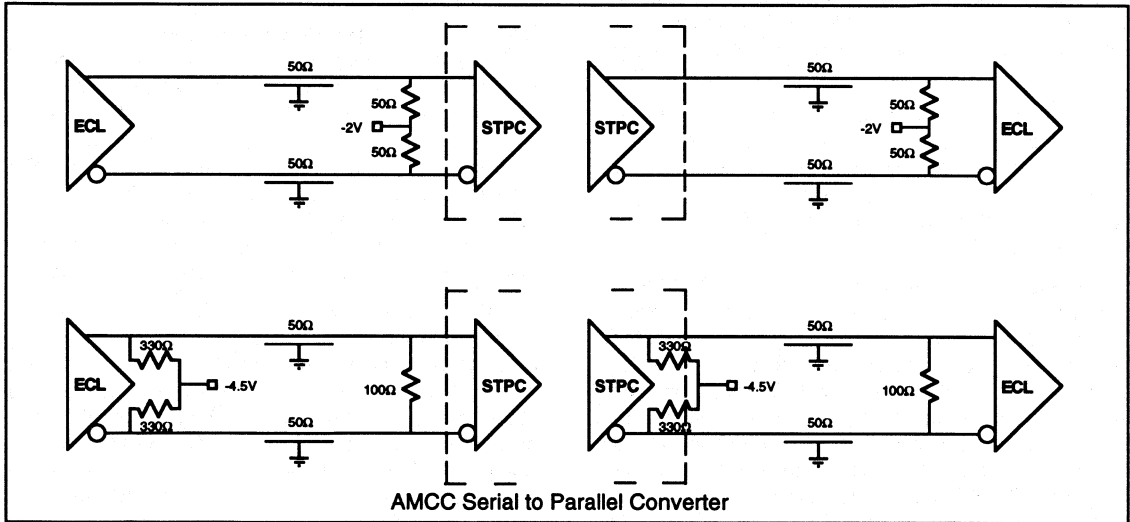


ECL Inputs and Outputs

The ECL compatible differential outputs are standard 100K style emitter follower outputs capable only of sourcing current. They are designed to be terminated with 50 Ω from each output to -2 Volts, assuming that each output drives a 50 Ω transmission line. As with standard 100K ECL logic, the requirement for a -2 Volt supply can be avoided by terminating into a Thevenin equivalent "H" network or by biasing the outputs at the source with pull down resistors connected to a -4.5 Volt supply and terminating the transmission lines at the sink with 50 Ω terminations to AC ground (or equivalently with 100 Ω between the differential signals).

The high speed ECL compatible differential inputs have no built in termination and are assumed to be terminated externally as required by the source that is driving them. To accommodate single-ended ECL input signals it is recommended that one differential input be tied to TVBB or RVBB (VBB outputs, both are equivalent) and the other utilized so as to produce the desired logic function. The VBB outputs are high impedance voltage sources capable of 50μA current drive only and must, therefore, not be used as DC bias in an AC coupled configuration. Figure 12 shows some examples of ECL input and output connections.

Figure 12. ECL Input and Output Applications



PIN DESCRIPTIONS

Receive Serial Data [RSDP/N]—Differential ECL Input. ECL level serial data stream signals, normally connected to an external clock and data recovery device or directly to an optical receiver module having integral clock and data recovery. The RSD inputs are sampled on the rising edge of RSCLKP.

Receive Serial Clock [RSCLKP/N]—Differential ECL Input. ECL level signals used as the receive master clock for the STPC device. RSCLK may be either a 622, 311, or 155 MHz clock, depending on the operating mode of the STPC. POCLK is derived from RSCLK when diagnostic loopback is not enabled. When diagnostic loopback is enabled (RDLEB) and internal loopback is disabled (ILEB), POCLK is derived from the external DLCLK input. When diagnostic loopback is enabled (RDLEB), transmit diagnostic loopback is enabled (TDLEB), and internal loopback is enabled (ILEB), POCLK is derived from the internal DLCLK output. During transitions, the jitter induced on POCLK is typically less than 1/8 UI.

Diagnostic Loopback Data Input [RDLDP/N]—Differential ECL Input. ECL level serial data stream signals, normally connected to a companion device or to the STPC itself for diagnostic loopback purposes. The RDLD inputs are sampled on the rising edge of RDCLKP.

Diagnostic Loopback Clock Input [RDCLKP/N]—Differential ECL Input. ECL-level signals, normally connected to a companion device or to the STPC itself for diagnostic loopback purposes. RDCLK may be either a 622, 311, or 155 MHz clock, depending on the operating mode of the STPC. POCLK is derived from RDCLK when diagnostic loopback is enabled and internal loopback is disabled (ILEB). POCLK is derived from the internal RDCLK when diagnostic loopback is enabled, transmit diagnostic loopback is enabled (TDLEB) and internal loopback is enabled (ILEB). When diagnostic loopback is disabled, POCLK is derived from RSCLK. During transitions, the jitter induced on POCLK is typically less than 1/8 UI.

Receive Bias Voltage Output [RVBB]—Analog Output. Provided to facilitate configuring differential inputs to accept single-ended ECL signals. RVBB is approximately -1.3V and should be connected to each unused differential input in order to set the switching threshold of the other input when it is used for single-ended reception. RVBB should not be loaded in any manner except for connections to STPC ECL inputs and optional 0.1uF capacitor decoupling to ground.

Receive Diagnostic Loopback Enable [RDLEB]—TTL Input. Selects diagnostic loopback. When high, the STPC device uses the receive serial data and clock inputs (RSD and RSCLK). When low, the STPC device uses the diagnostic loopback data and clock inputs. The Internal Loopback (ILEB) pin selects between the external loopback data and clock (RDLD and RDCLK) or the internal loopback data and clock. RDLEB has an integral pull-up resistor.

Out of Frame [OOF]—TTL Input. Used to enable framing pattern detection logic in the STPC. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set low, which ever is longer. OOF may be an asynchronous signal but must have a minimum pulse width of 6 ns. OOF has an integral pull-up resistor.

Loss of Signal [LOSP/N]—Differential ECL Input. Differential ECL inputs that are used by the external optical receiver module to indicate a loss of received optical power. When LOS is high, the data on the received serial data (RSD) pins will be squelched. The effect is equivalent to externally forcing the RSD inputs to an all zeros condition (after CMI decoding if RCMI is enabled). The LOS input is disabled when the Diagnostic Loopback (DLEB) pin is low. When LOS is low, data on the RSD pin will be processed normally.

Receive CMI Enable [RCMI]—TTL Input. Used to enable the CMI decoder. To configure the operating mode of the device as 622 Mbit/s (STS-12 or STM-4) or 155 Mbit/s (STS-3 or STM-1) one must set the RCMI input low and apply 622 MHz or 155 MHz clocks as appropriate. To select 155 Mbit/s CMI operation (STS-3 electrical) one must set the RCMI input high and apply a 311 MHz clock. RCMI has an integral pull-up resistor.

ATM Framing Enable [ATMFENB]—TTL Input. Used to enable the alternate framing approach used for 139 Mbit/s ATM streams. When ATMFENB is high, the STPC frames to three A1 bytes followed by three A2 bytes as required for SONET/SDH. When ATMFENB is low, the STPC frames to a single A1 byte followed by a single A2 byte. ATMFENB has an integral pull-up resistor.

Receive Master Reset [RRSTB]—TTL Input. Pulling RRSTB low will reset the receive side (serial to parallel section) of the device. RRSTB must have a minimum pulse width of 6 ns. After reset, frame boundary detection is disabled until OOF goes high. RRSTB has an integral pull-up resistor.

Line Loopback Data Output [LLDP/N]—Differential ECL Output. ECL level signals that carry a regenerated version of the receive serial data (RSD) input in normal mode. The LLDO pins carry the diagnostic loopback data input (RDLD) when in receive diagnostic loopback mode (RDLEB set low) and the internal loopback mode disabled (ILEB set high). The LLD pins carry the STPC transmit serial data (TSD) outputs when in receive diagnostic loopback mode (RDLEB set low), with the transmit diagnostic loopback enabled (TDLEB set low), and the internal loopback mode enabled (ILEB set low). LLD is updated on the falling edge of LLCLK. The LLD outputs are held in the inactive state, except when RLLEB is low.

Line Loopback Clock Output [LLCLKP/N]—Differential ECL Output. ECL level signals, phase aligned with the line loopback data output (LLD) signals. LLCLK is a buffered version of the receive serial clock (RSCLK) input in normal mode. The LLCLK is the diagnostic loopback clock input (RDLCLK) when in receive diagnostic loopback mode (RDLEB set low) and the internal loopback disabled (ILEB set high). The LLCLK carries the STPC transmit serial data clock (TSCLK) output when in receive diagnostic loopback mode (RDLEB set low), with the transmit diagnostic loopback enabled (TDLEB set low) and the internal loopback enabled (ILEB set low). The LLCLK outputs are held in the inactive state, except when RLLEB is low.

Receive Line Loopback Enable [RLLEB]—TTL Input. Selects line loopback. When high, the STPC device disables the line loopback outputs to save power and reduce noise (LLD and LLCLK forced to logic 0). When low, the STPC device enables the line loopback data and clock outputs (LLD and LLCLK active). RLLEB has an integral pull-up resistor.

Parallel Output Data [POUT<7:0>]—TTL/CMOS Output. A 77.76 Mbyte/s or 19.44 Mbyte/s byte serial stream, aligned to the parallel output clock (POCLK). POUT[7] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT[0] is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). POUT[7:0] is updated on the falling edge of POCLK.

Line Code Violation [LCV]—TTL/CMOS Output. Set high to indicate that one or more bits of the byte currently presented on POUT[7:0] contains a CMI line code violation. LCV is only active in CMI mode. LCV is updated on the falling edge of POCLK.

Frame Pulse [FP]—TTL/CMOS Output. Indicates frame boundaries in the incoming data stream (RSD). If framing pattern detection is enabled, as controlled by the out of frame (OOF) input, FP pulses high for one POCLK cycle when any 48-bit sequence matching the framing pattern is detected on the RSD inputs. When framing pattern detection is disabled, FP pulses high when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK. When ATMFEB is low, the framing pattern detector only looks for a matching 16-bit sequence.

Parallel Output Clock [POCLK]—TTL/CMOS Output. A 77.76 MHz or 19.44 MHz, 50% duty cycle, byte rate output clock that is aligned to the POUT[7:0] byte serial output data. POUT[7:0], LCV and FP are updated on the falling edge of POCLK. When RCMI is low, POCLK is equal to RSCLK (or RDLCLK) divided by eight. When RCMI is high, POCLK is equal to RSCLK (or RDLCLK) divided by sixteen.

Transmit Serial Data [TSDP/N]—Differential ECL Output. ECL level serial data stream signals, normally connected to an optical transmitter module. The TSD outputs are updated on the falling edge of TSCLK+. When line loopback mode is enabled (TLLEB set low) and with internal loopback disabled (ILEB set high), TSD is derived from TLLD. When line loopback mode is enabled (TLLEB set low), with receive line loopback enabled (RLLEB set low), and internal loopback enabled (ILEB set low), TSD is derived from the receive serial data (RSD) input.

Transmit Serial Clock Input [TSCLKIP/N]—Differential ECL Input. ECL level signals, normally used as the master clock for the parallel to serial converter portion of the STPC device. TSCLK may be either a 622, 311, or 155 MHz clock, depending on the operating mode of the STPC. PCLK is derived from TSCLK.

Transmit Serial Clock [TSCLKP/N]—Differential ECL Output. ECL level signals, phase aligned with the transmit serial data (TSD) output signals. TSCLK may be either a 622, 311, or 155 MHz clock, depending on the operating mode of the STPC. TSCLK is derived from TSCLKI in normal mode. When transmit line loopback mode is enabled (TLLEB set low) and with internal loopback disabled (ILEB set high), TSCLK is derived from TLLCLK. When transmit line loopback mode is enabled (TLLEB set low), with receive line loopback enabled (RLLEB set low) and with internal loopback enabled (ILEB set low), TSCLK is derived from receive serial clock (RSCLK) input.

Line Loopback Data Input [TLLDP/N]—Differential ECL Input. ECL level serial data stream signals, normally connected to a companion device or to the STPC itself for line loopback purposes. The TLLD inputs are sampled on the rising edge of TLLCLKP.

Line Loopback Clock Input [TLLCLKP/N]—Differential ECL Input. ECL level signals, normally connected to a companion device or to the STPC itself for line loopback purposes. TLLCLK may be either a 622, 311, or 155 MHz clock, depending on the operating mode of the STPC.

Transmit Bias Voltage Output [TVBB]—Analog Output. Provided to facilitate configuring differential inputs to accept single-ended ECL signals. TVBB is approximately -1.3V and should be connected to each unused, differential input in order to set the switching threshold of the other input when it is used for single-ended reception. TVBB should not be loaded in any manner except for connections to STPC ECL inputs and optional 0.1uF decoupling to ground.

Transmit Line Loopback Enable [TLLEB]—TTL Input. Selects transmit line loopback. When high, the STPC device sources data and clock to the transmit serial data and clock from the parallel to serial converter using its own timing (PIN[7:0], PICKL and TSCLKI). When low and with the internal loopback disabled (ILEB set high), the STPC device sources data and clock to the transmit serial data and clock directly from the line loopback data and clock inputs (TLLD and TLLCLK). When low, with the receive line loopback enabled (RLLEB set low), and with the internal loopback enabled (ILEB set low), the STPC device sources data and clock to the transmit serial data and clock directly from the receive serial data and clock inputs (RSD and RSCLK). TLLEB has an integral pull-up resistor.

Synchronization Enable [SYNC]—TTL Input. The active high (SYNC) input enables the timing generator to invert the internal byte transfer clock if transfers from the PIN[7:0] input holding register are occurring less than one bit period before or after clocking new data into the holding register. The SYNC pin is an asynchronous input which is sampled by and synchronized by TSCLKI. The SYNC pulse should be high for a minimum of two TSCLKI clock cycles. SYNC has an integral pull-up resistor.

Transmit CMI Enable [TCMI]—TTL Input. Used to enable the CMI decoder. To configure the operating mode of the device as 622 Mbit/s (STS-12 or STM-4) or 155 Mbit/s (STS-3 or STM-1) one must set the TCMI input low and apply 622 MHz or 155 MHz clocks as appropriate. To select 155 Mbit/s CMI operation (STS-3 electrical) one must set the TCMI input high and apply a 311 MHz clock. TCMI has an integral pull-up resistor.

Transmit Master Reset [TRSTB]—TTL Input. Pulling TRSTB low will reset the parallel to serial converter portion of the STPC device. TRSTB must have a minimum pulse width of 6 ns. After reset, the internal transfer of the input parallel data to the serial shift register is aligned such that the transfer occurs on the falling edge of PICKL (PICKL samples the data on the rising edge). This guard bands against a phase alignment event. TRSTB has an integral pull-up resistor.

Diagnostic Loopback Data Output [DLDP/N]—Differential ECL Output. ECL level signals are a duplicated copy of the transmit serial data (TSD) output in normal mode and continue to reflect the output of the parallel to serial converter when in transmit line loopback mode (TLLEB set low). DLD is updated on the falling edge of DLCLKP. The DLD outputs are held in the inactive state, except when TDLEB is low.

Diagnostic Loopback Clock Output [DLCLKP/N]—Differential ECL Output. ECL level signals, phase aligned with the diagnostic loopback data output (DLD) signals. DLCLK is a buffered version of the transmit serial clock input (TSCLKI). The DLCLK outputs are held in the inactive state, except when TDLEB is low.

Transmit Diagnostic Loopback Enable [TDLEB]—TTL Input. Selects transmit diagnostic loopback. When high, the STPC device disables the diagnostic loopback outputs to save power and reduce noise (DLD and DLCLK). When low, the STPC device enables the diagnostic loopback data and clock outputs (DLD and DLCLK). TDLEB has an internal pull-up resistor.

Parallel Input Data [PIN <7:0>]—TTL Input. This bus is a 77.76 Mbyte/s or 19.44 Mbyte/s byte serial stream, aligned to the parallel input clock (PICKL). PIN[7] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PIN[0] is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). PIN[7:0] is sampled on the rising edge of PICKL.

Parallel Input Clock [PICKL]—TTL Input. A 77.76 MHz or 19.44 MHz nominally 50% duty cycle input clock, to which PIN[7:0] is aligned. PICKL is used to transfer the data on the PIN inputs into a holding register in the parallel to serial converter. The rising edge of PICKL samples PIN[7:0].

Diagnostic Line Code Violation [DLCV]—TTL Input. A rising edge on the DLCV input causes a CMI code violation in the serial output data. DLCV is an asynchronous input, sampled and synchronized by TSCLKI with a minimum pulse width of four TSCLKI periods. DLCV has an integral pull-up resistor.

Phase Alignment Event [PAE]—TTL/CMOS Output. This signal pulses high during each PCLK cycle for which there is less than one bit period between the internal byte clock and PICKL timing domains. PAE is updated on the falling edge of the PCLK output.

Parallel Clock [PCLK]—TTL/CMOS Output. This output is a reference byte clock generated by dividing TSCLKI by eight in normal mode, or by sixteen when in CMI mode. It is normally used to coordinate byte wide transfers between upstream logic and the STPC device. PAE is updated on the falling edge of PCLK.

Internal Loopback Enable [ILEB]—TTL Input. Selects internal line loopback. When high, the STPC device sources the loopback's clock and data from the external loopback pins (RDLCLK, RDLD). When low, the STPC device uses the internal loopback's clock and data inputs. ILEB has an integral pull-up resistor.

ECL to TTL [ECLIP/N]—Differential ECL Input. Used to convert a differential ECL signal to a single-ended TTL output signal (TTLO).

TTL [TTLO]—TTL Output. The TTL output pin is the converted ECL signal coming from the ECLI differential input pins.

TTL to ECL [TTLI]—TTL Input. The TTL to ECL pin is a TTL input that is used to convert a single-ended TTL signal to a differential ECL output signal (ECLO).

ECL [ECLOP/N]—Differential ECL Output. The ECL output pins are the converted TTL input signal coming from the TTLI input pin.

Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Respect to GND	-0.5		7.0	V
Voltage on VEE with Respect to GND	0.5		-8.0	V
Voltage on any TTL Input Pin	-0.5		5.5	V
Voltage on any ECL Input Pin	0		-3.0	V
TTL/CMOS Output Sink Current			20	mA
TTL/CMOS Output Source Current			10	mA
High Speed ECL Output Source or sink current			50	mA
Static Discharge Voltage		500		V

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Case Temperature under Bias	-40		85	°C
Junction Temperature under Bias	-10		125	°C
Voltage on VCC with Respect to GND	4.75	5.0	5.25	V
Voltage on VEE with Respect to GND ¹	-4.2	-4.5/-4.8	-5.46	V
Voltage on any TTL Input Pin	0		V _{cc}	V
Voltage on any ECL Input Pin	0		-2.0	V
TTL/CMOS Output Sink Current			8	mA
TTL/CMOS Output Source Current			1	mA
ECL Output Source Current			25	mA

1. VEE (min) = -4.2V for Ambient Temperature $\geq 0^{\circ}\text{C}$, -4.5V for Ambient Temperature $< 0^{\circ}\text{C}$.

TTL INPUT/OUTPUT DC CHARACTERISTICS¹
 $(T_A = -40^\circ\text{C to } +85^\circ\text{C}, V_{CC} = 5\text{ V } \pm 5\%, V_{EE} = -4.5\text{ V } \pm 7\% \text{ or } -5.2 \pm 5\%)$

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IL}^2	Input LOW Voltage	Guaranteed Input LOW Voltage for all inputs		0.8	Volts
V_{IH}^2	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all inputs	2.0		Volts
I_{IL}	Input LOW Current	$V_{CC} = \text{MAX}, V_{IN} = 0.5\text{V}$	-400.0		μA
I_{IH}	Input HIGH Current	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$		50.0	μA
I_I	Input HIGH Current at Max VCC	$V_{CC} = \text{MAX}, V_{IN} = 5.25\text{V}$		1.0	mA
I_{OS}	Output Short Circuit Current	$V_{CC} = \text{MAX}, V_{OUT} = 0.5\text{V}$	-100.0	-25.0	mA
I_{OZL}	Output Three-State Current LOW	$V_{CC} = \text{MAX}, V_{OL} = 0.4\text{V}$	-50.0	50.0	μA
I_{OZH}	Output Three-State Current HIGH	$V_{CC} = \text{MAX}, V_{OH} = 2.4\text{V}$	-50.0	50.0	μA
V_{IK}	Input Clamp Diode Voltage	$V_{CC} = \text{MIN}, I_{IN} = -18\text{mA}$	-1.2		Volts
V_{OL}	TTL Output LOW Voltage	$V_{CC} = \text{MIN}, I_{OL} = 8\text{mA}$		0.5	Volts
V_{OH}	TTL Output HIGH Voltage	$V_{CC} = \text{MIN}, I_{OH} = -20\text{mA}$	2.4		Volts

1. These conditions will be met with an airflow of 400 LFPM.
2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

ECL INPUT/OUTPUT DC CHARACTERISTICS¹
 $(T_A = -40^\circ\text{C to } +85^\circ\text{C}, V_{CC} = 5\text{ V } \pm 5\%, V_{EE} = -4.5\text{ V } \pm 7\% \text{ or } -5.2 \pm 5\%)$

Symbol	Parameter	Conditions	Signal Name	Min	Max	Unit
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for all differential inputs		-2.00	-0.70	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all differential inputs		-1.75	-0.45	Volts
V_{ID}	Input DIFF Voltage	Guaranteed Input DIFF Voltage for all differential inputs		0.25	1.40	Volts
I_{IL}	Input LOW Current	$V_{EE} = \text{MAX}, V_{DIFF} = 0.5\text{V}$		-1.00	20.00	μA
I_{IH}	Input HIGH Current	$V_{EE} = \text{MAX}, V_{DIFF} = 0.5\text{V}$		-1.00	20.00	μA
V_{OL}	Output LOW Voltage	50Ω to -2V termination		-2.00	-1.50	Volts
V_{OH}	Output HIGH Voltage	50Ω to -2V termination		-1.11	-0.62	Volts

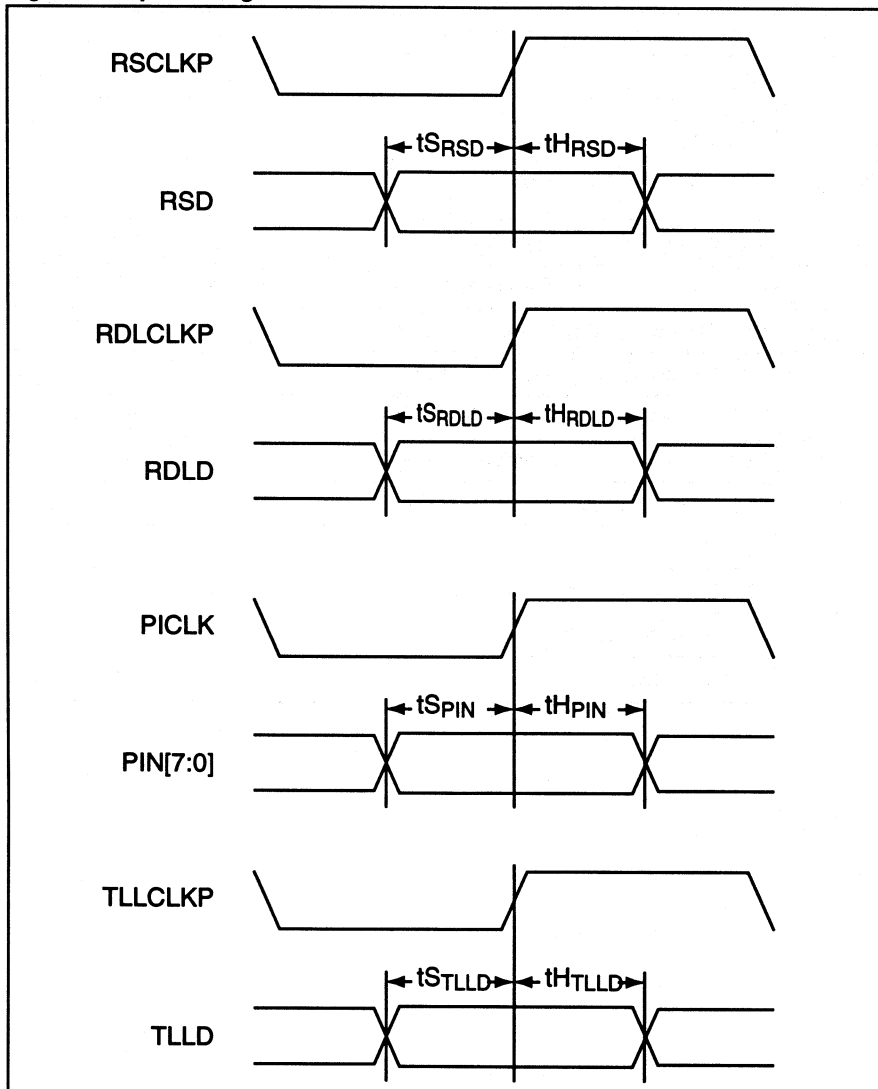
1. These conditions will be met with an airflow of 400 LFPM.

STPC INPUT TIMING

 (T_c = -40°C to T_c +85°C, V_{cc} = 5 V ±5%, V_{EE} = -4.5 V ±7% or -5.2V ± 5%)

Symbol	Parameter	Min	Max	Unit
	RSCLK Freq. (Normally 622, 311, or 155 MHz)		640	MHz
	RSCLK Duty Cycle	33	67	%
t _{S_{RSD}}	RSD to RSCLK Set-up Time	400		ps
t _{H_{RSD}}	RSCLK to RSD Hold Time	200		ps
	RDCLK Freq. (Normally 622, 311, or 155 MHz)		640	MHz
	RDCLK Duty Cycle	33	67	%
t _{S_{RDLD}}	RDLD to RDCLK Set-up Time	400		ps
t _{H_{RDLD}}	RDCLK to RDLD Hold Time	200		ps
t _{WOOF}	OOF High Pulse Width	6		ns
t _{WRSTB}	RRSTB Low Pulse Width	6		ns
	TSCLKI Freq. (Normally 622, 311, or 155 MHz)		640	MHz
	TSCLKI Duty Cycle	33	67	%
	PICLK Freq. (Normally 77.76 or 19.44 MHz, must be divided down version of TSCLKI)	33	67	%
	PICLK Duty Cycle	33	67	%
t _{SPIN}	PIN[7:0] Set-up Time w.r.t. PICLK	1		ns
t _{HPIN}	PIN[7:0] Hold Time w.r.t. PICLK	1		ns
	TLLCLK Freq. (Normally 622, 311, or 155 MHz)		640	MHz
	TTLCLKI Duty Cycle	33	67	%
t _{STLLD}	TLLDI to TLLCLK Set-up Time	400		ps
t _{HTLLD}	TLLCLKI to TLLD Hold Time	200		ps
t _{W_{SYNC}}	SYNC High Pulse Width	2 TSCLKI		periods
t _{W_{DLCV}}	DLCV High Pulse Width	4 TSCLKI		periods
t _{WRSTB}	TRSTB Low Pulse Width	6		ns

Figure 13. Input Timing



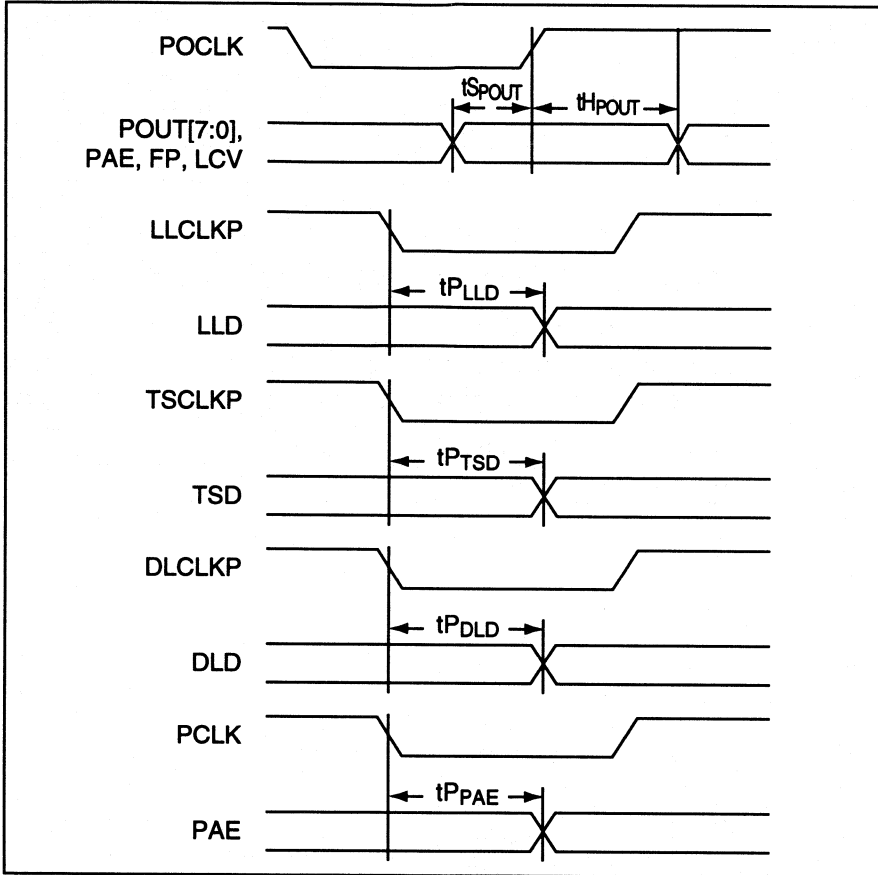
Notes on Input Timing:

1. When a set-up time is specified between an ECL data input and an ECL clock input, the set-up time is the time in picoseconds from the crossover point of the differential data input to the crossover point of the differential clock input.
2. When a hold time is specified between an ECL data input and an ECL clock input, the hold time is the time in picoseconds from the crossover point of the differential clock input to the crossover point of the differential data input.
3. When a set-up time is specified between a TTL data input and a TTL clock input, the set-up time is the time in picoseconds from the 1.4V point of the data input to the 1.4V point of the clock input.
4. When a hold time is specified between a TTL data input and a TTL clock input, the hold time is the time in picoseconds from the 1.4V point of the clock input to the 1.4V point of the data input.

STPC OUTPUT TIMING

Symbol	Parameter	Min	Max	Unit
	POCLK Freq. (Normally 77 or 19 MHz)		80	MHz
	POCLK Duty Cycle	40	60	%
t _{SPOUT}	POUT[7:0], FP, LCV and PAE Set-up Time w.r.t. POCLK	3		ns
t _{HPOUT}	POUT[7:0], FP, LCV and PAE Hold Time w.r.t. POCLK	2		ns
	LLCLK Frequency (Follows RSCLK or DLCLK)		640	MHz
	LLCLK Duty Cycle (up to 5% additive distortion)	28	72	%
t _{PLLD}	LLCLK Low to LLD Valid Propagation Delay	-350	350	ps
	TSCLK Freq. (Normally 622, 311, or 155 MHz)		640	MHz
	TSCLK Duty Cycle (up to 5% additive distortion)	28	72	%
t _{PTSD}	TSCLK Low to TSD Valid Propagation Delay	-350	350	ps
	DLCLK Freq. (Normally 622, 311, or 155 MHz)		640	MHz
	DLCLK Duty Cycle	33	67	%
t _{PDL}	DLCLK Low to DLD Valid Propagation Delay	-350	350	ps
	PCLK Freq. (Normally 77.76 or 19.44 MHz)		80	MHz
	PCLK Duty Cycle	40	60	%

Figure 14. Output Timing



Notes on Output Timing:

1. Output propagation delay time of TTL outputs is the time in picoseconds from the 1.4 V point of the reference signal to the 1.4V point of the output.
2. Maximum output propagation delays of TTL outputs are measured with a 50 pF load on the outputs.
3. Output propagation delay time of ECL outputs is the time in picoseconds from the cross-over point of the reference signal to the cross-over point of the output.
4. Maximum output propagation delays of ECL outputs are measured with a 50Ω load to -2V in parallel with a 10 pF load.
5. When a set-up time is specified between a TTL data input and a TTL clock input, the set-up time is the time in picoseconds from the 1.4V point of the data input to the 1.4V point of the clock input.
6. When a hold time is specified between a TTL data input and a TTL clock input, the hold time is the time in picoseconds from the 1.4V point of the clock input to the 1.4V point of the data input.

Pin Assignment

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	NC	31	NC	61	NC	91	NC
2	NC	32	TTLVCC	62	TTLGND	92	TTLVCC
3	TTLGND	33	ECLIOVCC	63	ECLIOVCC	93	ECLIOVCC
4	ECLIOVCC	34	TTLI	64	ILEB	94	TVBB2
5	ECLIP	35	PAE	65	TLLCLKN	95	POUT6
6	ECLIN	36	PCLK	66	TLLCLKP	96	POUT5
7	RVBB	37	ECLVCC	67	ECLVCC	97	ECLVCC
8	ECLVCC	38	ECLVEE	68	VE	98	ECLVEE
9	VE	39	TRSTB	69	TLLDN	99	POUT4
10	LOSN	40	TCMI	70	TLLDP	100	POUT3
11	LOSP	41	TDLEB	71	RDLDP	101	POUT2
12	RSCLKN	42	TLLEB	72	RDLDN	102	RVBB2
13	RSCLKP	43	DLCV	73	RDLCLKP	103	POUT1
14	RSDN	44	SYNC	74	RDLCLKN	104	POUT0
15	RSDP	45	ECLIOVCC	75	ECLIOVCC	105	POCLK
16	ECLIOVCC	46	PICK	76	DLCLKN	106	ECLIOVCC
17	TSCLKIP	47	PIN7	77	DLCLKP	107	OOF
18	TSCLKIN	48	PIN6	78	DLDN	108	ATMFENB
19	TSDP	49	PIN5	79	DLDP	109	RCMI
20	TSDN	50	PIN4	80	LLDP	110	RRSTB
21	TSCLKP	51	PIN3	81	LLDN	111	RDLEB
22	TSCLKN	52	DNC	82	VE	112	RLLEB
23	VE	53	ECLVEE	83	ECLVCC	113	ECLVEE
24	ECLVCC	54	ECLVCC	84	LLCLKP	114	ECLVCC
25	ECLOP	55	PIN2	85	LLCLKN	115	FP
26	ECLON	56	PIN1	86	POUT7	116	LCV
27	TVBB	57	PIN0	87	ECLIOVCC	117	TTLO
28	ECLIOVCC	58	ECLIOVCC	88	TTLGND	118	ECLIOVCC
29	TTLGND	59	TTLVCC	89	NC	119	TTLVCC
30	NC	60	NC	90	NC	120	NC

Power Supply Connections:

TTLVCC = +5V
 ECLVEE = -5.2V
 VE = -5.2V
 TTLGND = 0V
 ECLVCC = 0V
 ECLIOVCC = 0V
 NC = No Connect
 DNC = Do Not Connect (leave floating)

Figure 15. 120-Pin TEP Package

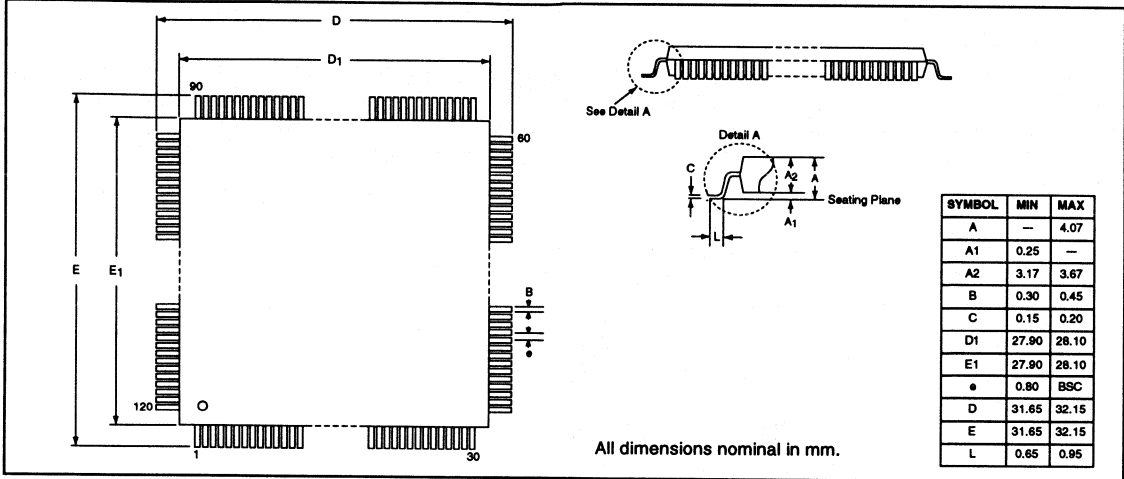
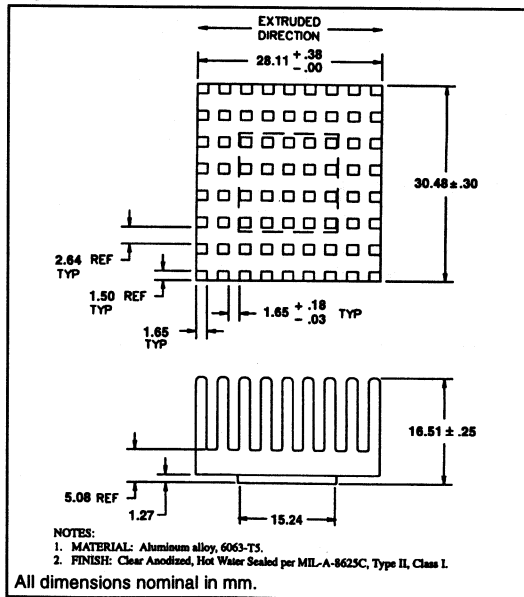


Figure 16. DW0045-17 Heatsink



Thermal Management

Maximum VEE Supply	Power	Øja Still Air w/DW0045-17 Heatsink	Max Still Air ¹ w/DW0045-17 Heatsink	Required Air ² w/DW0045-17 Heatsink
-4.8V	3.78W	11.9°C/W	85°C	N/A
-5.46V	4.53W	11.9°C/W	76°C	100 LFPM

Notes:

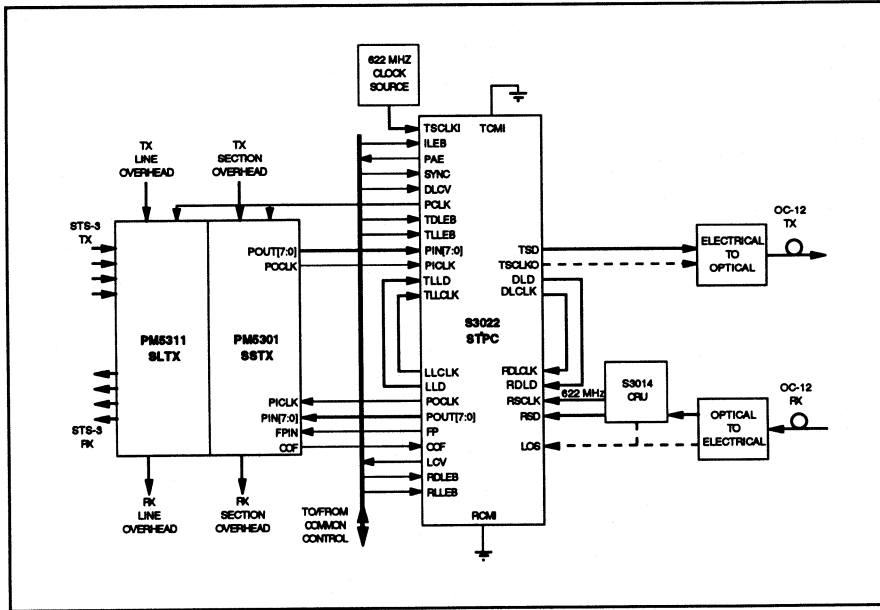
1. Max ambient temperature permitted in still air to maintain $T_j \leq 130^\circ\text{C}$.
2. Airflow required in 85°C ambient conditions to maintain $T_j \leq 130^\circ\text{C}$.

APPLICATION EXAMPLES

622 Mbit/s Interface

The PM5318 STPC device is designed to interface seamlessly with the PM5301 SSTX or PM5312 STTX devices to make a 622 Mbit/s transport interface. Figure 17 shows an STPC connected to an STTX on the equipment side and electrical to optical converters on the line side to realize the core of a typical OC-12 or STM-4 transmission system. Similar connections are used to implement an ATM interface using the PM5355 SUNI-622 device.

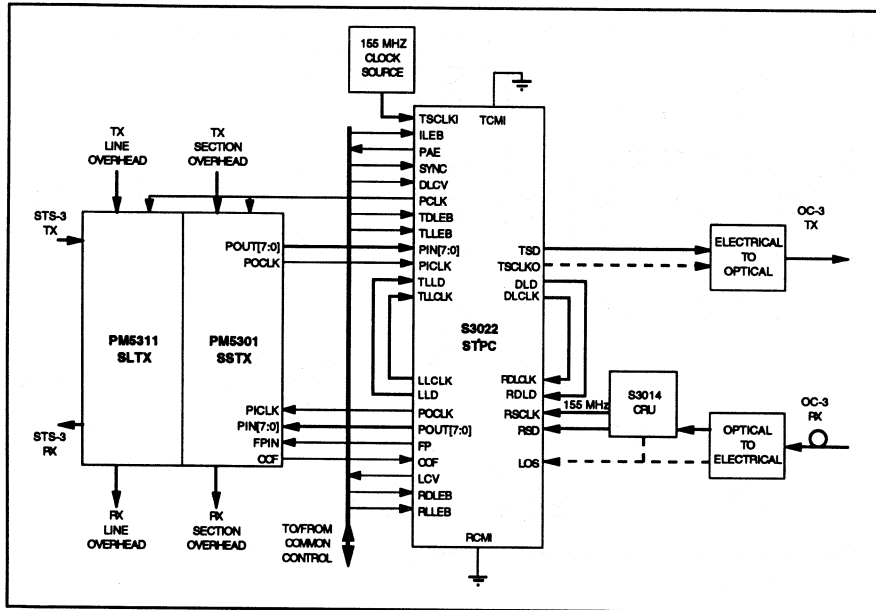
Figure 17. OC-12/STM-4 Application



155 Mbit/s Interface

The PM5318 STPC device is designed to interface seamlessly with the PM5301 SSTX or PM5312 STTX devices to make a 155 Mbit/s transport interface. Figure 18 shows the STPC connected to an STTX on the equipment side and electrical to optical converters on the line side to realize the core of a typical OC-3 or STM-1 transmission system.

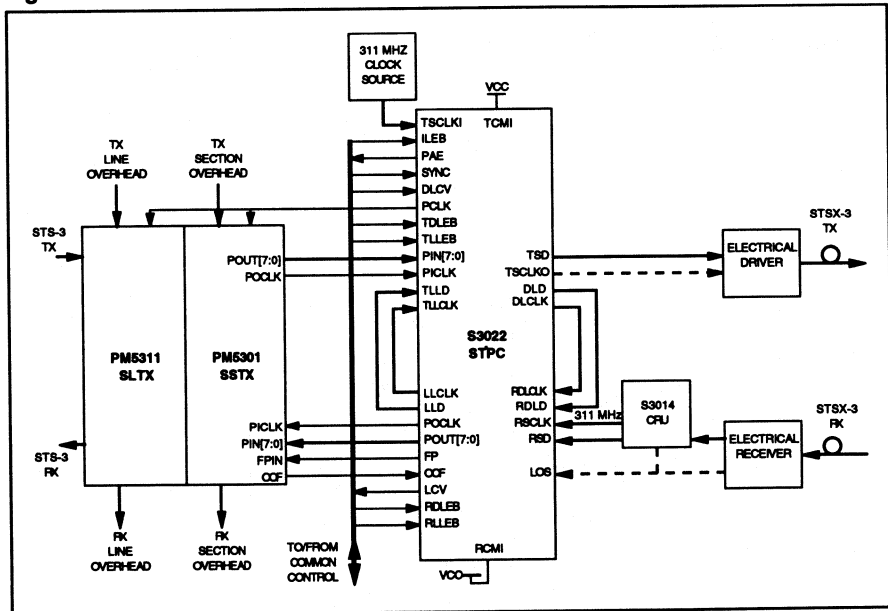
Figure 18. OC-3/STM-3 Application



155 Mbit/s CMI Electrical Interface

With the STPC device optioned for CMI coded STS-3/STM-1, an electrical transmission system using co-axial cable can be implemented as shown in Figure 19. In this case, the interface operates from a 311 MHz clock. TSD would be coupled through a line driver and transformer to a co-axial cable through a transformer and comparators that would slice the incoming signal based on peak detection.

Figure 19. CMI Electrical Interface



Ordering Information

S-Commercial/Industrial	3022	A-120 TEP w/ Heatsink unattached
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X
Grade

X
Part Number

X
Package

FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications for jitter tolerance, jitter transfer and jitter generation
- On-chip high frequency PLL with internal loop filter for clock recovery
- Supports clock recovery for STS-3/STM-1 (155.52 Mbit/s) or STS-12/STM-4 (622.08 Mbit/s) NRZ data
- Selectable 19.44 MHz or 77.76 MHz reference frequency
- Lock detect—monitors transition density, run length and frequency
- 300mW typically
- Low-jitter PECL interface
- On-chip inverting amplifier allows use of low cost reference crystal
- Micro-power Bipolar technology
- 5V supply
- Available in die form or 16 PLCC package

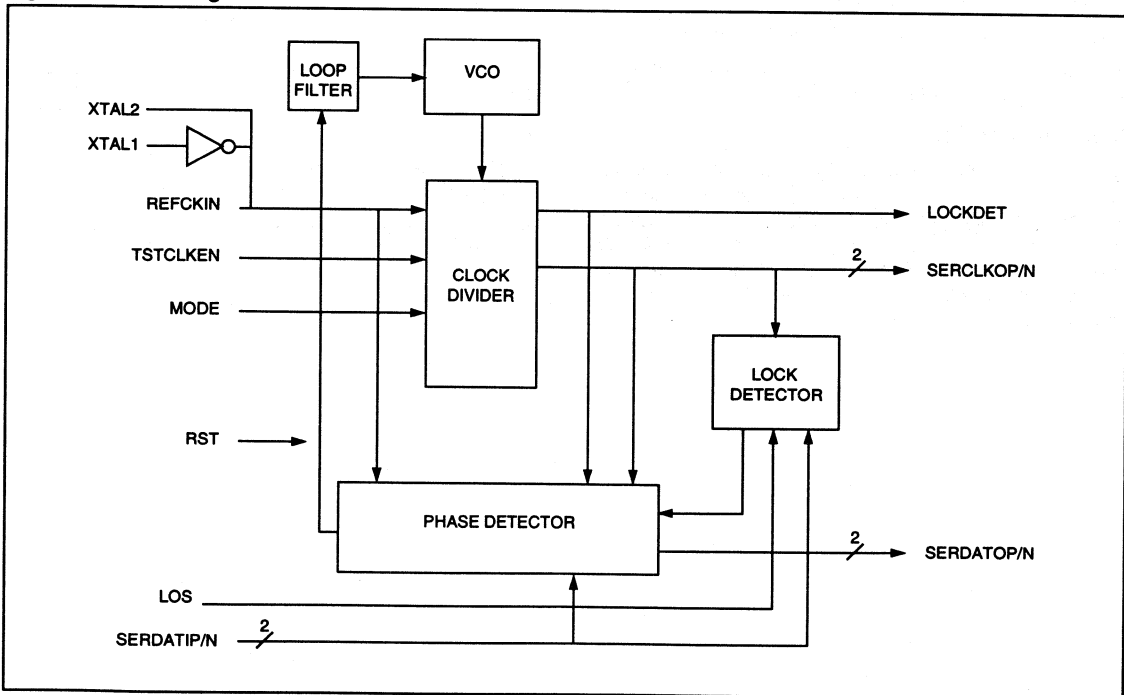
GENERAL DESCRIPTION

The function of the S3025 clock recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S3025 is implemented using AMCC's proven Phase Locked Loop (PLL) technology.

The S3025 receives either an STS-3/STM-1 or STS-12/STM-4 scrambled NRZ signal and recovers the clock from the data. The chip outputs a differential PECL bit clock and retimed data.

The S3025 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 1.

Figure 1. Block Diagram



S3025 OVERVIEW

The S3025 supports clock recovery for the STS-3/STM-1 and STS-12/STM-4 data rates. In this mode, PECL differential serial data is input to the chip at the rate specified by the MODE pin, and clock recovery is performed on the incoming data stream. An external TTL reference clock is required to minimize the PLL lock time and provide a stable output clock source in the absence of serial input data. Retimed data and clock are output from the S3025.

CHARACTERISTICS

Performance

The S3025 PLL complies with the minimum jitter tolerance for clock recovery proposed for SONET/SDH equipment defined by the T1X1.6/91-022 document, when used with differential inputs and outputs as shown in Figure 2.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 2. The measurement condition is the input jitter amplitude which causes an equivalent of 1 dB power penalty.

Serial Data Output Set-up and Hold Time

The output set-up and hold times are represented by the waveforms shown in Figure 3.

Input Jitter Transfer

Jitter transfer is the ratio of the jitter output over the jitter input vs. frequency for clock recovery circuits. For SONET interfaces the PLL based clock recovery circuits are classified as Type B. The key requirement to note is the jitter peaking specification. This specification defines how much gain may be applied to the input jitter.

Figure 2. Input Jitter Tolerance Specification

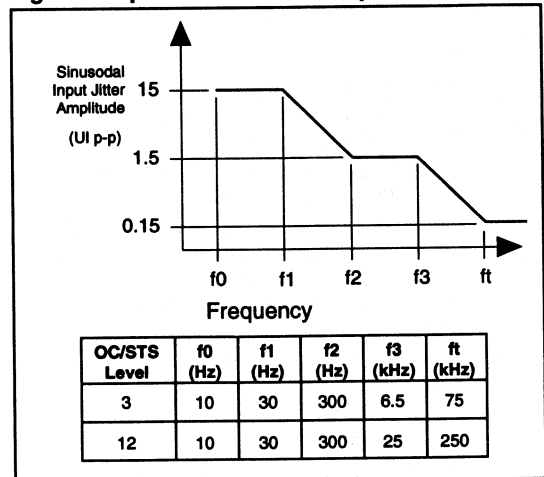
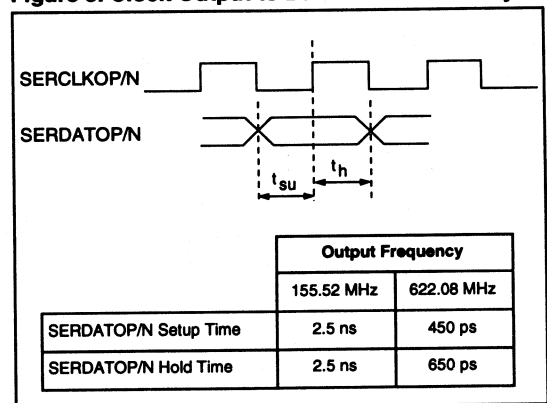


Figure 3. Clock Output to Data Transition Delay



CONTENTS

CROSSPOINT SWITCH PRODUCTS

S2016–16x16 1.5 Gbit/s Differential Crosspoint Switch	8-3
S2024–“Crossbow” 32x32 800 Mbit/s Crosspoint Switch	8-9
S2025–32x32 1.5 Gbit/s Differential Crosspoint Switch	8-17

FEATURES

- 16 x 16 differential crosspoint switch
- Full broadcast switching capability
- Differential 10K PECL data path
- Configurable differential output driver enables
- Up to 1.5 Gbit/s NRZ data rate
- TTL configuration controls
- Reconfigurable without disturbing operation
- 120-pin TEP package
- +5V only power supply

APPLICATIONS

- Digital video
- Digital demultiplexing
- Microwave or fiber-optic data distribution
- High-speed automatic test equipment
- Datacom or telecom switching

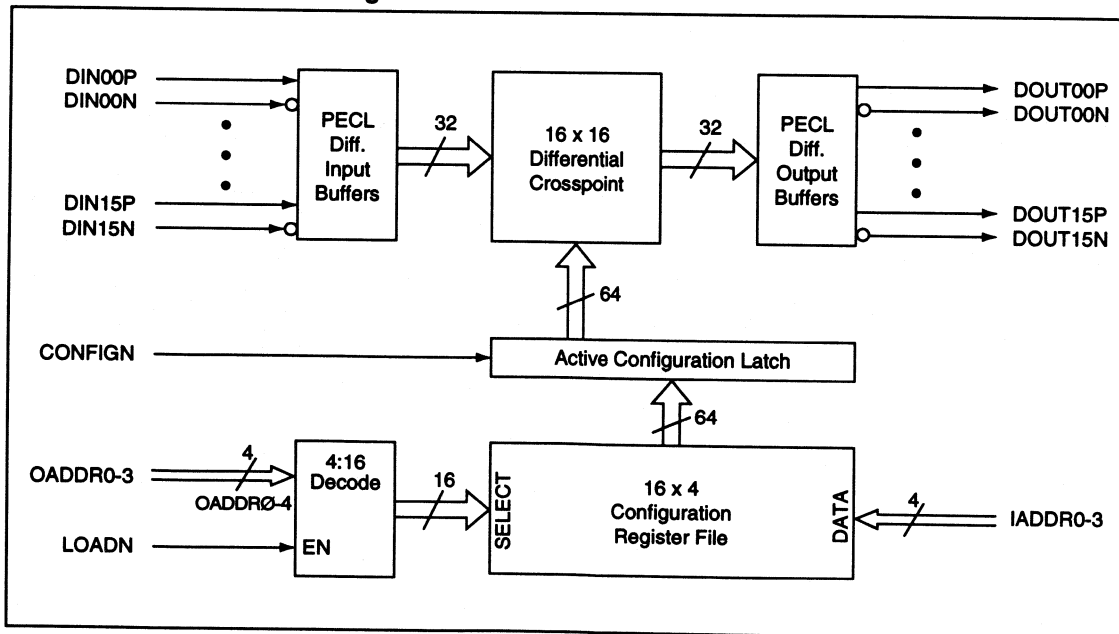
GENERAL DESCRIPTION

The S2016 is a very high-speed 16 x 16 differential crosspoint switch with full broadcast capability. Any of its 16 differential PECL input signal pairs can be connected to any or all of its 16 differential PECL output signal pairs.

The differential 10K PECL logic data path makes the part ideal for high-speed applications. The differential nature of the data path is retained throughout the crosspoint structure, to minimize data distortion and to handle NRZ data rates up to 1.5 gigabits per second.

TTL configuration controls simplify interfacing to slower speed circuitry. Once a new configuration has been entered into the configuration register file, the S2016 can be completely reconfigured by pulsing the CONFIGN input.

Figure 1. Functional Block Diagram



DATA TRANSFER

For each configured connection between a differential input pair and an enabled output pair, any data appearing at the input pair will be passed immediately through to the output pair.

RECONFIGURATION

The S2016 can be selectively reconfigured one output pair at a time, or any number of output pairs can be reconfigured simultaneously. Configuration data is stored in 16 registers, one register for each output pair. As shown in Figure 1, the configuration data is passed in parallel from all 16 registers to a latch which holds the active switch configuration. This two-stage arrangement allows one or more output pairs to be reconfigured simultaneously.

To connect an output pair to a given input pair, the output pair to be reconfigured is selected using the OADDR0-3 (OADDR3=MSB) inputs. With the output pair configuration register selected, the desired input pair selection is provided on the IADDR0-3 (IADDR3=MSB) inputs. The IADDR0-3 information will be stored into the selected output pair configuration register by the LOADN strobe.

When the differential switch is to be reconfigured, the S2016 minimizes the time required through the use of an active configuration latch. While the switch is operational, and prior to the time at which it must be reconfigured, a new configuration can be loaded into the output pair configuration registers. Once the 16 output pair configuration registers contain the desired connection and output pair driver enable information, the contents of the registers are transferred in parallel to the active configuration latch by the CONFIGN strobe. This allows multiple connections to be simultaneously changed.

The configuration latch can be made transparent by driving the CONFIGN input to a logic 0. When this is done, changes strobed into the output pair configuration registers by the LOADN input pair will be passed immediately to the switch.

Figure 2. Data Transfer Waveforms

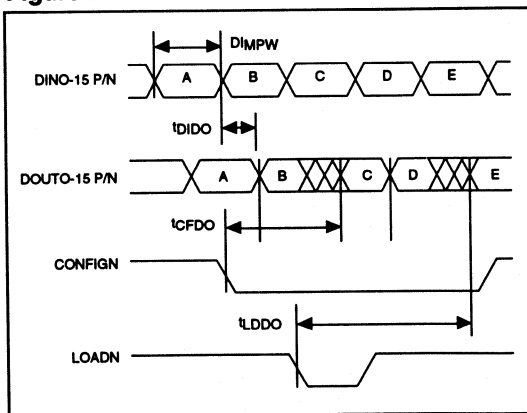


Figure 3. Reconfiguration Waveforms

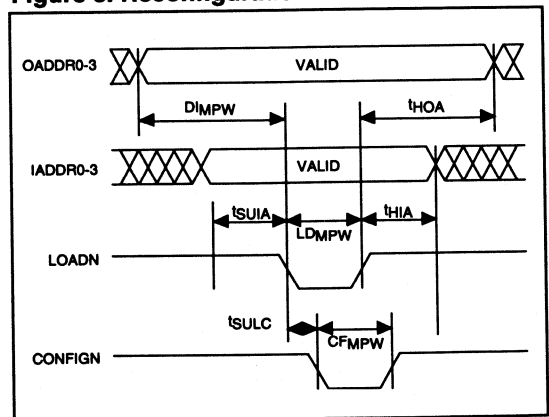


Table 1. Data Transfer Timing¹

Symbol	Description	Min.	Max.	Units
t_{DIDO}	Propagation delay from DIN0–15 P/N to DOUT0–15 P/N		3	ns
t_{CFDO}	Propagation delay from falling edge of CONFIGN to DOUT0–15 P/N valid		6	ns
t_{LDDO}	Propagation delay from falling edge of LOADN to DOUT0–15 P/N valid (When CONFIGN is held low)		7	ns
D_{MPW}	Pulse width of DIN0–15 P/N	0.650		ns
t_{Skew}	Skew between outputs		0.5	ns
F_{MAX}	Data rate	1500		Mbit/s

Table 2. Reconfiguration Timing²

Symbol	Description	Min.	Max.	Units
t_{SUOA}	Setup time of OADDR0-3 before falling edge of LOADN	3500		ps
t_{HOA}	Hold time of OADDR0-3 after rising edge of LOADN	360		ps
t_{SUIA}	Setup time of IADDR0-3 and ENABLE before falling edge of LOADN	1760		ps
t_{HIA}	Hold time of IADDR0-3 and ENABLE after rising edge of LOADN	700		ps
t_{SULC}	Setup time of LOADN to CONFIGN so that the falling edge of CONFIGN will start reconfiguration	660		ps
L_{MPW}	Pulse width low of LOADN	4200		ps
C_{MPW}	Pulse width low of CONFIGN	4200		ps

1. All timing measured from the $V_{CC} - 1.3V$ point on the signals.
2. All timing measured from the 1.5V point on the signals.

Pin Descriptions

Pin Names	Signal	I/O	Description
DIN0P/N - DIN15P/N	Differential PECL	Inputs	Input data. Differential. Can be used as single-ended inputs with VBB tied to one side of each differential input pair.
DOUT0P/N - DOUT15 P/N	Differential PECL	Outputs	Output data. Differential.
OADDR0 - OADDR3	TTL	Inputs	Output pair address. Active high. Used to select an output configuration register in the configuration register file.
IADDR0 - IADDR3	TTL	Inputs	Input pair address. Active high. IADDR0-3 selects the input pair to connect to the output pair selected by OADDR0-3.
LOADN	TTL	Input	Load strobe. Active low. When low, stores the configuration data on IADDR0-3 into the configuration register file.
CONFIGN	TTL	Input	Configuration strobe. Active low. When low, parallel loads the contents of the configuration register file into the active configuration register file into the active configuration latch.

Table 3. Absolute Maximum Ratings

Supply Voltage V_{CC}	7.0V
PECL Input Voltage	$V_{CC} - 2.5V$ to V_{CC}
PECL Output Source Current (continuous)	-50mA DC
TTL Input Voltage	5.5V
Operating Junction Temperature T_j	+150°C
Storage Temperature	-65°C to +150°C

Table 4. Recommended Operating Conditions

Parameter	Min	Nom	Max	Units
Supply Voltage V_{CC}	4.75	5.0	5.25	V
Ambient Temperature	0		70	°C
Junction Temperature			130	°C
I_{CC}		730	1010	mA

Table 5. Differential PECL Input/Output DC Characteristics, $V_{CC} = 4.75V$ to $5.25V^1$

Symbol	Conditions	Min	Typ	Max	Units
V_{OH}				$V_{CC} - 650$	mV
V_{OL}		$V_{CC} - 2100$			mV
V_{OD}^2		250	600	1000	mV
V_{OC}	Output Disabled	$V_{CC} - 2100$	$V_{CC} - 2000$	$V_{CC} - 1990$	mV
V_{IH}				$V_{CC} - 600$	mV
V_{IL}		$V_{CC} - 2000$			mV
V_{ID}^2		250	500	1000	mV
I_{IH}		-0.5		10	μA
I_{IL}		-0.5		10	μA

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Table 6. TTL Input DC Characteristics

Symbol	Parameter	Conditions	Commercial 0° to 70°C			Unit
			Min	Typ ³	Max	
V_{IH}^4	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all input pairs	2.0			V
V_{IL}^4	Input LOW Voltage	Guaranteed Input LOW Voltage for all input pairs			0.8	V
V_{IK}	Input Clamp Diode Voltage	$V_{CC} = \text{MIN}, I_{IN} = -13 \text{ mA}$		-0.8	-1.2	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{MAX}, V_{IN} = 2.7V$			5	μA
I_I	Input HIGH Current at Max.	$V_{CC} = \text{MAX}, V_{IN} = V_{CC} + 0.3V$			1	mA
I_{IL}	Input LOW Current	$V_{CC} = \text{MAX}, V_{IN} = 0.5V$			-0.4	mA

- All outputs are loaded with 50Ω to $V_{CC} - 2V$.
- V_{ID} and V_{OD} represent differential voltage swing specifications.
- Typical limits are at 25°C, $V_{CC} = 5.0V$.
- These input levels provide a zero noise immunity and should only be tested in a static, noise-free environment.

Figure 4. 120-Pin TEP Package

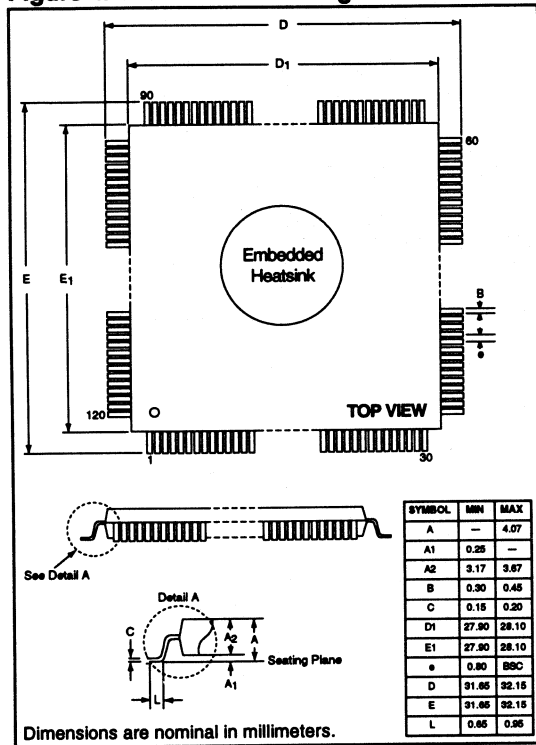
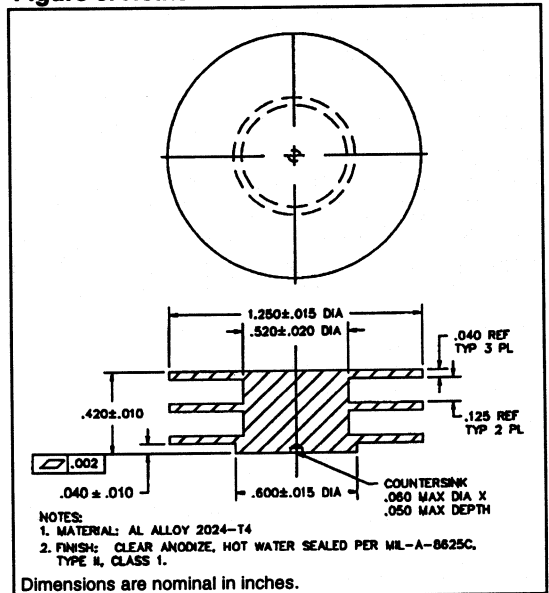


Figure 5. Heatsink



Ordering Information

Grade	16 x 16 Differential Crosspoint Switch	Package
S-Commercial	2016	A – 120 TEP lead formed with Heatsink unattached

X XXXX X
 Grade Part Number Package

FEATURES

- Full broadcast switching capability
- 32 x 32 crosspoint structure, expandable to 64 x 64 with no external components
- ECL 10K data path and TTL I/O for configuration control provide high speed with easy interfacing to slower-speed circuitry
- Up to 800 Mbit/s NRZ data rate in transparent mode, 400-Mbit/s operation in synchronous mode
- 196-pin LDCC package
- Reconfigurable without disturbing operation
- Differential or single-ended clocking

APPLICATIONS

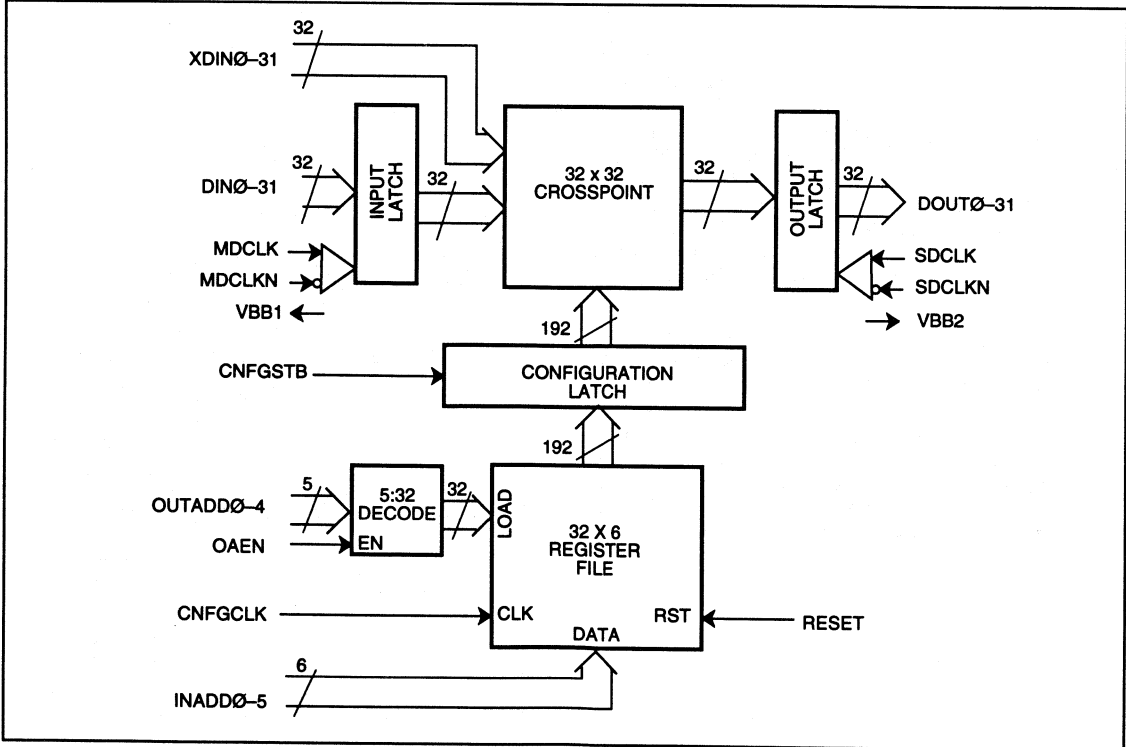
- Digital video
- Digital demultiplexing
- Microwave or fiber-optic data distribution
- High-speed automatic test equipment
- Datacom or telecom switching

DESCRIPTION

The S2024 “Crossbow” is a high-speed 32 x 32 crosspoint switch with full broadcast capability—any of its 32 inputs can be connected independently to any or all of its 32 outputs. In addition, the S2024 can be expanded, through use of its expansion data inputs (XDIN0–XDIN31), to a 64 x 64 crosspoint switch with no external components. Further expansion is possible with external addressing logic.

Two operating modes—synchronous (400 Mbit/s) and transparent (800 Mbit/s)—provide maximum flexibility across a range of applications. The 10K ECL logic data path makes the part ideal for high-speed applications, while the S2024’s TTL addressing and control simplify interfacing to slower-speed circuitry. The switch can be completely reconfigured in only 4 ns without disturbing switch operations.

Figure 1. Functional Block Diagram



OPERATING MODES

SYNCHRONOUS MODE

In synchronous mode, two clock signals, MDCLK for data input and SDCLK for data output, provide the latch enable strobes to allow the input data and output data to be stored in 32-bit latches. The S2024 is capable of 400-Mbit/s operation in this mode. The data is latched on the falling edge of SDCLK and MDCLK.

Inputs MDCLK/MDCLKN and SDCLK/SDCLKN can be used as true differentials or as single-ended clocking signals. Onboard voltage reference outputs VBB1 and VBB2 allow single-ended clocking capability when configured as shown in Figure 6.

TRANSPARENT MODE

In transparent, or asynchronous, mode, any data appearing at the input will be passed immediately through to its designated output. Transparent transfer of data through the latches takes place when both MDCLK and SDCLK clock inputs are held high. In this mode the S2024 is capable of up to a 800 Mbit/s NRZ data rate.

RECONFIGURATION MODE

The S2024 can be selectively reconfigured one output at a time, or any number of outputs can be reconfigured simultaneously. Configuration data is stored in 32 registers, one register for each output data pin. The 6-bit content of each register selects the input data pin which is to be connected to that output data pin. To connect an output to a given input, the output to reconfigure is selected using OUTADD0-4 and OAEN to enable the appropriate output configuration register. With the output configuration register selected, the desired input pin connection is provided on INADD0-5. The input pin selection on INADD0-5 will be stored into the selected output configuration register on the rising edge of CNFGCLK.

When the switch is to be reconfigured, the S2024 minimizes the time required through the use of an additional configuration latch. While the switch is operational (and prior to the time at which it must be reconfigured) a new set of input addresses can be loaded into the register file. When all registers have been updated, the contents of the registers are parallel-transferred to the configuration latch, when CNFGSTB goes high. This process allows a switch reconfiguration in just 4 ns.

Figure 2. Synchronous Mode

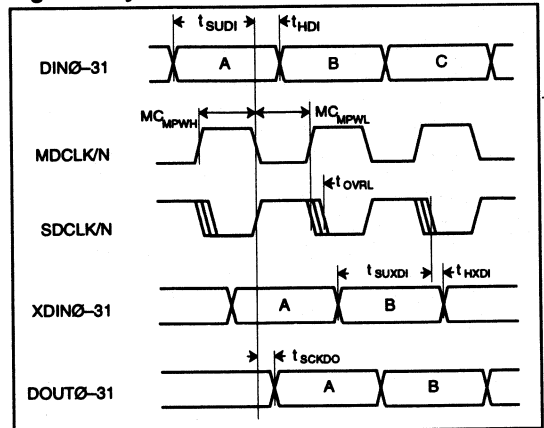


Figure 3. Transparent Mode

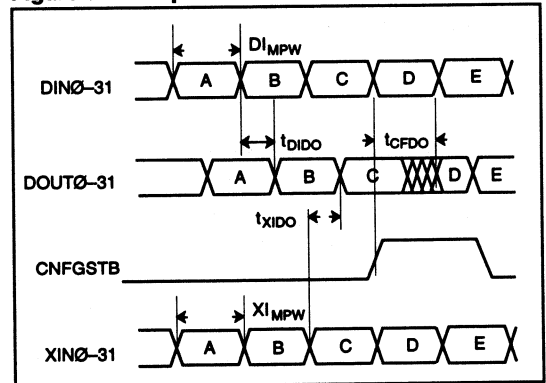
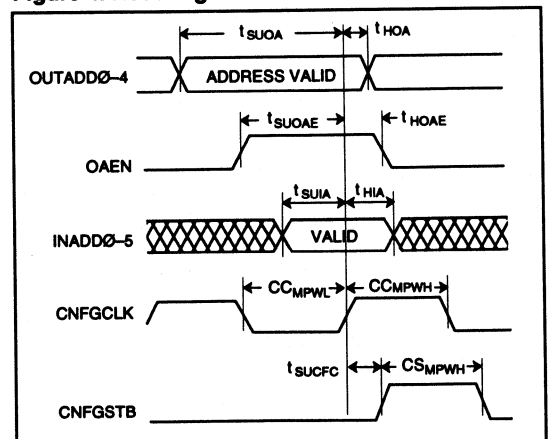


Figure 4. Reconfiguration Mode



SYNCHRONOUS MODE TIMING TABLE

SYMBOL	DESCRIPTION	S2024B-8				S2024B-6				UNITS
		COMMERCIAL		MILITARY		COMMERCIAL		MILITARY		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{SUDI}	Setup time of DIN0-31 before falling edge of MDCLK/N	980		1160		980		1160		ps
t _{HDI}	Hold time of DIN0-31 after falling edge of MDCLK/N	770		1220		770		1220		ps
t _{OVRL}	Overlap when MDCLK/N and SDCLK/N are high		1760		1860		1760		1860	ps
t _{SUXDI}	Setup time of XDIN0-31 before falling edge of SDCLK/N	1040		1160		1040		1160		ps
t _{HXDI}	Hold time of DIN0-31 after falling edge of SDCLK/N	680		1400		680		1400		ps
t _{SKDO}	Propagation delay from rising edge of SDCLK/N to DOUT0-31		2210		3400		2770		4250	ps
M _{COMPWH}	Pulse width high of MDCLK/N or SDCLK/N	630		630		790		790		ps
M _{CPWL}	Pulse width low of MDCLK/N or SDCLK/N	370		370		460		460		ps
Skew	Output Skew		500		500		500		500	ps
F _{MAX}	Data Rate		400		400		300		300	Mbit/s

TRANSPARENT MODE TIMING TABLE

SYMBOL	DESCRIPTION	S2024B-8				S2024B-6				UNITS
		COMMERCIAL		MILITARY		COMMERCIAL		MILITARY		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{DIDO}	Propagation delay from DIN0-31 to DOUT0-31		4100		4180		5125		5230	ps
t _{XIDO}	Propagation delay from XDIN0-31 to DOUT0-31		2720		3040		3400		3800	ps
t _{CFDO}	Propagation delay from rising edge of CNFGSTB to DOUT0-31 valid		3320		3760		4150		4700	ps
D _{MPW}	Pulse width of DIN0-31	820		860		1030		1080		ps
X _{MPW}	Pulse width of XDIN0-31	870		910		1090		1140		ps
Skew	Output Skew		500		500		500		500	ps
F _{MAX}	Data Rate		800		800		600		600	Mbit/s

RECONFIGURATION TIMING TABLE (S2024B-8, S2024B-6)

SYMBOL	DESCRIPTION	COMMERCIAL		MILITARY		UNITS
		Min	Max	Min	Max	
t _{SUOA}	Setup time of OUTADD0-4 before rising edge of CNFGCLK		3500		4360	ps
t _{HOA}	Hold time of OUTADD0-4 after rising edge of CNFGCLK		360		560	ps
t _{SUOAE}	Setup time of OAEN before rising edge of CNFGCLK		2540		3860	ps
t _{HOAE}	Hold time of OAEN before rising edge of CNFGCLK		-240		-140	ps
t _{SUIA}	Setup time of INADD0-5 before rising edge of CNFGCLK		1760		2660	ps
t _{HIA}	Hold time of INADD0-5 before rising edge of CNFGCLK		760		980	ps
t _{SUCFC}	Setup time of CNFGCLK to CNFGSTB so that the rising edge of CNFGSTB will start reconfiguration		660		760	ps
t _{SUCFG}	Setup time of CNFGSTB falling edge before the rising edge of CNFGCLK		1110		1960	ps
CC _{MPWL}	Pulse width low of CNFGCLK		4200		4200	ps
CC _{MPWH}	Pulse width high of CNFGCLK		4200		4200	ps
CS _{MPWH}	Pulse width low of CNFGSTB		4200		4200	ps

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Pin Descriptions

Pin Names	Signal	I/O	Description
DIN0–DIN31	ECL	Inputs	Input data. Active high.
DOU0–DOU31	ECL	Outputs	Output data. Active high.
XDIN0–XDIN31	ECL	Inputs	Expansion input data. Active high. These inputs are selected by the most significant bit of the output configuration registers.
INADD0–INADD5	TTL	Inputs	Input data addresses. Used to select the input data pin connected to each output data pin. Stored into register file by CNFGCLK. INADD5 is used to select the expansion data inputs.
OUTADD0–OUTADD4	TTL	Inputs	Output configuration register address. Used to select the output configuration registers in the register file.
OAEN	TTL	Input	Output address enable. When high, enables the selection of appropriate output configuration register.
MDCLK, MDCLKN	ECL	Inputs	Master latch clock inputs (input data). True differential inputs. Can be used single-ended with VBB1 and VBB2.
SDCLK, SDCLKN	ECL	Inputs	Slave latch clock inputs (output data). True differential inputs. Can be used single-ended with VBB1 and VBB2.
CNFGCLK	TTL	Input	Address configuration clock. On rising edge, stores data into output configuration register.
RESET	TTL	Input	Chip reset. Active high. Asynchronously resets the register file.
CNFGSTB	TTL	Input	Reconfiguration enable input. The contents of the register file are parallel loaded into the configuration latch when CNFGSTB goes high, causing switch reconfiguration.
VBB1, VBB2		Output	Reference threshold voltage outputs to allow provision for single-ended capability for clock inputs.
ACTEST		Output	Used during device testing to determine AC performance of chip. Signal is the output of a 9-stage ring oscillator followed by 2 divide-by-2 circuits. Minimum acceptable output frequency is 32.6 MHz.

EXPANDING THE S2024 TO A 64 X 64 CROSSPOINT SWITCH

Four S2024s can be easily connected to form a 64 x 64 crosspoint switch. In order to accomplish this, the switches must be configured so that any input can be multiplexed to any output. The accompanying figure provides an example of a 64 x 64 switch, making use of the S2024's expansion data inputs.

This arrangement allows all outputs to select input data from any bit of the 64-bit data bus. The two secondary S2024s receive data from the two primaries by means of the expansion data inputs. The expansion inputs are used when the switching operation has been realized by the previous switches and only a flow through is needed.

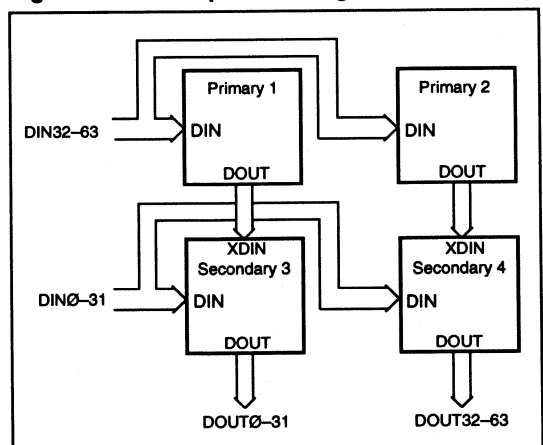
Crosspoint 1 switches D32–D63 to Crosspoint 3.

Crosspoint 2 switches D32–D63 to Crosspoint 4.

Crosspoint 3 switches D0–D31 to O0–O31 and/or reproduces the outputs of Crosspoint 1 through the expansion inputs.

Crosspoint 4 switches D0–D31 to O32–O63 and/or reproduces the outputs of Crosspoint 2 through the expansion inputs.

Figure 5. S2024 Expansion Diagram



ABSOLUTE MAXIMUM RATINGS

ECL Supply Voltage VEE (VCC = 0)	-8.0 VDC
ECL Input Voltage (VCC = 0)	GND to -3V
ECL Output Source Current (continuous)	-50mA DC
TTL Supply Voltage VCC (VEE = 0)	7.0V
TTL Input Voltage (VEE = 0)	5.5V
Operating Temperature	-55°C (ambient) +125°C (case)
Operating Junction Temperature TJ	+150°C
Storage Temperature	-65°C to +150°C

ECL 10K INPUT/OUTPUT DC CHARACTERISTICS V_{EE} = -5.2 V¹

	T _{ambient}				T _{case}	Units
	-55°C	0°C	25°C	75°C	125°C	
V _{OHmax}	-850	-770	-730	-650	-575	mV
V _{IHmax} ³	-800	-720	-680	-600	-525	mV
V _{OHmin}	-1080	-1000	-980	-920	-850	mV
V _{IHmin} ³	-1255	-1145	-1105	-1045	-1000	mV
V _{ILmax} ³	-1510	-1490	-1475	-1450	-1400	mV
V _{OLmax}	-1655	-1625	-1620	-1585	-1545	mV
V _{OLmin}	-1980	-1980	-1980	-1980	-1980	mV
V _{ILmin} ³	-2000	-2000	-2000	-2000	-2000	mV
I _{IH} ² MAX	30	30	30	30	30	μA
I _{IL} ² MAX	-5	-5	-5	-5	-5	μA

RECOMMENDED OPERATING CONDITIONS

Parameter	Commercial			Military			Units
	Min	Nom	Max	Min	Nom	Max	
ECL (10K) Supply Voltage (VEE) VCC = 0	-4.94	-5.2	-5.46	-4.7	-5.2	-5.7	V
ECL Input Signal Rise/Fall Time	—	1.0	3.0	—	1.0	3.0	ns
TTL Supply Voltage VCC	4.75	5.0	5.25	4.5	5.0	5.5	V
Operating Temperature	0 (ambient)	—	70 (ambient)	-55 (ambient)	—	125 (case)	°C
Junction Temperature	—	—	130	—	—	150	°C
I _{CC}	—	—	194	—	—	194	mA
I _{EE}	—	—	1589	—	—	1589	mA
P _{OE}	—	—	0.58	—	—	0.58	W

TTL INPUT/OUTPUT DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST DC CONDITIONS	COMM 0°/+70°C			MIL -55°/+125°C			UNITS
			Min	Typ ²	Max	Min	Typ ²	Max	
V _{IH} ³	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			2.0			V
V _{IL} ³	Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8			0.8	V
V _{IK}	Input clamp diode voltage	V _{CC} = Min, I _{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	V
I _{IH}	Input HIGH current	V _{CC} = Max, V _{IN} = 2.7V			50			50	μA
I _I	Input HIGH current at Max	V _{CC} = Max, V _{IN} = 5.5V			1.0			1.0	mA
I _{IL}	Input LOW current	V _{CC} = Max, V _{IN} = 0.5V			-0.4			-0.4	mA

Notes

1. Data measured with V_{EE} = -5.2 ± .1V assuming a +50°C rise between ambient (T_a) and junction temperature (T_j) for -55°C, 0°C, +25°C, and +70°C, and a +25°C rise for +125°C. These conditions will be met with an airflow of 400 for commercial environment. Cooling of case to +125°C is required for military environment.
2. Typical limits are at 25°C, V_{CC} = 5.0V.
- 3a. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
- 3b. Use extreme care in defining input levels for dynamic testing. Many outputs may be charged at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using V_{IL} ≤ 0.4V and V_{IH} ≥ 2.4V for dynamic TTL testing and V_{ILMIN} and V_{IHMAX} for ECL testing.

196 LDCC

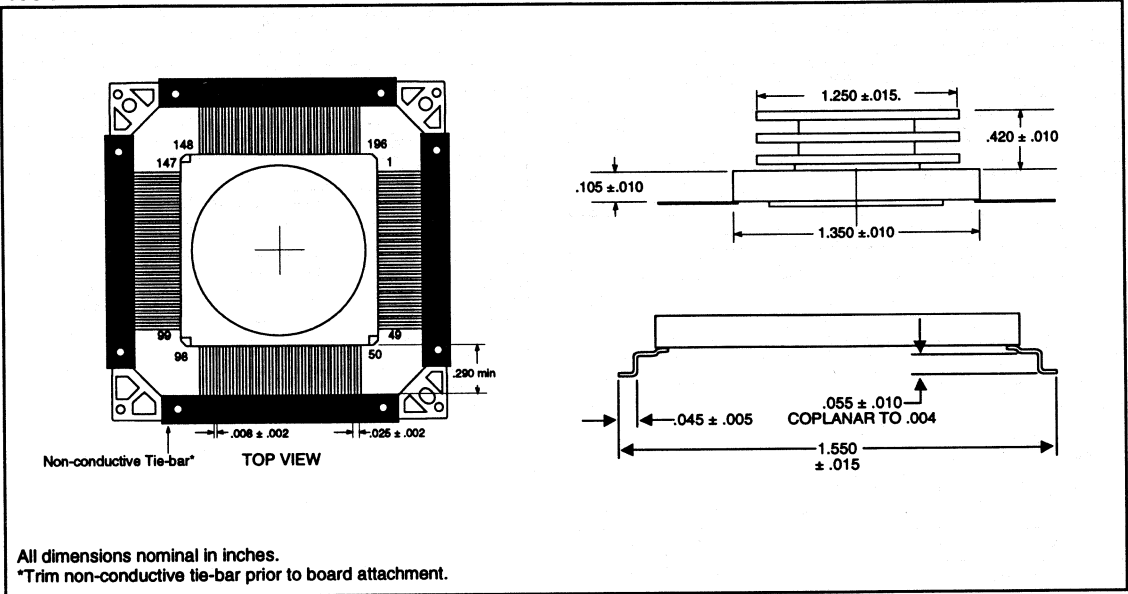
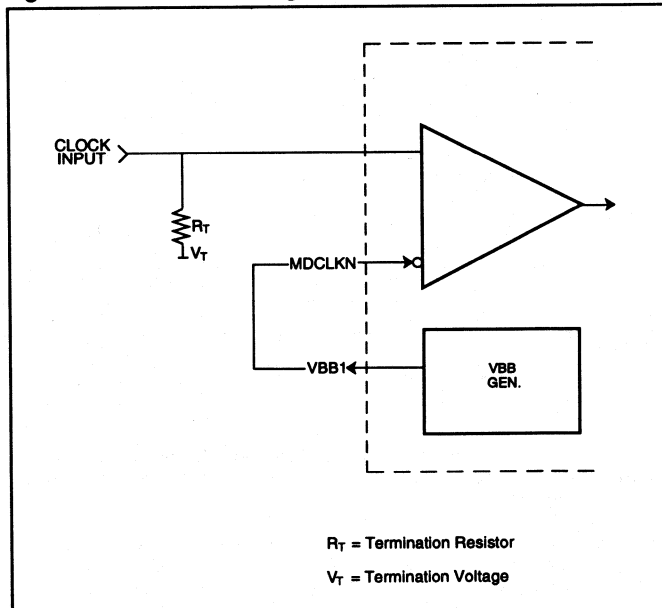


Figure 6. Differential to Single-Ended Conversion



PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	OUTADD0	50	+5V	99	DOUT14	148	+5V
2	OUTADD1	51	GND	100	DOUT15	149	GND
3	OUTADD2	52	XDIN8	101	EGND	150	DIN11
4	GND	53	GND	102	GND	151	GND
5	OUTADD3	54	XDIN7	103	DOUT16	152	DIN12
6	ACTEST	55	XDIN6	104	DOUT17	153	DIN13
7	EGND	56	XDIN5	105	DOUT18	154	DIN14
8	XDIN26	57	XDIN4	106	DOUT19	155	DIN15
9	N/C	58	XDIN3	107	DOUT20	156	DIN16
10	GND	59	XDIN2	108	GND	157	DIN17
11	XDIN25	60	GND	109	EGND	158	GND
12	XDIN24	61	XDIN0	110	DOUT21	159	DIN18
13	OUTADD4	62	XDIN1	111	DOUT22	160	DIN19
14	INADD0	63	-5.2V	112	EGND	161	DIN20
15	INADD1	64	VBB1	113	-5.2V	162	-5.2V
16	GND	65	MDCLKN	114	GND	163	N/C
17	-5.2V	66	MDCLK	115	DOUT23	164	DIN21
18	INADD2	67	GND	116	DOUT24	165	GND
19	INADD3	68	EGND	117	DOUT25	166	DIN22
20	INADD4	69	SDCLKN	118	N/C	167	DIN23
21	INADD5	70	SDCLK	119	DOUT26	168	GND
22	GND	71	GND	120	GND	169	DIN24
23	N/C	72	VBB2	121	DOUT27	170	-5.2V
24	-5.2V	73	-5.2V	122	-5.2V	171	-5.2V
25	-5.2V	74	GND	123	-5.2V	172	GND
26	-5.2V	75	-5.2V	124	-5.2V	173	-5.2V
27	XDIN23	76	-5.2V	125	DOUT28	174	DIN25
28	GND	77	EGND	126	GND	175	DIN26
29	XDIN22	78	DOUT0	127	DOUT29	176	DIN27
30	EGND	79	DOUT1	128	N/C	177	DIN28
31	ACTEST	80	DOUT2	129	DOUT30	178	GND
32	EGND	81	GND	130	DOUT31	179	DIN29
33	XDIN21	82	N/C	131	DIN0	180	DIN30
34	GND	83	DOUT3	132	GND	181	DIN31
35	-5.2V	84	-5.2V	133	-5.2V	182	-5.2V
36	XDIN20	85	DOUT4	134	DIN2	183	XDIN31
37	XDIN19	86	DOUT5	135	DIN1	184	XDIN30
38	XDIN18	87	DOUT6	136	DIN3	185	XDIN29
39	XDIN17	88	GND	137	DIN4	186	GND
40	GND	89	DOUT7	138	GND	187	EGND
41	XDIN16	90	DOUT8	139	DIN5	188	CNFGCLK
42	XDIN15	91	DOUT9	140	DIN6	189	CNFGSTB
43	XDIN14	92	DOUT10	141	DIN7	190	OAEN
44	XDIN13	93	DOUT11	142	DIN8	191	RESET
45	XDIN12	94	DOUT12	143	DIN9	192	XDIN28
46	GND	95	GND	144	GND	193	GND
47	XDIN11	96	DOUT13	145	DIN10	194	XDIN27
48	XDIN10	97	GND	146	THDIODE	195	GND
49	XDIN9	98	+5V	147	THDIODE	196	+5V

Ordering Information

GRADE	32 X 32 CROSSPOINT SWITCH	PACKAGE	SPEED GRADE
S – commercial M – military	2024	B – 196 LDCC with straight leads C – 196 LDCC leadformed with heatsink unattached	6 – 600 Mbit/s 8 – 800 Mbit/s

X XXXX X - XX
Grade Part number Package Speed grade

FEATURES

- 32 x 32 differential crosspoint switch
- Full broadcast switching capability
- Differential 10K PECL data path
- Configurable differential output driver enables
- Up to 1.5 Gbit/s NRZ data rate
- TTL configuration controls
- Reconfigurable without disturbing operation
- 196-pin LDCC package

APPLICATIONS

- Digital video
- Digital demultiplexing
- Microwave or fiber-optic data distribution
- High-speed automatic test equipment
- Datacom or telecom switching

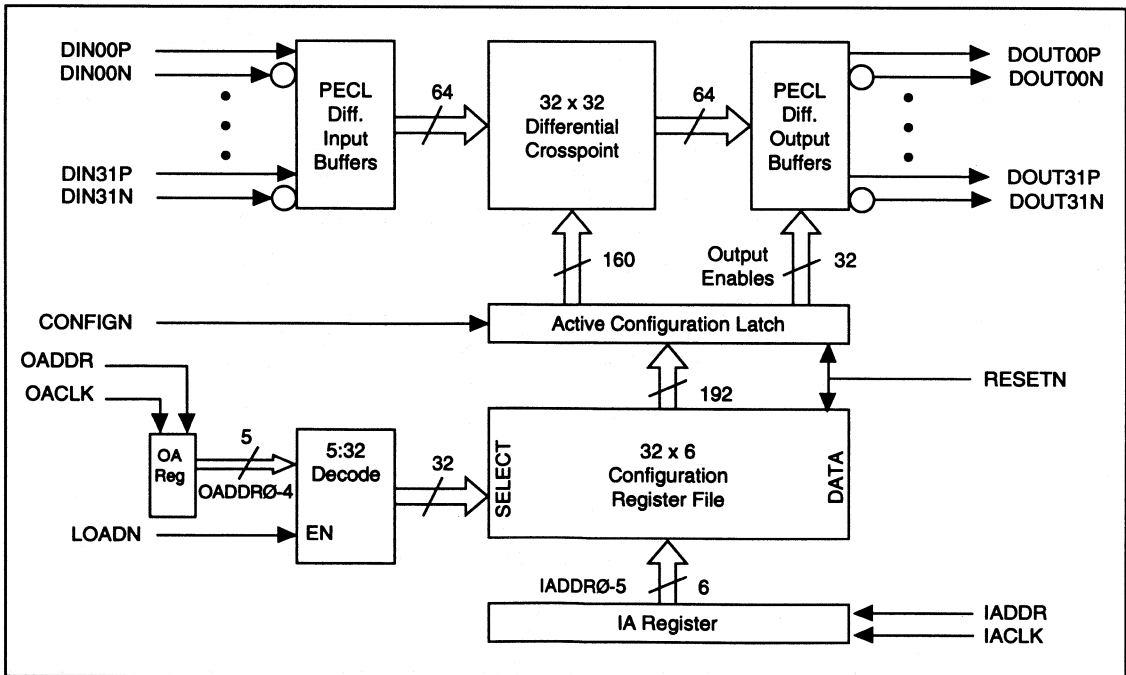
GENERAL DESCRIPTION

The S2025 is a very high-speed 32 x 32 differential crosspoint switch with full broadcast capability. Any of its 32 differential PECL input signal pairs can be connected to any or all of its 32 differential PECL output signal pairs. In addition, the S2025 includes configurable differential output driver enables that allow it to be expanded to larger differential crosspoint switch structures.

The differential 10K PECL logic data path makes the part ideal for high-speed applications. The differential nature of the data path is retained throughout the crosspoint structure, to minimize data distortion and to handle NRZ data rates up to 1.5 gigabits per second.

TTL configuration controls simplify interfacing to slower speed circuitry. Once a new configuration has been entered into the configuration register file, the S2025 can be completely reconfigured in only 6 ns without disturbing switch operations.

Figure 1. Functional Block Diagram



DATA TRANSFER

For each configured connection between a differential input pair and an enabled output pair, any data appearing at the input pair will be passed immediately through to the output pair.

RECONFIGURATION

The S2025 can be selectively reconfigured one output pair at a time, or any number of output pairs can be reconfigured simultaneously. Configuration data is stored in 32 registers, one register for each output pair. As shown in Figure 1, the configuration data is passed in parallel from all 32 registers to a latch which holds the active switch configuration. This two-stage arrangement allows one or more output pairs to be reconfigured simultaneously.

Each output configuration register holds 6 bits. Five bits are used to select which input pair will be connected to the output pair and one bit is used to enable or disable the output pair driver.

To connect an output pair to a given input pair, the output pair to be reconfigured is selected using bits OADDR0-4 of the OA register. These bits are set

using the OADDR and OACLK inputs. The OACLK input, with 100 MHz maximum frequency, can load the OA shift register through the OADDR input, with the OADDR4 (MSB) entering first, followed by the OADDR3, and so on. With the output configuration register selected, the desired input selection is provided on the bits IADDR0-4 of the IA register. Whether or not the output pair is to be enabled is provided on the bit IADDR5 of the same register. The bits IADDR0-5 are set using the IADDR and IACLK inputs. The IACLK input, with 100 MHz maximum frequency, can load the IA shift register through the IADDR input, with the IADDR5 entering first, followed by the IADDR4 (MSB), and so on. The IADDR0-5 information will be stored into the selected output pair configuration register pair by the LOADN strobe.

When the differential switch is to be reconfigured, the S2025 minimizes the time required through the use of an active configuration latch. While the switch is operational, and prior to the time at which it must be reconfigured, a new configuration can be loaded into the output pair configuration registers. Once the 32 output pair configuration registers contain the desired connection and output pair

Figure 2. Data Transfer Waveforms

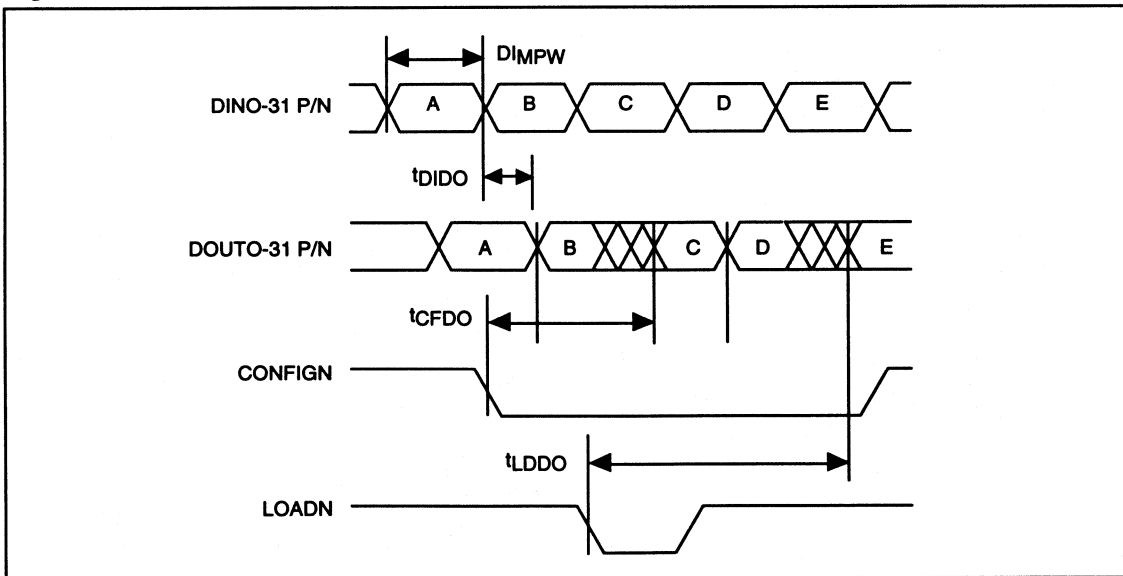
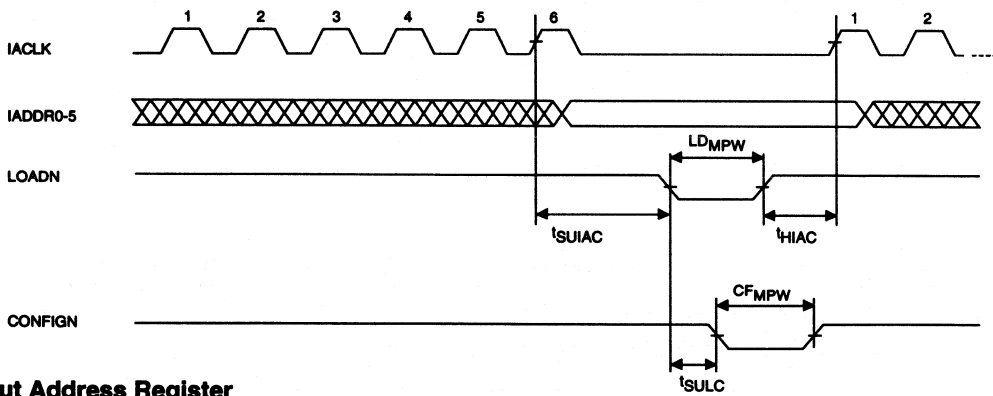
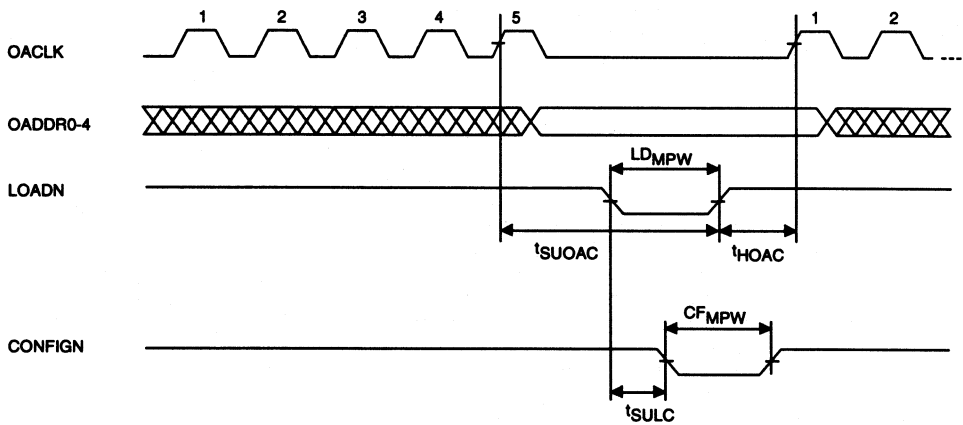


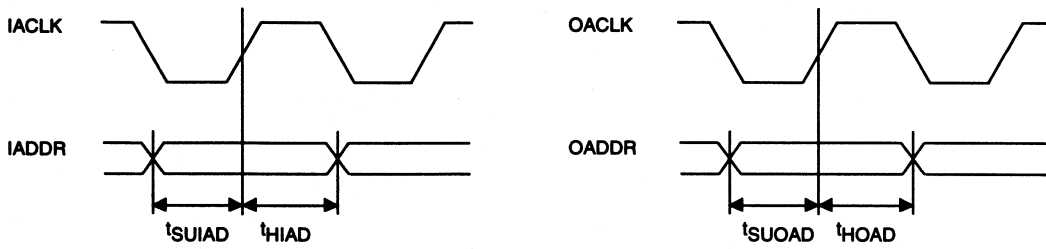
Figure 3. Reconfiguration Waveforms



a. Input Address Register



b. Output Address Register



c. Clock Timing

driver enable information, the contents of the registers are transferred in parallel to the active configuration latch by the CONFIGN strobe. This allows multiple connections to be simultaneously changed.

The configuration latch can be made transparent by tying the CONFIGN input to a logic 0. When this is done, changes strobed into the output pair

configuration registers by the LOADN input pair will be passed immediately to the switch.

Reset Behavior

When the RESETN input pair is asserted, the S2025 assumes a configuration where all the differential output drivers are disabled. Individual output drivers then remain disabled until they are explicitly reconfigured to be enabled.

Table 1. Data Transfer Timing¹

Symbol	Description	Min.	Max.	Units
t_{DIDO}	Propagation delay from DIN0–31 P/N to DOUT0–31 P/N		3	ns
t_{CFDO}	Propagation delay from falling edge of CONFIGN to DOUT0–31 P/N valid		6	ns
t_{LDDO}	Propagation delay from falling edge of LOADN to DOUT0–31 P/N valid (When CONFIGN is held low)		8	ns
$D_{I_{MPW}}$	Pulse width of DIN0–31 P/N	0.650		ns
F_{MAX}	Data rate	1500		Mbit/s

Table 2. Reconfiguration Timing²

Symbol	Description	Min.	Max.	Units
t_{SUIAD}	Setup time of IADDR before rising edge of IACLK	2		ns
t_{HIAD}	Hold time of IADDR after rising edge of IACLK	1		ns
t_{SUIAC}	Setup time of IACLK before falling edge of LOADN	1		ns
t_{HIAC}	Hold time of IACLK after rising edge of LOADN	2		ns
t_{SUOAD}	Setup time of OADDR before rising edge of OACLK	2		ns
t_{HOAD}	Hold time of OADDR after rising edge of OACLK	1		ns
t_{SUOAC}	Setup time of OACLK before falling edge of LOADN	2		ns
t_{HOAC}	Hold time of OACLK after rising edge of LOADN	2		ns
t_{SULC}	Setup time of LOADN to CONFIGN so that the falling edge of CONFIGN will start reconfiguration	1		ns
LD_{MPW}	Pulse width low of LOADN	2		ns
CF_{MPW}	Pulse width low of CONFIGN	2		ns
F_{MAX}	IACLK, OACLK maximum frequency	100		MHz

1. All timing measured from the $V_{CC} - 1.3V$ point on the signals.
2. All timing measured from the 1.5V point on the signals.

Table 3. Pin Descriptions

Pin Names	Signal	I/O	Description
DIN0P/N– DIN31 P/N	Differential PECL	Input Pairs	Input data. Differential inputs can be used as single-ended input pairs with V_{BB} tied to one side of each differential pair.
DOUT0P/N– DOUT31 P/N	Differential PECL	Output Pairs	Output data. Differential.
OADDR	TTL	Input	Serial data input to the Output Address Shift Register.
OACLK	TTL	Input	Output Address Shift Register is loaded on the rising edge of OACLK.
IADDR	TTL	Input	Serial data input to the Input Address Shift Register.
IACLK	TTL	Input	Input Address Shift Register is loaded on the rising edge of IACLK.
LOADN	TTL	Input	Load strobe. Active low. When low, stores the configuration data in IA register into the configuration register file.
CONFIGN	TTL	Input	Configuration strobe. Active low. When low, parallel loads the contents of the configuration register file into the active configuration latch.
RESETN	TTL	Input	Reset. Active low. Resets all the output enable bits in the configuration register file and in the active configuration latch.

EXPANDING TO A 64 X 64 SWITCH

The S2025 includes configurable differential output pair driver enables that allow it to be expanded to form a 64 x 64 differential crosspoint switch.

As shown in Figure 4, four S2025 devices can be used to form a 64 x 64 differential crosspoint switch. Each of the 64 pairs of differential outputs are connected to output pairs on two different S2025 devices.

Similarly, each of the 64 pairs of differential outputs are connected to output pairs on two different S2025 devices. The configuration register files of the two devices are then programmed to enable only one of the two connected output pairs at once.

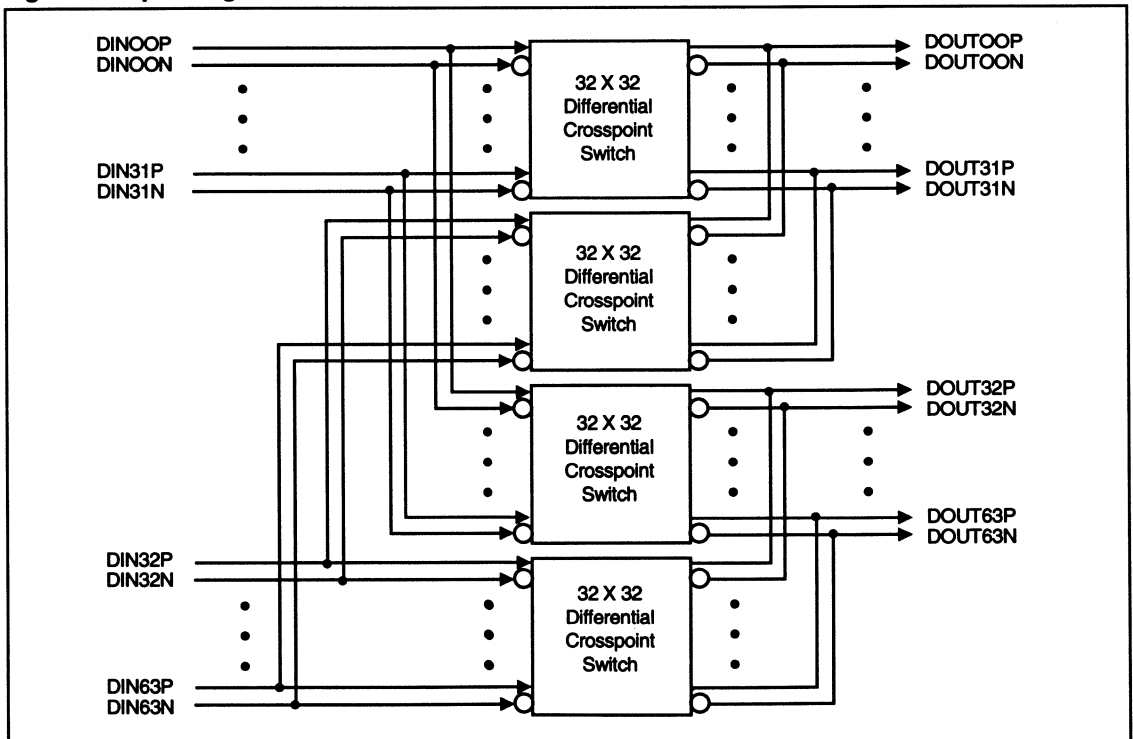
With the interconnection scheme shown in Figure 4, any of the 64 output pairs can be connected to any of the 64 input pairs.

To avoid power-up output pair contention, the Reset condition for the S2025 assumes a configuration where all the differential output pairs are disabled.

Normal high-speed PECL routing and termination practices are required for all PECL connections. For maximum data throughput, reflected signals from impedance mismatches at the package/pcb boundary, as well as those due to poor placement of terminating impedances must be minimized. Care also must be taken during board layout to position the devices for the shortest possible trace lengths when connecting differential outputs together.

Larger differential crosspoint switch structures can also be built using the S2025's ability to selectively enable and disable its differential output pair drivers.

Figure 4. Expanding to a 64 x 64 Switch



THERMAL MANAGEMENT GUIDELINES

Because of the relatively high power dissipation of the S2025 device, thermal management is a key design consideration. The junction temperature (T_j) of the device must not exceed 150°C for it to operate within its specifications. There are a number of ways to implement thermal management, depending upon the system requirements and applications. AMCC is offering the following two methods as guidelines to ensure proper operation of the S2025.

1. Convection—Heat Sink with Forced Air Flow

AMCC offers the standard heat sink 45-17 for impingement cooling (air flow forced directly to the face of the heat sink). This method is similar to the fan/heat-sink devices used on new, high-performance, and high-power microprocessors. The dimensions of the heat sink are given in Figure 6.

Considering the junction-to-case, and case-to-ambient thermal resistivities, one can estimate the amount of required air flow and the maximum ambient temperature (T_a) in order to keep the T_j below the critical limit of 150°C. Table 4 lists these values for 45-17 and 45-24 heat sinks when $T_j = 150^\circ\text{C}$.

Table 4

T_a °C (max) (H/S 45-17)	Air Flow (lfpm)
40	200
60	400
70	600
80	800

2. Conduction—Liquid Cooling Methods

Passive cooling schemes, such as Aavid Engineering's Oasis technology may also be used to ensure low junction temperature. Oasis uses Flourinert, a liquid that boils around 57°C, to transfer heat from the hot device to a condenser, where the vaporized Flourinert is cooled, becomes liquid again, and returns to the hot device. The S2025 case temperature would not exceed 57°C, as long as the cooling system is functioning properly. In such case, using the following equation, one could calculate the maximum anticipated T_j to be around 85°C.

$$T_j = T_c + (Pd \times 2)$$

(T_c is the case temperature in °C, and
 Pd is the dissipated power in Watts.)

For more information on Oasis technology, please contact:

Aavid Engineering Incorporated
 Oasis Products Group
 One Kool Path/P.O. Box 400
 Laconia, NH 03247-0400
 Tel: 603/528-3400
 FAX: 603/528-1478

Table 5. Absolute Maximum Ratings

Supply Voltage V_{CC}	7.0V
PECL Input Voltage	$V_{CC} - 2.5V$ to V_{CC}
PECL Output Source Current (continuous)	-50mA DC
TTL Input Voltage	5.5V
Operating Junction Temperature T_j	+150°C
Storage Temperature	-65°C to +150°C

Table 6. Recommended Operating Conditions

Parameter	Min	Nom	Max	Units
Supply Voltage V_{CC}	4.75	5.0	5.25	V
Ambient Temperature	0		70	°C
Junction Temperature			150	°C
I_{CC}		1950	2600	mA

Table 7. Differential PECL Input/Output DC Characteristics, $V_{CC} = 5.0V$ to $5.25V^1$

Symbol	$T_{Ambient}$			Unit
	0°C	25°C	70°C	
V_{OHmax}^1	$V_{CC} - 815$	$V_{CC} - 775$	$V_{CC} - 695$	mV
V_{IHmax}	$V_{CC} - 720$	$V_{CC} - 680$	$V_{CC} - 600$	mV
V_{OHmin}^1	$V_{CC} - 1045$	$V_{CC} - 1025$	$V_{CC} - 965$	mV
V_{IDmin}	$V_{CC} - 250$	$V_{CC} - 250$	$V_{CC} - 250$	mV
V_{ILmin}	$V_{CC} - 2000$	$V_{CC} - 2000$	$V_{CC} - 2000$	mV
V_{OLmax}^1	$V_{CC} - 1545$	$V_{CC} - 1525$	$V_{CC} - 1465$	mV
V_{OLmin}^1	$V_{CC} - 1900$	$V_{CC} - 1885$	$V_{CC} - 1860$	mV
V_{OC}^1	$V_{CC} - 1800$	$V_{CC} - 1785$	$V_{CC} - 1760$	mV
I_{IHmax}	20	20	20	μA
I_{ILmax}	-5	-5	-5	μA

Table 8. TTL Input DC Characteristics

Symbol	Parameter	Conditions	Commercial 0° to 70°C			Unit
			Min	Typ ³	Max	
V_{IH}^4	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all input pairs	2.0			V
V_{IL}^4	Input LOW Voltage	Guaranteed Input LOW Voltage for all input pairs			0.8	V
V_{IK}	Input Clamp Diode Voltage	$V_{CC} = MIN, I_{IN} = -18 mA$		-0.8	-1.2	V
I_{IH}	Input HIGH Current	$V_{CC} = MAX, V_{IN} = 2.7V$			50	μA
I_I	Input HIGH Current at Max.	$V_{CC} = MAX, V_{IN} = V_{CC} + 0.3V$			1	mA
I_{IL}	Input LOW Current	$V_{CC} = MAX, V_{IN} = 0.5V$			-0.4	mA

1. All outputs are loaded with 50Ω to $V_{CC} - 2V$.
2. V_{ID} and V_{OD} represent differential voltage swing specifications.
3. Typical limits are at 25°C, $V_{CC} = 5.0V$.
4. These input levels provide a zero noise immunity and should only be tested in a static, noise-free environment.

Table 9. S2025 Pinout

SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.
DOUT15P	1	TTLGND	50	DIN31P	99	TTLGND	148
DOUT15N	2	VCC	51	DIN31N	100	VCC	149
DIN00P	3	DOUT17P	52	DIN29P	101	DOUT00N	150
VCC	4	VCC	53	VCC	102	VCC	151
DIN00N	5	DOUT17N	54	DIN29N	103	DOUT01N	152
DIN02P	6	DOUT18P	55	DIN27P	104	DOUT00P	153
DIN02N	7	DOUT18N	56	DIN25P	105	DOUT01P	154
DIN04N	8	DOUT19N	57	DIN23P	106	DOUT02N	155
DIN04P	9	DOUT19P	58	DIN27N	107	DOUT02P	156
VCC	10	DOUT20P	59	VCC	108	DOUT03P	157
DIN06N	11	VCC	60	DIN21P	109	VCC	158
DIN06P	12	DOUT20N	61	DIN25N	110	DOUT03N	159
DIN08P	13	DOUT21N	62	DIN23N	111	OADDR	160
DIN08N	14	ECLGND	63	DIN19N	112	DOUT04N	161
DIN10N	15	DOUT21P	64	ECLGND	113	ECLGND	162
VCC	16	IACLK	65	VCC	114	DOUT04P	163
ECLGND	17	DOUT22P	66	DIN21N	115	DOUT05N	164
DIN10P	18	VCC	67	DIN19P	116	VCC	165
DIN12N	19	DOUT23P	68	DIN17N	117	DOUT05P	166
DIN12P	20	DOUT22N	69	DIN17P	118	DOUT06N	167
DIN14N	21	DOUT24P	70	DIN15N	119	VCC	168
VCC	22	VCC	71	VCC	120	DOUT07P	169
DIN16P	23	DOUT23N	72	DIN15P	121	ECLGND	170
ECLGND	24	ECLGND	73	ECLGND	122	ECLGND	171
ECLGND	25	VCC	74	ECLGND	123	VCC	172
ECLGND	26	ECLGND	75	ECLGND	124	ECLGND	173
DIN14P	27	ECLGND	76	DIN13N	125	DOUT06P	174
VCC	28	DOUT24N	77	VCC	126	DOUT07N	175
DIN18P	29	DOUT25N	78	DIN13P	127	DOUT08P	176
DIN16N	30	DOUT25P	79	DIN11N	128	DOUT08N	177
DIN20P	31	DOUT26N	80	DIN11P	129	VCC	178
DIN18N	32	VCC	81	DIN09N	130	DOUT09P	179
DIN22N	33	DOUT26P	82	DIN07N	131	DOUT09N	180
VCC	34	DOUT27N	83	VCC	132	OACLK	181
ECLGND	35	ECLGND	84	ECLGND	133	ECLGND	182
DIN20N	36	DOUT27P	85	DIN09P	134	DOUT10P	183
DIN24N	37	IADDR	86	LOADN	135	DOUT10N	184
DIN22P	38	DOUT28P	87	RESETN	136	DOUT11P	185
DIN24P	39	VCC	88	DIN07P	137	VCC	186
VCC	40	DOUT29P	89	VCC	138	DOUT11N	187
DIN26N	41	DOUT28N	90	CONFIGN	139	DOUT12P	188
DIN26P	42	DOUT29N	91	DIN05P	140	DOUT12N	189
DIN28P	43	DOUT30P	92	DIN05N	141	DOUT13P	190
DIN28N	44	DOUT30N	93	DIN03N	142	DOUT13N	191
DIN30P	45	DOUT31N	94	DIN03P	143	DOUT14N	192
VCC	46	VCC	95	VCC	144	VCC	193
DOUT16P	47	DOUT31P	96	DIN01N	145	DOUT14P	194
DIN30N	48	VCC	97	DIN01P	146	VCC	195
DOUT16N	49	TTLGND	98	THDIODEP	147	TTLGND	196

Notes: V_{CC} = 5V
TTLGND, ECLGND = 0V

Figure 5. 196-Pin LDCC Package

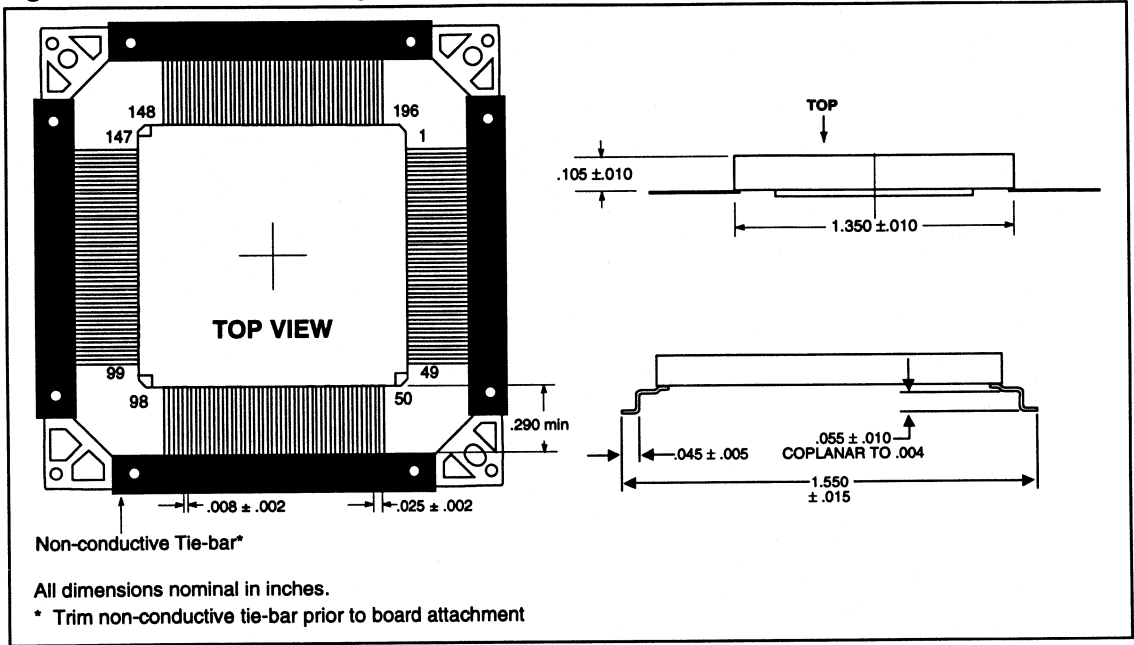
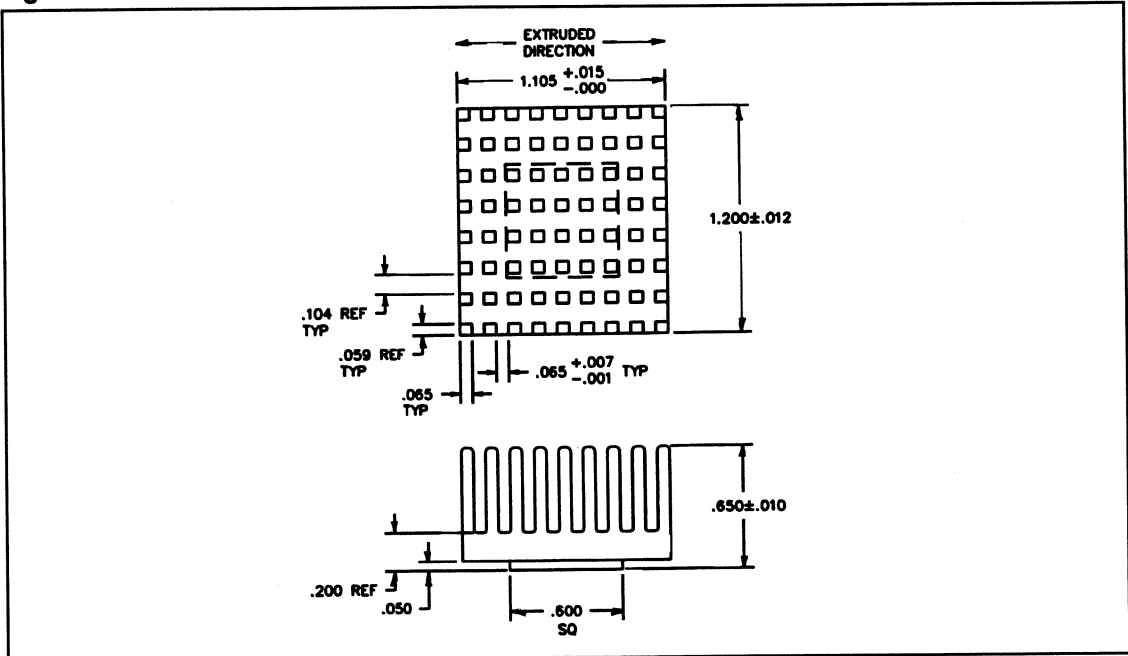


Figure 6. AMCC Heat Sink 45-17



Ordering Information

Grade	32 x 32 Differential Crosspoint Switch	Package
S – Commercial	2025	A – 196 LDCC with straight leads and heatsink attached C – 196 LDCC lead formed with Heatsink unattached

X
Grade

XXXX
Part Number

X
Package

CONTENTS

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E4 FRAMING CIRCUIT DESIGN

The S3005/S3006 parts can be used to implement serializer/deserializer CMI encode/decode and the clock synthesis/recovery functions for the CCITT PDH E4 standard. In E4 (CMI) mode, however, the framing of the 8-bit data bus is not performed in the logic of the S3006. This application note explains how this logic can be designed in the adjacent controller device. The logic functions and frequency of operation will allow the function to be implemented in a FPGA device or a CMOS ASIC.

Framing Pattern

The E4 Frame Detect block decodes the 111110100000 pattern for compliance to the E4 standard.

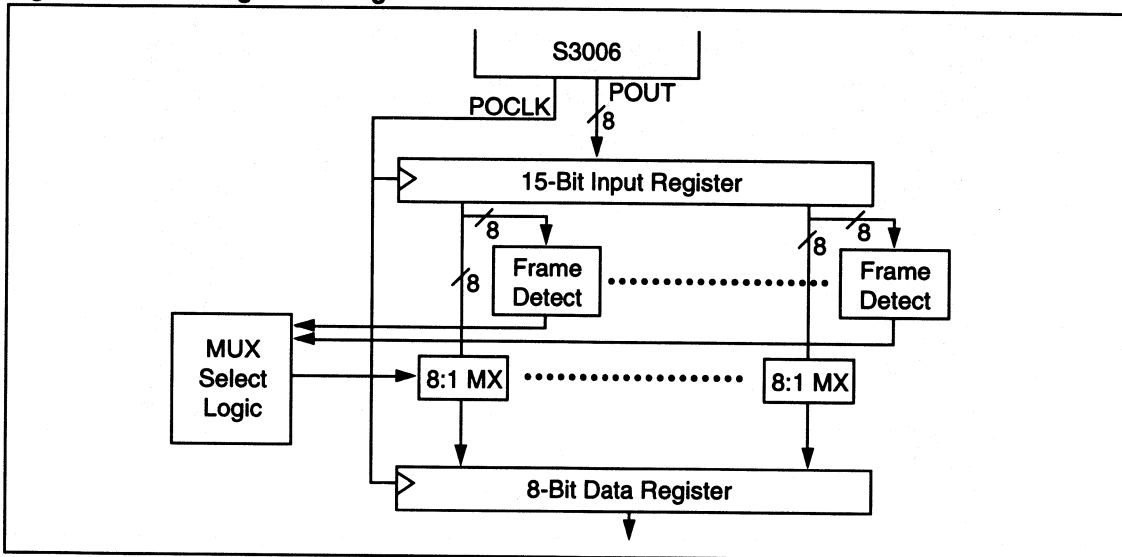
General Design

The S3006 parallel output data is sampled in each of eight possible alignments until the correct framing pattern and sequence is seen. When the correct framing pattern is detected by the E4 frame detect block the 8:1 multiplexer selection is "frozen" and the correctly framed data will be presented in the frame register. This circuit will frame (assuming no bit errors) in a single frame. Additional filter logic can be

added to look for 3 consecutive "correct" framing patterns before declaring frame sync. In addition, the frame detect logic should be monitored to verify that correct framing sequences are being seen after frame sync is achieved. If correct framing sequences are not detected then the frame search logic should be enabled again.

The circuit as shown in Figure 1 consists of an input register, eight 8:1 multiplexers, the multiplexer select logic, and the E4 frame pattern detect logic. The timing of the circuit is done using the S3006 POCLK which is operating at 17 MHz. Data is clocked into the input register from the POUT data lines of the S3006. The data is then routed to the 8:1 multiplexers which select the eight possible byte alignments. The frame register contains the data to be examined for correct frame alignment by the E4 frame detect logic. The frame detect logic detects all of the possible byte alignments of the E4 framing pattern. When the FA pattern is detected, the multiplexer selection is then "frozen" and the additional 0X pattern is checked before declaring frame sync. The detailed circuit design and timing diagrams are shown in Figures 2 and 3.

Figure 1. E4 Framing Block Diagram



BLOCK DESCRIPTIONS

Input Register: 15-bit register which holds all the possible positions of the unframed data. The bit position of the data in this register is dependent on the random alignment of the data outputs of the S3006.

8:1 Multiplexers: These eight multiplexers select the data alignment to be clocked into the data register.

Frame Detect: These are 8 wide decoders which decode the 111110100000 E4 framing pattern. The

inputs are connected to each of the eight possible locations of the framing pattern.

Multiplexer Select Logic: This block takes in the results of all the decoder blocks and outputs the correct 8:1 multiplexer select values.

Data Register: This block contains the correctly framed data after frame alignment has occurred.

Figure 2. Detailed Schematics of E4 Framing Circuit

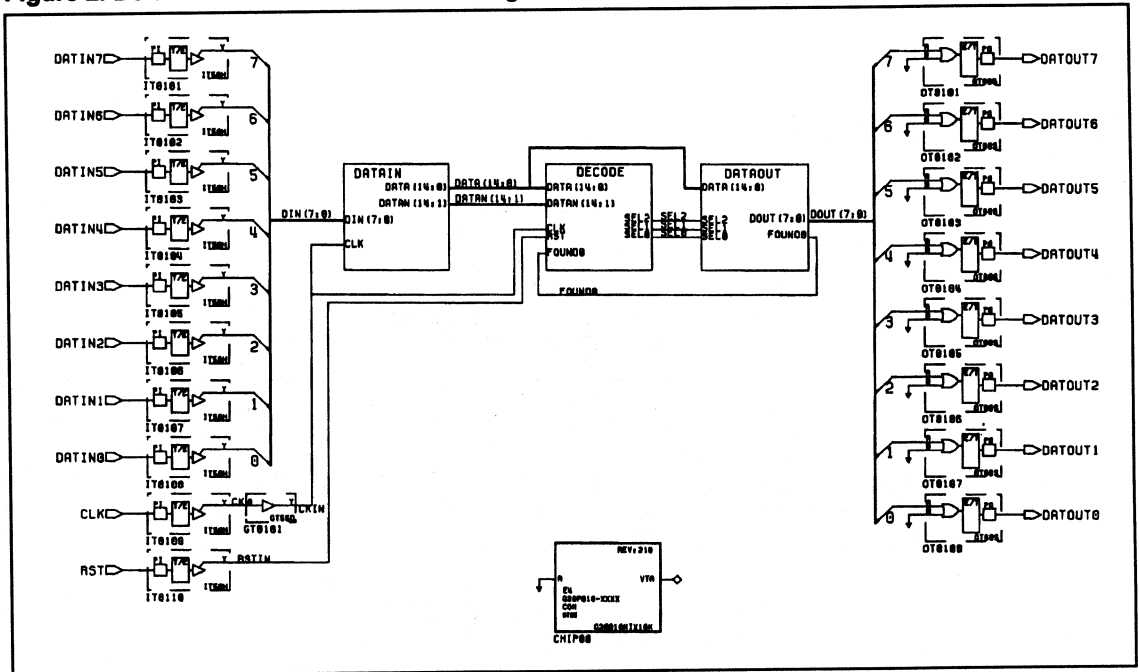


Figure 2. Detailed Schematics of E4 Framing Circuit (Con't.)

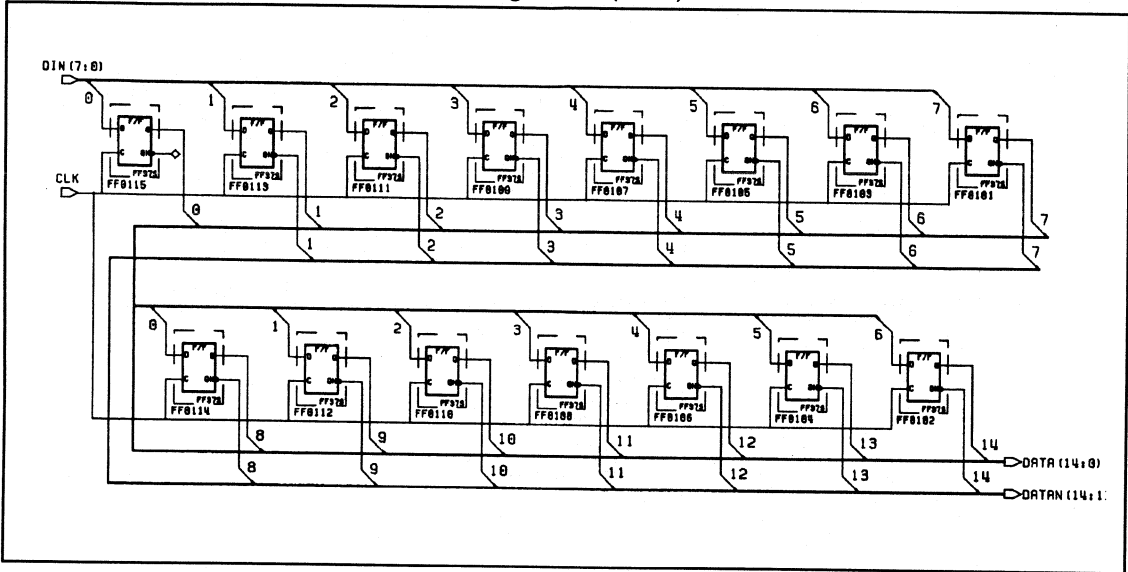


Figure 2. Detailed Schematics of E4 Framing Circuit (Con't.)

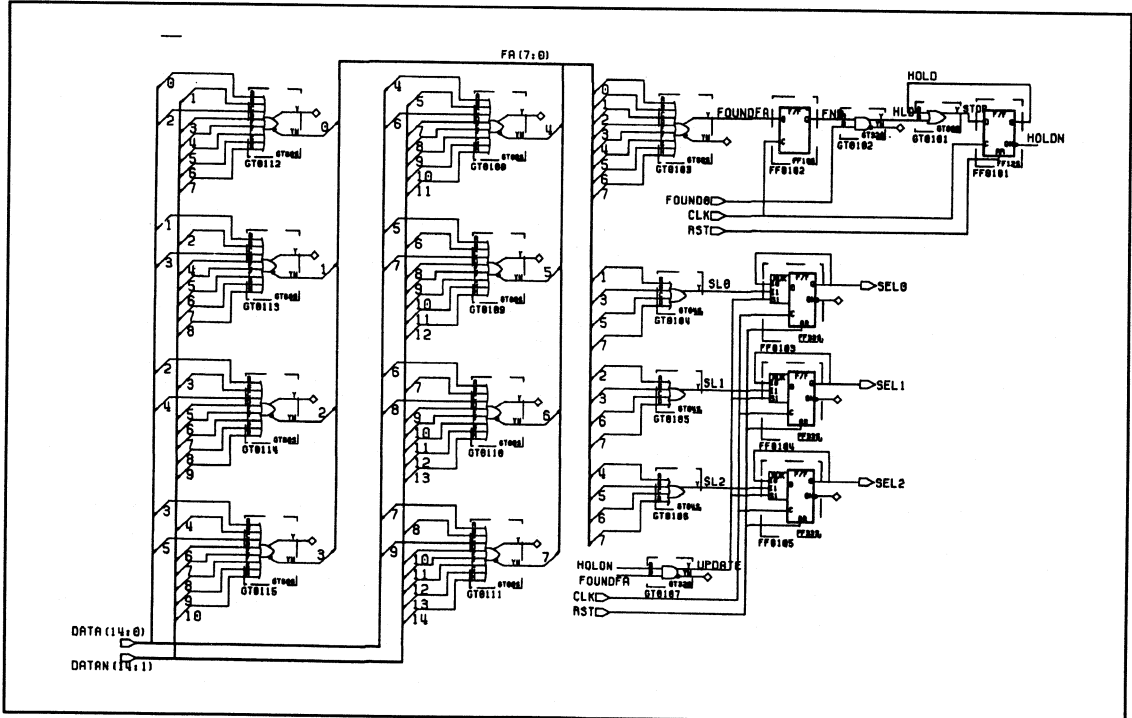


Figure 2. Detailed Schematics of E4 Framing Circuit (Con't.)

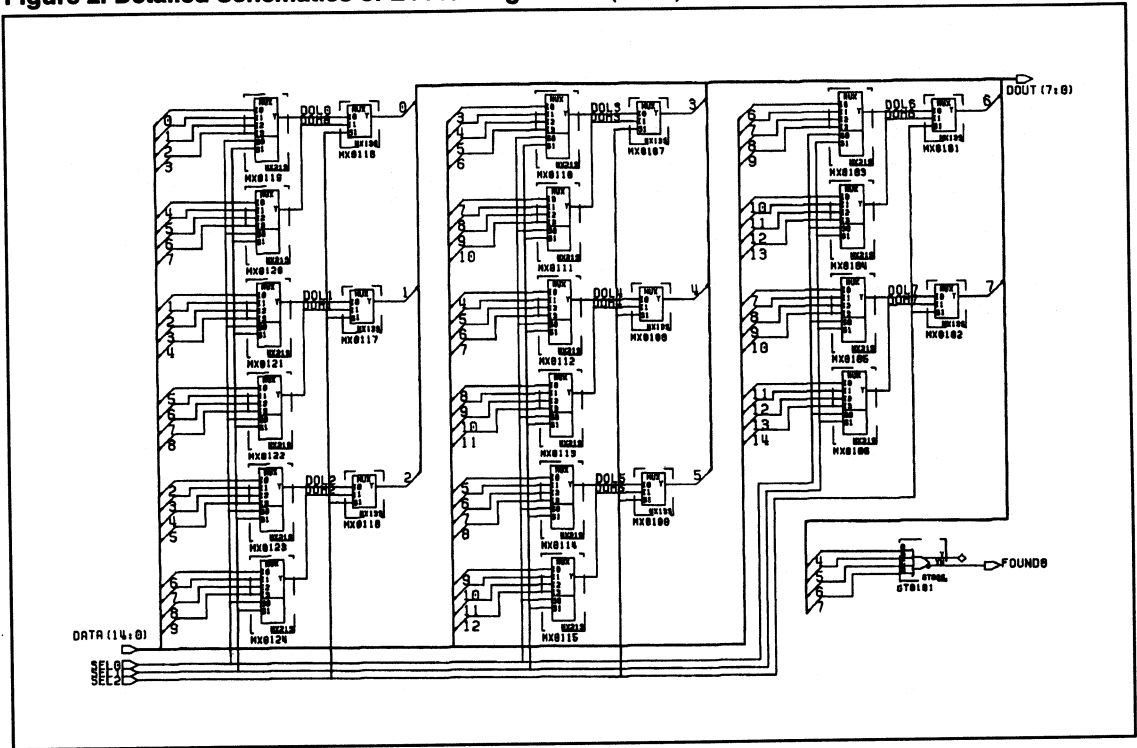
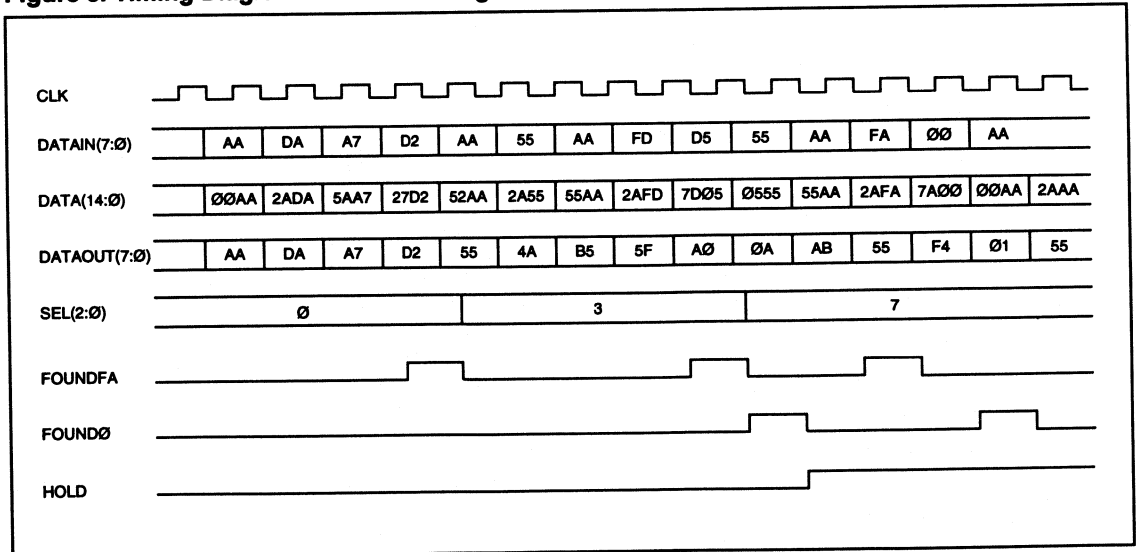


Figure 3. Timing Diagrams for E4 Framing Circuit



WHAT IS LOCK DETECT?

"Lock detect" is the term used to describe the state achieved when a phase-locked loop (PLL) has successfully aligned with an external input signal. All of AMCC's data communications and telecommunications parts incorporate a lock detect feature.

WHY HAVE LOCK DETECT?

AMCC lock detect implementation techniques allow the PLL to retain its lock to the reference clock even in the absence of data. In our clock recovery units, if the lock to the input data stream is lost for any reason, the PLL will immediately lock to the external clock reference, thus ensuring that any parts requiring downstream clocking are not disturbed by the loss of lock.

HOW DOES AMCC IMPLEMENT LOCK DETECT?

Clock Recovery

The clock recovery units (CRUs) on AMCC datacom and telecom receiver chips implement the lock detect feature. The Lock Detect output signal indicates whether or not the PLL is locked to the serial data. This signal has several uses. It:

- Validates the data output to the I/O subsystem. That is, if Lock Detect is false, then the data output cannot be depended on for valid bit error rates.
- Provides an indicator of bad/no data present at the serial data inputs.
- Guarantees continuous downstream clocking with no "glitches" in the Word Clock signal. When the PLL is out of lock, the Word Clock frequency is based on the reference clock. (In a CRU without a reference clock and lock detect, the Word Clock signal would either go to an erroneous frequency, glitch, or stop when the part went out of lock.)

The lock detect function on all AMCC parts is optimized for the particular application. The clock recovery macro decides whether to acquire lock to the serial data inputs or the reference clock inputs, based on a simple state machine. This state machine makes its decision based on the run length and transition density of the serial data inputs—it continuously examines the data stream and monitors the number of

edges in a given number of data cycles. The lock detect criteria for all AMCC CRU parts are shown in Table 1. If the run length and transition density checks are satisfied, PLL control is transferred to the serial data. The S3012 raises the lock detect signal at this point. For all other AMCC receiver chips the lock detect signal goes high after approximately 2000 serial clock cycles. (These 2000 serial clock cycles are required in order to guarantee that the recovered clock is centered in the eye opening of the received data.) During that 2000 serial clock cycle time, the serial data is provided by the CRU, but it exhibits a bit error rate which initially exceeds the 10^{-12} requirement.

If at any time during the reception of data the run length or transition density checks are violated, the state machine will force the PLL to lock to the reference clock. The Lock Detect signal will go low when this occurs. This guarantees that the PLL will maintain the correct frequency in the absence of data.

Table 1. Data Lock Criteria

Part No.	Transition Density Check	Run Length Check
S3006	12.5%	64 bit
S3012	12.5%	96 bit
S3014	12.5%	128 bit

Clock Synthesis

AMCC transmitters also implement a lock detect feature in their clock synthesis macros. Here, the Lock Detect output signal indicates that the PLL is locked to the reference clock. This signal has two primary uses. It:

- Validates the Word Clock output to the I/O subsystem. That is, if Lock Detect is false, then the Word Clock outputs should not be depended on for valid frequency.
- Provides an indicator of bad/no clock present at the reference clock inputs, implying that the reference clock oscillator should be checked for malfunction.
- Confirms that phase error is < 5%.

PLL Board Layout Guidelines

Phase Locked Loops are sensitive to noise on input signals and power supplies. When PLLs are closely associated with digital logic, as in AMCC's ASSPs with PLLs and PLL arrays, care must be taken to protect the analog portions of the circuit from the effects of noise sources both on-chip and on neighboring devices. The isolation of on-chip noise sources is a key concern during the design and layout of the device. All isolation depends on careful board layout for optimum performance.

AMCC's circuits have specific requirements for the isolation and decoupling of the signal and power pins associated with the analog functions of the Phase Locked Loop. In addition, external loop filter capacitors are used on all PLLs. While this capacitor is mounted on the package for the standard 68 LDCC and 100 LDCC, the PLCC and PQFP/TEP packages use dedicated signal pins and board mounted capacitors.

Analog vs. Digital Power Supply Hookup

The analog power and ground pins of a packaged ASSP or PLL array supply individual functional elements within the phase locked loop. This allows these elements to be isolated from each other as well as from the general purpose digital logic section.

On some products, this separate assignment is indicated by the naming convention for the analog power and ground pins. In a mixed voltage part the assignment is:

- AGND0/AVEE0—Loop Filter
- AGND1/AVEE1—VCO
- AGND2/AVEE2—Phase Detector and Serial Input Buffers
- AGND3/AVEE3—Bit and Byte Clock Dividers
- AGND4/AVEE4—Serial Output Buffers

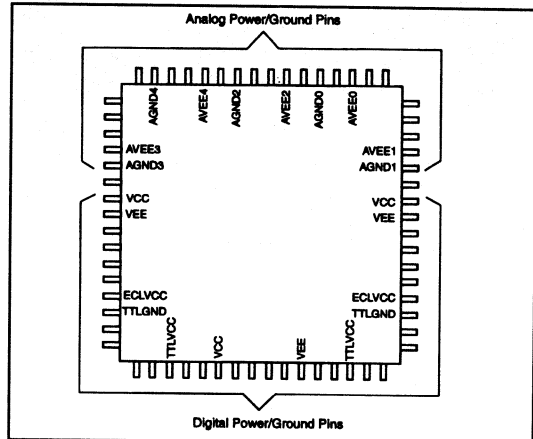
This is the general assignment of the major functional elements. Depending on the complexity of a given PLL function, additional logic for loop initialization, activity and lock detection and test/bypass modes can be included, usually powered by AGND3/AVEE3.

Since the PLL function is isolated in approximately the top 10% to 25% of the device, these uniquely named pins appear "wrapped" around one side of the package. This can be seen in Figure 1, a representative, although hypothetical PLL array in a Leaded Chip Carrier (LDCC) package.

Of these pin pairs, AGND3/AVEE3 is the least sensitive to AC noise but is the most sensitive to DC offsets with respect to the general logic portions of the device, since serial clocks, data and control information must cross this boundary. Communication with the other PLL functional sections is by differential signals.

The remaining power and ground pins serve the general purpose digital portion of the array and are treated in the same manner as on conventional ASIC and ASSP devices. The core and I/O supplies are separately identified in order that specific noise generators such as TTL outputs can be decoupled. The TTLVCC (usually +5 volts) and TTLGND (usually 0 volts) supply the totem pole current for TTL outputs. In addition, devices such as serial receivers may have parallel output busses of as many as 32 signals. On those devices additional power pins labeled ITPWR and ITGND are provided. These pins must all be provided with sufficient decoupling in order to prevent the noise generated by simultaneous switching (FFFF to 0000 on a 32 bit bus) from affecting the PLL functional elements.

Figure 1.

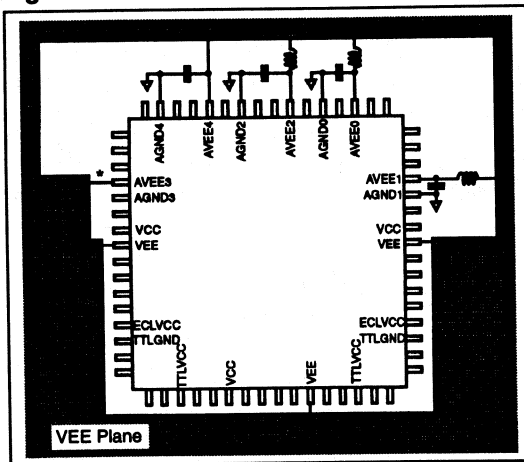


Placement of Capacitors and Inductors

Decoupling should be applied on a per-pin basis. Ceramic chip capacitors, and ferrite beads or surface mount ferrite beads should be used as shown in Figure 2.

DC voltage differentials between Analog VEE and Digital VEE should be minimized. When so identified, AVEE0, 1 and 2 should be no more than 250 mv from Digital VEE. Use one inductor per AVEE pin to minimize the DC drop due to current in the PLL circuitry. It is recommended that the DC resistance of the inductors should be 1 Ohm or less and the AC impedance should be on the order of 50 Ohms at 20MHz. Suggested inductors include Murata BLM32A06 or Mouser P/N 542FB73-226 Ferrite bead. AVEE3 and AVEE4 should not use inductors, but capacitive decoupling should be provided for AVEE4.

Figure 2.



* When separately identified, AVEE3 which drives the PLL digital logic, should be connected directly to the Digital VEE plane. The voltage differential between AVEE3 and Digital VEE should be no greater than 20mv.

High Freq/Low Freq Decoupling

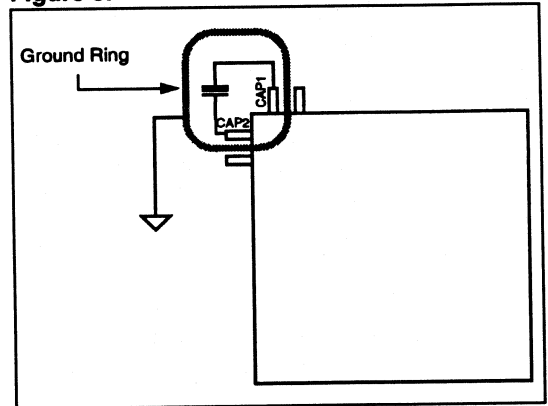
Capacitors shown in the drawing should use paralleled 100pf/0.1µf ceramic chip capacitors for broadband decoupling. X7R or BX dielectric is acceptable.

These decoupling networks are in addition to the decoupling of the Digital power pins required in good design practice, ie 0.01 to 0.1 µf per core or I/O power pin and 1 µf/watt of low frequency within 1 cm of the device.

Placement of External Filter components

ASSPs with PLLs and PLL arrays in plastic, TEP, or the 132 LDCC packages require the external capacitor for the loop filter to be placed on the circuit board. These pins are called out as CAP1 and CAP2. These connections control the internal VCO and are sensitive to coupled noise at the nanovolt level. Ground ring isolation should be used to isolate this capacitor from board traces carrying switching signals or power/ground supply currents. There should be only one connection point to the ring to avoid voltage gradients across the ring. This is shown in Figure 3.

Figure 3.



For PLL designs where package and pin-outs allow it, ground or n/c pins should be used to allow a complete ground ring to be implemented. This is particularly critical on fine pin-pitch packages. The ground ring should be tied to a quiet ground plane, not a current carrying bus.

Signal Termination and Line Impedance

ASSPs and PLL arrays must be capable of transmitting and receiving high bandwidth serial data signals with a minimum of induced or applied error in the phase and time domain. Reflected signals from impedance mismatches at the package/pcb boundary, as well as those due to poor placement of terminating impedances can be as damaging to system performance as violation of the decoupling and layout guidelines described above.

AMCC uses source-terminated outputs for most serial data above 500 Mb/s and clocking signals greater than 500 MHz. The 50 Ohm output impedance on the die matches the impedance of the dedicated package trace. This uniform impedance should be matched to the circuit board trace to minimize reflections. Since these critical outputs are differential, the board traces should also be carefully matched for electrical length (propagation delay). For example, a length mismatch of 2 cm due to accumulated "bends" in a pair of parallel 50 Ohm traces could result in a 6% duty cycle distortion in a 1 Gb/sec signal. Delays should be matched to within 25 ps for 1Gb/sec signals.

The corresponding high bandwidth differential receivers used on AMCC PLL arrays include internal 100 Ohm line-to-line termination. This matches the dual 50 Ohm lines described above. See Figure 4.

If an AMCC source terminated output is driving a differential input that is not internally terminated, an external termination must be provided as shown in Figure 5. This is usually the case when driving the ECL input of a fiber optic transmitter. The terminating resistor should be placed as close to the input pins as possible, using a surface mounted component.

For signals that operate significantly below 500 MHz, AMCC uses a conventional ECL differential output structure. This approach minimizes on-chip power dissipation with negligible effect on the quality of moderate bandwidth signals.

This may also be the only style of differential output available on a fiber optic receiver. In both cases the ECL emitter-follower outputs must be provided with current sourcing resistors. These resistors should also be located as close to the output pins as possible (less than 1 cm) and surface mount components are strongly recommended. This configuration is shown in Figure 6.

Figure 4.

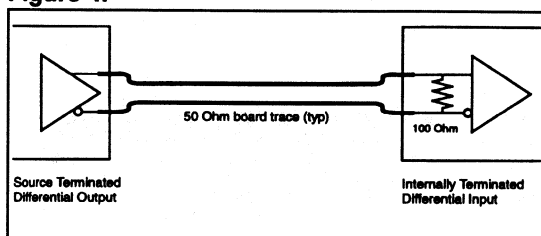


Figure 5.

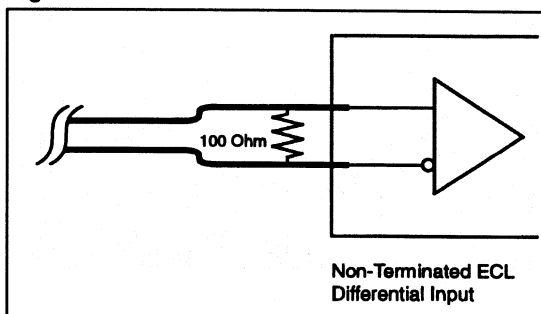
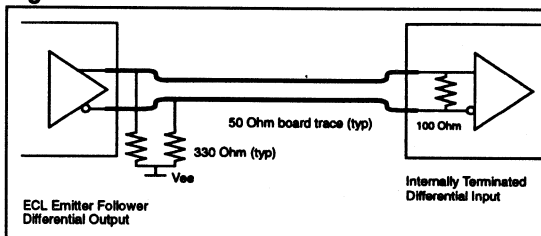


Figure 6.



SONET/SDH/ATM S3011A/S3012A Examples

The S3011A and S3012A have essentially identical power pin footprints. The S3011A omits the AGND2/A+5V2 pair, and the CAP1/CAP2 capacitor should be 0.01 μ f for the S3011A. Figure 7 illustrates the connections for the S3011A transmitter device. The ground ring is shown around the loop filter capacitor. The ring should be completed under the device to include pins 79, 80 and 1,2. The values of the decoupling components are as described in the generic example on page 9-10.

The S3012A omits the AGND4/A+5V4 pair and the CAP1/CAP2 capacitor should be 0.1 μ f for the S3012A. Figure 8 illustrates the connections for the S3012A receiver device. The ground ring is shown around the loop filter capacitor. Again, the ring should be completed under the device to include pins 79, 80 and 1,2. The values of the decoupling components are as described in the generic example on page 9-10.

Figure 7.

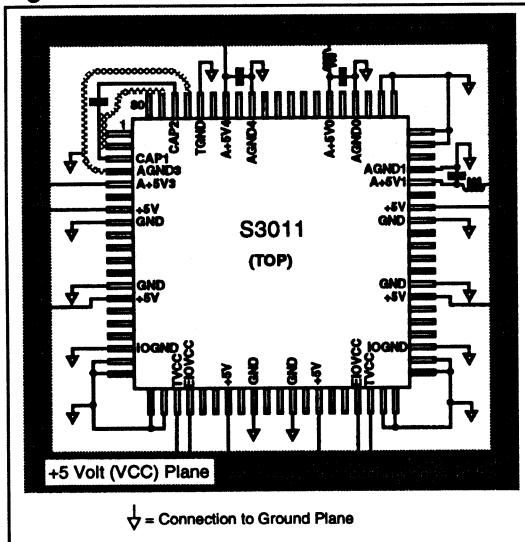
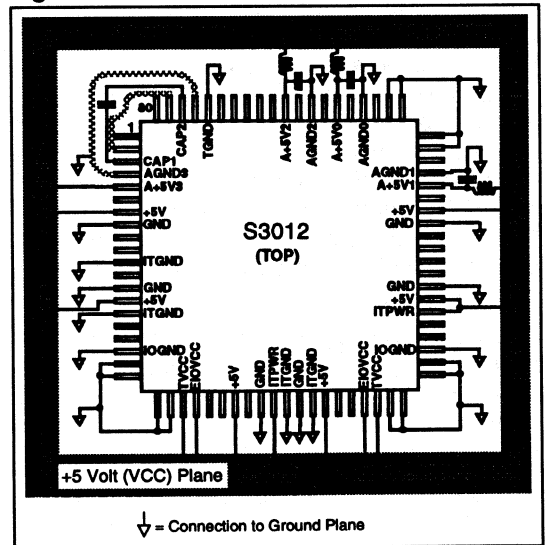


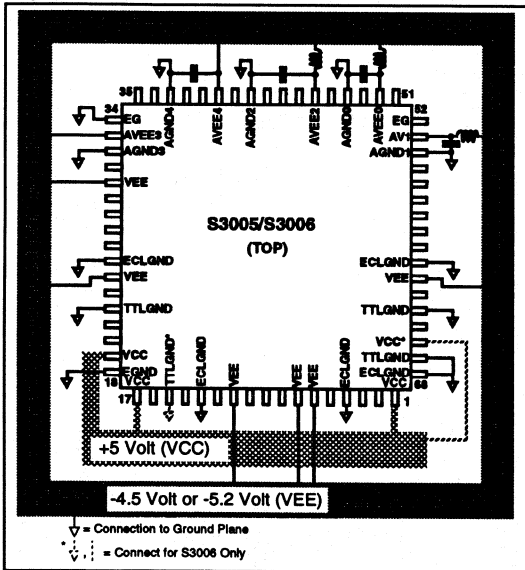
Figure 8.



SONET/SDH/ATM S3005A/S3006A Examples

The S3005A and S3006A have identical power pin footprints. For these devices in the 68 LDCC package, the filter clean-up capacitor is mounted on the package, simplifying board layout. Since these devices use dual supplies, Figure 9 shows the VCC connection to a +5 volt plane needed for the TTL control and data interface. The values of the decoupling components are as described in the generic example on page 9-10.

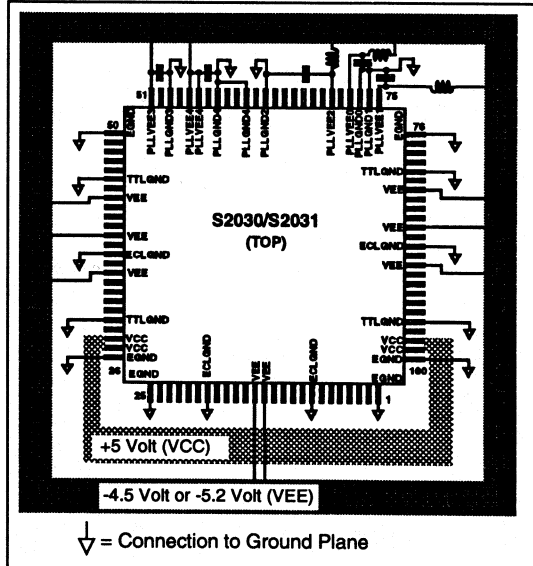
Figure 9.



Fibre Channel Interface S2030A/S2031A Example

The S2030A and S2031A have identical power pin footprints. For these devices in the 100 LDCC package, the filter clean-up capacitor is mounted on the package, simplifying board layout. Since these devices use dual supplies, Figure 10 shows the VCC connection to a +5 volt plane needed for the TTL control and data interface. The values of the decoupling components are as described in the generic example on page 9-10.

Figure 10.



Fibre Channel Interface S2039A/S2040A Example

The S2039A and S2040A have essentially identical power pin footprints. For these devices in the 132 LDCC package, the filter clean-up capacitor should be connected between CAP1 and CAP2. The value for the S2039A is 0.022 μ fd. The ground ring should surround the capacitor to the extent permitted by pin spacing and board layout rules. Since these devices use a single +5 Volt supply, Figures 11 and 12 show the connection of AVEE pins to the ground plane and the connection of AVCC pins to the +5 Volt plane either directly or via ferrite bead inductors. Figure 11 shows the connection of AVEE4 at pin 75 for the S2039A, and added TTLGND at pins 42 and 126. These pins are used for signals on

the S2040A. The values of the decoupling components are as described in the generic example on page 9-10.

The clean-up capacitor value for the S2040A receiver is 0.039 μ fd. The ground ring should surround the capacitor to the extent permitted by pin spacing and board layout rules. The S2040A also has added AVEE4 and AVCC4 pins which require an additional decoupling capacitor. It should be noted that the power pins that are not common between the two devices are used for signals on the S2039A. The values of the decoupling components are as described in the generic example on page 9-10.

Figure 11.

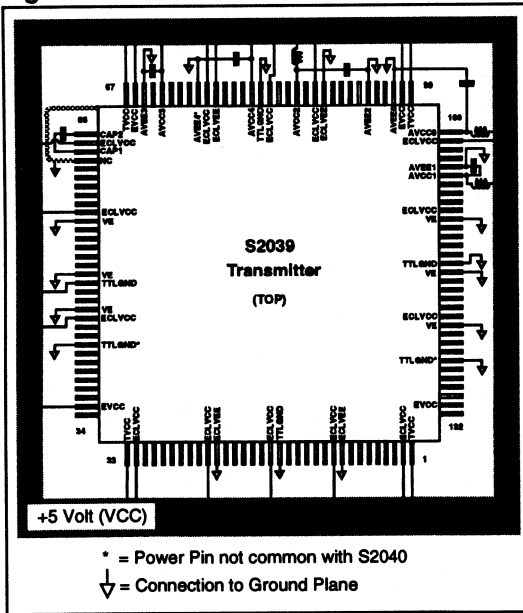
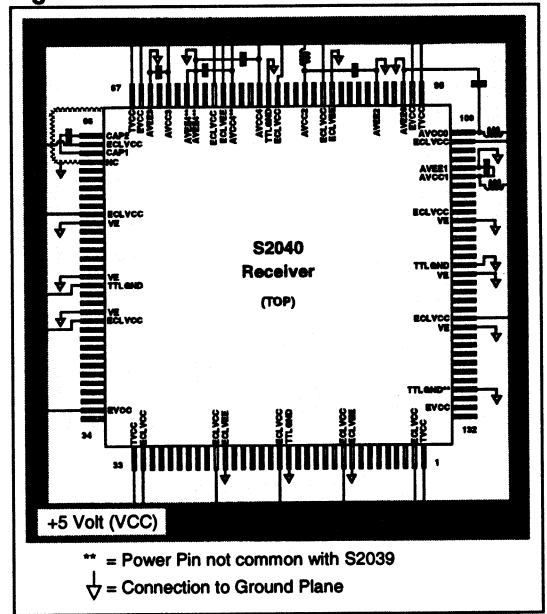


Figure 12



S2032A/S2033A High Performance Serial Interface Examples

The S2032A and S2033A have similar but not identical power pin footprints. For these devices in the 68 LDCC package, the filter clean-up capacitor is mounted on the package, simplifying board layout. The values of the decoupling components are as described in the generic example on page 9-10.

The power pin footprint for the S2033A is shown in Figure 14. Please note the different locations for AVEE4 (pin 35) and AVCC0 (pin 51) from the S2032A, shown in Figure 13. As before, the values of the decoupling components are as described in the generic example on page 9-10.

Figure 13.

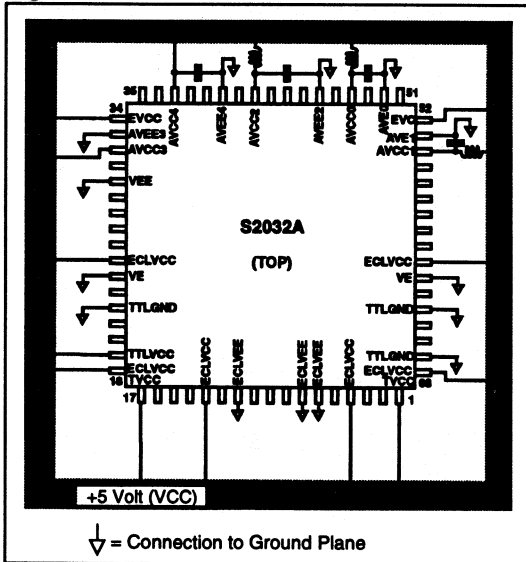
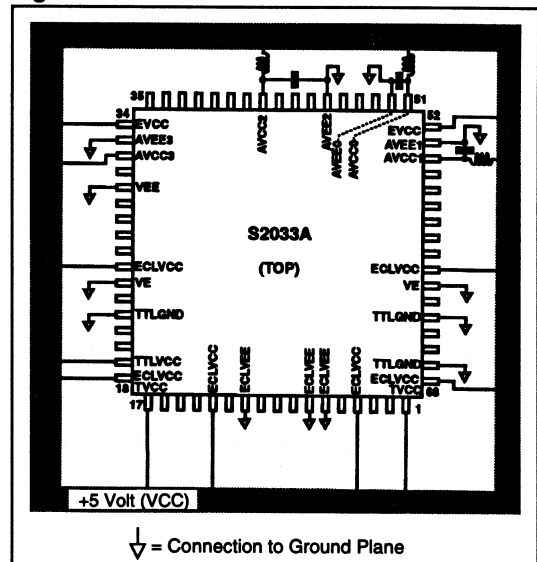


Figure 14.



The S2032B and S2033B are also available in the 80 TEP package. Again, the two devices have similar but not identical power pin footprints. For this package option the filter clean-up capacitor should be connected between CAP1 and CAP2. The value for the S2032 is 0.022 μfd . The ground ring should surround the capacitor as shown in Figure 15. The values of the decoupling components are as described in the generic example on page 9-10.

The clean-up capacitor value for the S2033B receiver is 0.039 μfd . The ground ring should surround the capacitor as shown in Figure 16. Please note the different locations for AVEE0 (pin 62) and AVCC0 (pin 63) from the S2032A. The values of the decoupling components are as described in the generic example on page 9-10.

Figure 15.

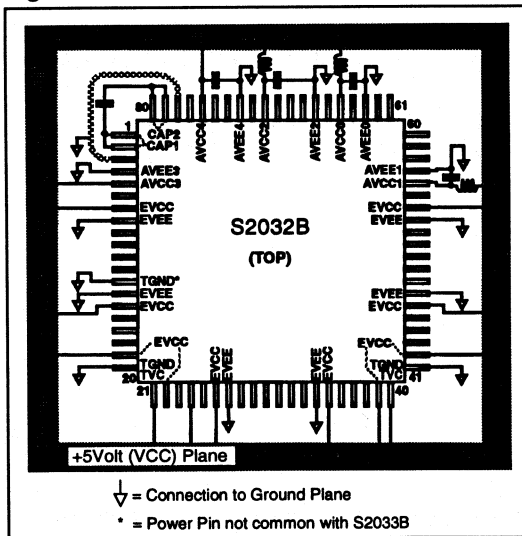
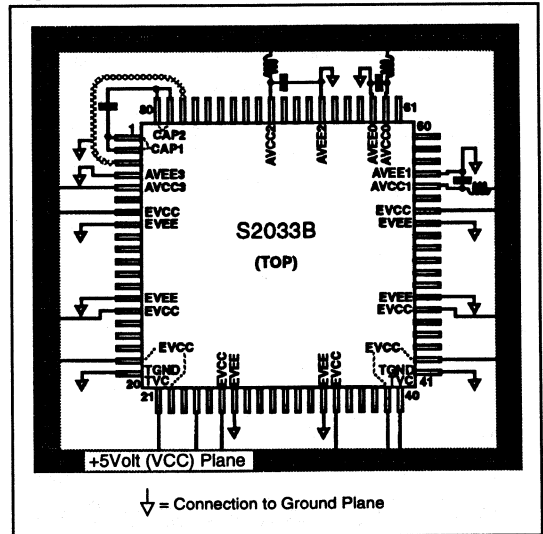


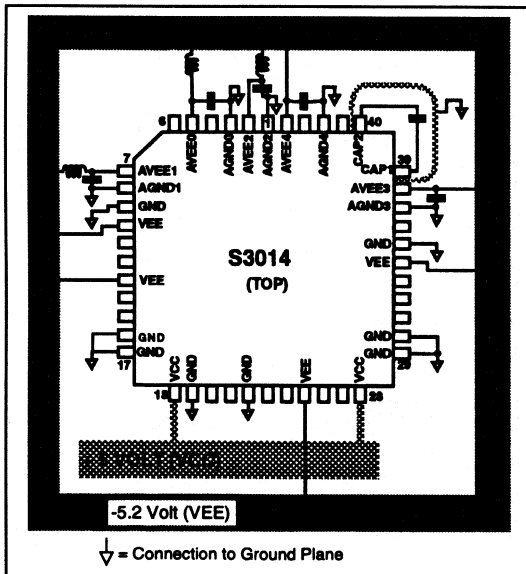
Figure 16.



SONET/SDH/ATM CSU/CRU S3014A Example

The S3014A provides either clock synthesis (CSU) or clock recovery (CRU) functions. For these devices in the 44 PLCC package, the filter clean-up capacitor of 0.1 μf d should be connected between CAP1 and CAP2. The ground ring should surround the capacitor to the extent permitted by pin spacing and board layout rules. Since this device uses dual supplies, Figure 17 shows the VCC connection to a +5 volt plane needed for the TTL control and data interface. The values of the decoupling components are as described in the generic example on page 9-10.

Figure 17.



E4/STM-1/OC-3/ATM S3015/S3016 Examples

The S3015 and S3016 have similar power pin footprints. The CAP1/CAP2 capacitor should be 0.01µf for the S3015. Figure 18 illustrates the connections for the S3015 transmitter device. The ground ring is shown around the loop filter capacitor. The ring should be completed under the device connecting pins 51 and 2. Please note that pin 2 should be directly connected to the ground plane to avoid current through the ground ring. The values of the decoupling components are as described in the generic example on page 9-10.

The S3016 has a similar power pin footprint to the S3015. For the S3016, the CAP1/CAP2 capacitor should be 0.1µf. In addition, please note that AVEE5 and AVCC5 on pins 21 and 24 are added to provide power for the equalizer network buffer. The ground ring is shown around the loop filter capacitor. The ring should be completed under the device connecting pins 51 and 2. Please note that pin 2 should be directly connected to the ground plane to avoid current through the ground ring. The values of the decoupling components are as described in the generic example on page 9-10.

Figure 18.

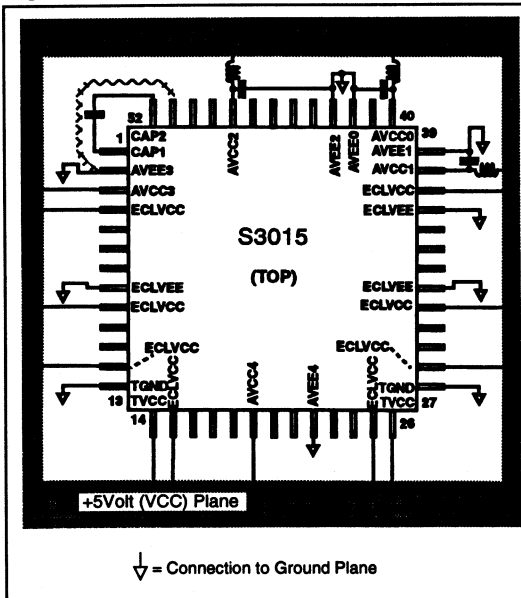
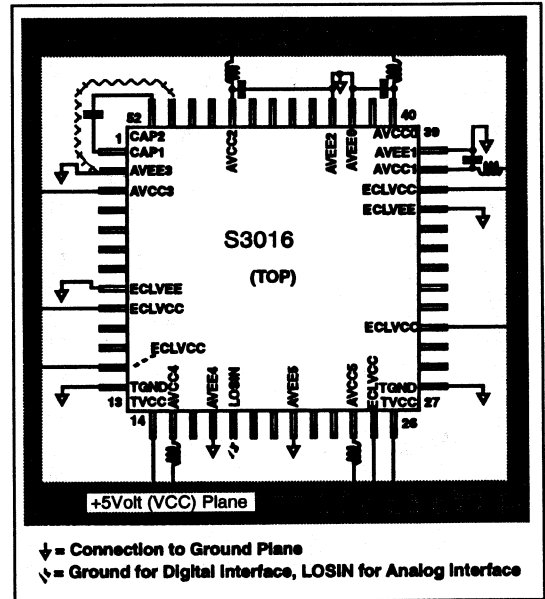


Figure 19.



MANAGING AND MEASURING JITTER IN A GIGABIT LINK

INTRODUCTION

This application note describes management and measurement of jitter in Fibre Channel and SONET serial links, using AMCC's families of SONET/SDH and Fibre Channel transmitter and receiver circuits, as well as links implemented using AMCC's PLL arrays. It discusses design techniques for jitter minimization, describes equipment needed for jitter measurement, and provides connections and set-up descriptions.

RELEVANCE OF JITTER IN HIGH-SPEED SERIAL LINK DESIGN

Jitter is defined as short-term phase variations of the significant instants of a digital signal from an ideal clock running at the same average rate as the signal. "Significant instant" refers to any clearly defined point on the waveform, such as a zero crossing. "Short-term" specifically means phase oscillations of at least 10 Hz. (Lower-frequency phase noise is generally referred to as "wander.") Jitter can be measured in peak-to-peak "unit intervals" (UI). One UI is equal to the period of the ideal clock, or one baud interval, at the data rate specified. This method of representing jitter is useful in facilitating comparison of different data rates.

Since jitter can introduce bit errors and cause loss of synchronization in high-speed links, it is crucial for the designer to be aware of the causes of jitter and to attempt to minimize it as much as possible through-out the system. Both the SONET and Fibre Channel standards contain rigorous jitter specifications. Each standard specifies jitter somewhat differently, as described in the following sections.

SONET Jitter Specification

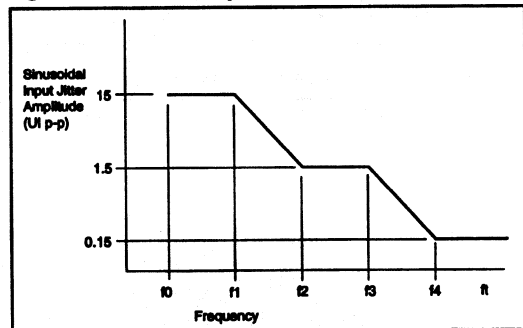
The SONET standard allows the asynchronous payloads to "float" inside the synchronous frame, to accommodate varying clock rates. These "pointer" movements occur in byte-wide steps at irregular intervals, which can cause large jitter to be introduced in the payload. Additional jitter is introduced by mismatched oscillators in the signal regenerators of self-timed systems.

Input jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input sig-

nal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 1. The measurement condition is the input jitter amplitude which causes an equivalent of 1 dB power penalty. The template basically defines an area over which the equipment must operate without experiencing the designated performance degradation.

Jitter generation is defined as the amount of jitter at the OC-N/STS-N output of a piece of SONET equipment. It shall not exceed 0.01 UI rms when measured using a highpass filter with a 12-kHz cutoff frequency.

Figure 1. SONET Input Jitter Tolerance



OC/STS Level	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	f4 (kHz)
3	10	30	300	6.5	75
12	10	30	300	25	250

The *jitter transfer function* is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. The jitter transfer requirements are shown in Figure 2.

Fibre Channel Jitter Specification

In the Fibre Channel standard, the general pulse shape characteristics include rise time, fall time, pulse overshoot, pulse undershoot, and ringing. The general parameters specifying the mask of the transmitter eye diagram are shown in Figure 3. The 10⁻¹² BER requirement is guaranteed by specifying the

Figure 2. SONET Jitter Transfer

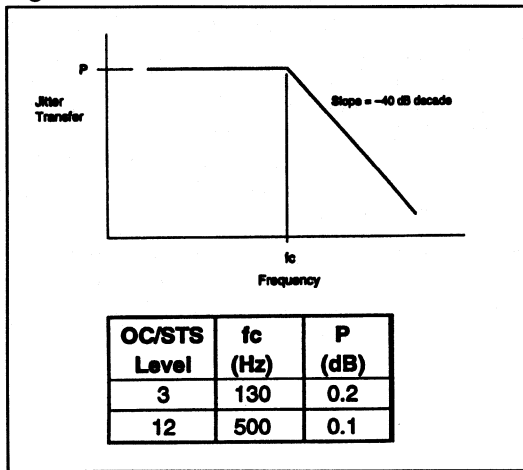


Figure 3. Fibre Channel Jitter Mask

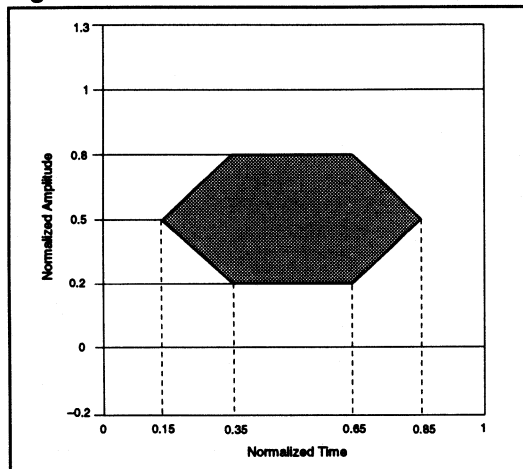
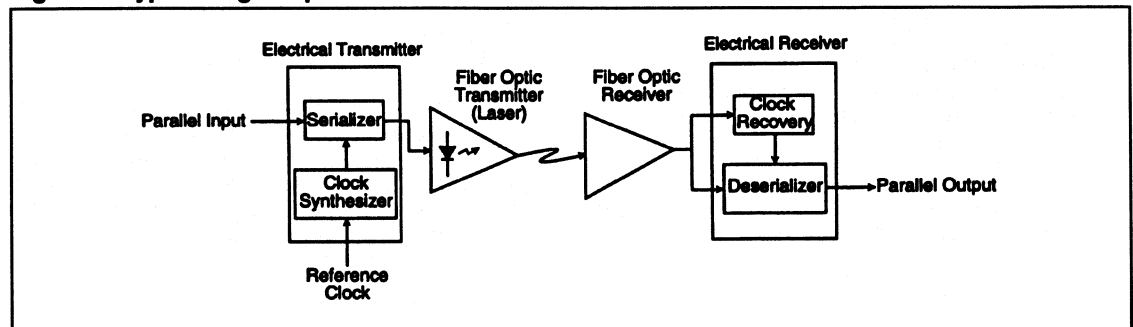


Figure 4. Typical Gigabit-per-second Serial Link



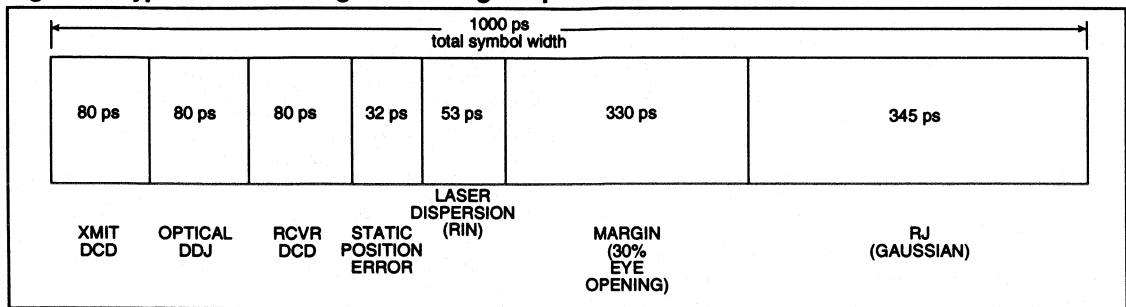
transmitter eye diagram, and the fiber cable plant and the minimum and maximum received power levels. The specified values take into account power penalties caused by the use of a transmitter with a worst-case combination of transmitter spectral, extinction ratio, and pulse shape characteristics. Fibre Channel does not include a specification for jitter frequency because there is no requirement for repeaters as in the SONET standard.

JITTER BUDGET

A typical gigabit-per-second serial link, illustrated in Figure 4, is made up of several components. These include the reference clocks, electrical transmitter, optical transmitter, optical receiver, and electrical receiver. Each system component has its associated jitter specification, management, and measurement requirements, and the designer must work within a jitter budget that allocates a certain amount to each component. The diagram in Figure 5 shows a typical jitter budget as "slices" of a data bit for a system running at 1 gigabit-per-second (ideal symbol width=1000ps). The "slices" are defined as follows:

- Transmit duty cycle distortion (DCD) jitter, caused by propagation delay differences in the transmitter between high-to-low and low-to-high transitions. DCD shows up as a pulse width distortion of the nominal baud time.
- Optical data dependent jitter (DDJ), the jitter related to the transmitted symbol sequences. DDJ is caused by the limited bandwidth characteristics, nonideal individual pulse responses, and imperfections in the optical channel components (related to the fiber optic cable).

Figure 5. Typical Jitter "Budget" for a Gigabit-per-second Serial Link



- Receiver data dependent jitter, caused by the limited bandwidth of the receiver. The optical receiver is typically designed for matched filter response to obtain maximum sensitivity. This results in DDJ when multiple baud times of data in a fixed 1 or 0 state are followed by a single baud time in the opposite state.
- Static position error, which is the error associated with the sampling accuracy (or, how close the timing pulse is to the optimum sampling point, or center of the eye).
- Laser dispersion, also called Relative Intensity Noise (RIN), which is the jitter caused by fluctuations in the intensity of optical power in the laser cavity due to optical reflection into the cavity.
- Margin (30% eye opening), which is the resulting eye opening from which the clock recovery device must extract the clocking information.
- Random jitter (RJ), the jitter due to Gaussian noise sources. The peak-to-peak value of RJ is of a probabilistic nature and any specific value requires an associated probability.

TECHNIQUES FOR MANAGING AND MEASURING JITTER

Each link component requires different jitter minimization design techniques, as well as jitter measurement/characterization methods to ensure that the design techniques employed have been successful. The following sections discuss each component of a typical transceiver module design in turn, providing suggestions for managing jitter and describing the measurement equipment and connections for each.

Bear in mind that a great deal of thought should be given *in the beginning of the design process* to the eventual measurement and characterization needs of the system. It is painful to try to recover a buried signal that is needed for testing after the design is

complete! Therefore, when designing your board, take care to build a degree of flexibility into the design. For example, allow access on your board to the parallel and serial ports separately, so that you are later able to connect them in any configuration needed for testing. Allow for numerous "hooks" into your system.

Equipment Needed

To fully characterize or test a high-speed serial link design, the following test equipment may be needed, depending on the types of tests being performed:

- Bit error rate tester (BERT) (the HP70004A display and HP70841B pattern generator or HP70322A synthetic generator are recommended)
- Coaxial attenuator, 0-7 dB in 1-dB increments, with female SMA connectors.
- 50-Ω coaxial power splitter with female SMA connectors.
- Digital sampling oscilloscope (HP54120, Tektronix CSA803, or similar).
- Delay line(s) for oscilloscope (the HP54008A, Tektronix DL11, passive delay line, or similar).
- Any necessary power supplies.
- Spectrum analyzer (HP8561B or similar).

Overall Design Considerations

There are some general guidelines for jitter management that apply to the link design as a whole. In general, noise isolation should be a primary consideration throughout the entire design process, as PLLs are sensitive to noise on input signals and power supplies. (See AMCC Application Note #4, *PLL Board Layout Guidelines*.) Low-noise power supplies should be selected for critical analog functions. Extra care should be taken to minimize the switching transients of heavily loaded bus interface drivers.

Transmission line effects should also be taken into consideration. As a general rule, transmission lines should be used when L_{max} is greater than $9T_r$ (L_{max} in centimeters and T_r in nanoseconds). At data rates of 1 gigabit ($T_r = 200$ ps), then L_{max} is only 1.8 cm. In general, it is wise to use "good" transmission lines for all gigabit signals.

Jitter Characterization and Testing

Figure 6 shows a simplified link board design, with typical connections common for testing. A variety of test configurations may be used, depending on the test being conducted. A general optical test set-up is shown in Figure 7, and a general electrical test set-up for a coaxial board is shown in Figure 8. When Testing very high-speed signals, it is often not possible to branch or load the line at every desirable test point, due to signal reflection problems. In cases where it is not feasible to tie directly onto the line itself, self-loop or link loop outputs can be used to monitor the signal. In Figure 6, 7, and 8, some test equipment is shown connected to the link loopback clock and data signals. SMA connector footprints are shown in these figures. The connectors would be included on the board for testing purposes only, and

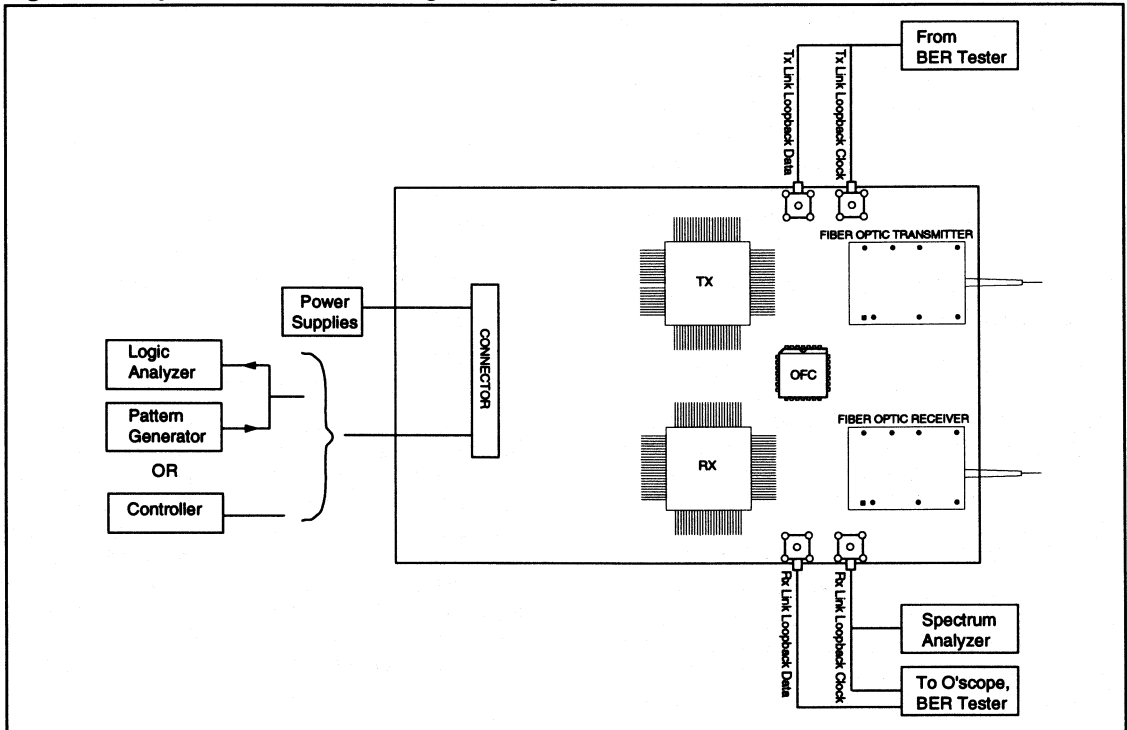
would not need to be populated during final board production.

Testing the link as a whole—in other words, examining the parallel data into the parallel port of the transmitter and examining the data emerging from the parallel port of the receiver—is a good place to start as it allows you to spot any obvious errors immediately and to make sure that the TTL board-wide interfaces are correct. Then, you can break the system down into its various pieces and examine them separately, as discussed in later sections of this note.

The following checklist offers suggestions for uncovering board-wide errors:

1. In the data domain, observe the bit errors at the parallel (word) interface level. This can typically be done using software resident in your system controller or using a parallel BERT, as this feature is implemented in many software packages. If what you observe on the receiver parallel output is not the same as what was sent into the transmitter input, then there is likely to be some violation of timing limits (set-up and hold) at the parallel interface. Possible culprits are:

Figure 6. Simplified Link Board Design Showing Connections Common for Testing

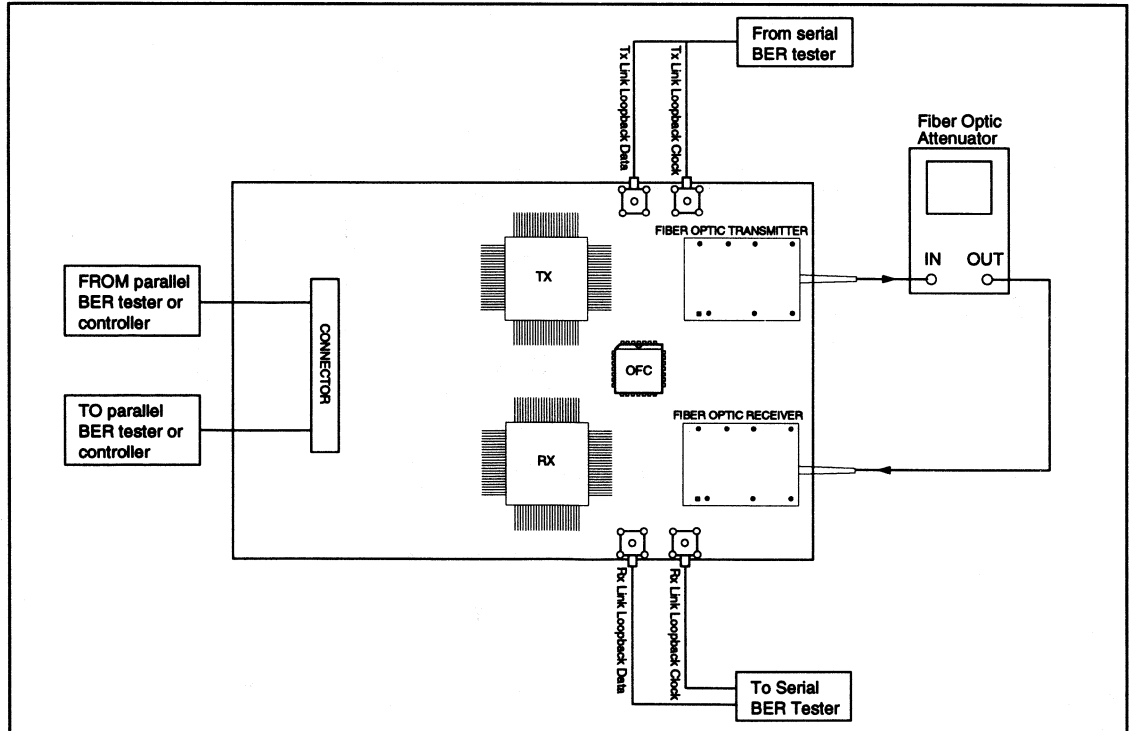


- For SONET transmitters, phase drift of the parallel load clock, detectable as Phase Alignment errors (PAE).
 - For Fibre Channel transmitters, the set-up/hold limits are specified with respect to a WORDCK output, and you must ensure that the clock is configured correctly.
2. At the receiver output, there is another external system setup/hold specification into the controller device. You may be getting stable data out of the part, but you must also make sure that the data is getting into the next part correctly. Verify and validate setup/hold of your controller device and the parallel bus.
3. Some higher-level testers have the ability to do bit error rate test (BERT) in the parallel transmit/serial receive mode. This allows further isolation, in the case of intermittent or low occurrence rate errors. Serial data out of the transmitter should be checked

in the time domain for correct frequency (bitrate). Make sure that the correct reference frequency and operating mode have been selected.

When using an oscilloscope for jitter testing and measurement, note that AMCC's source-terminated ECL output can be tied directly to 50Ω -to-ground connections, greatly simplifying the measurement process. Using a direct connection is perfectly adequate when you are looking only at timing and jitter information. However, if you need to make precise dc-level measurements, you will need to use ECL terminators, as shown in Figure 9. Note that a non-standard bias voltage is used for the terminators, since source-terminated outputs must be terminated single-ended as 50Ω to -1.050V, as opposed to the -2.45V bias needed to give 50Ω to -2.0V on standard ECL. On-board level shifters are not included in the serial data paths to minimize jitter on this critical path.

Figure 7. General Optical Test Setup for Jitter Measurement



Power Supply and Other Noise Sources

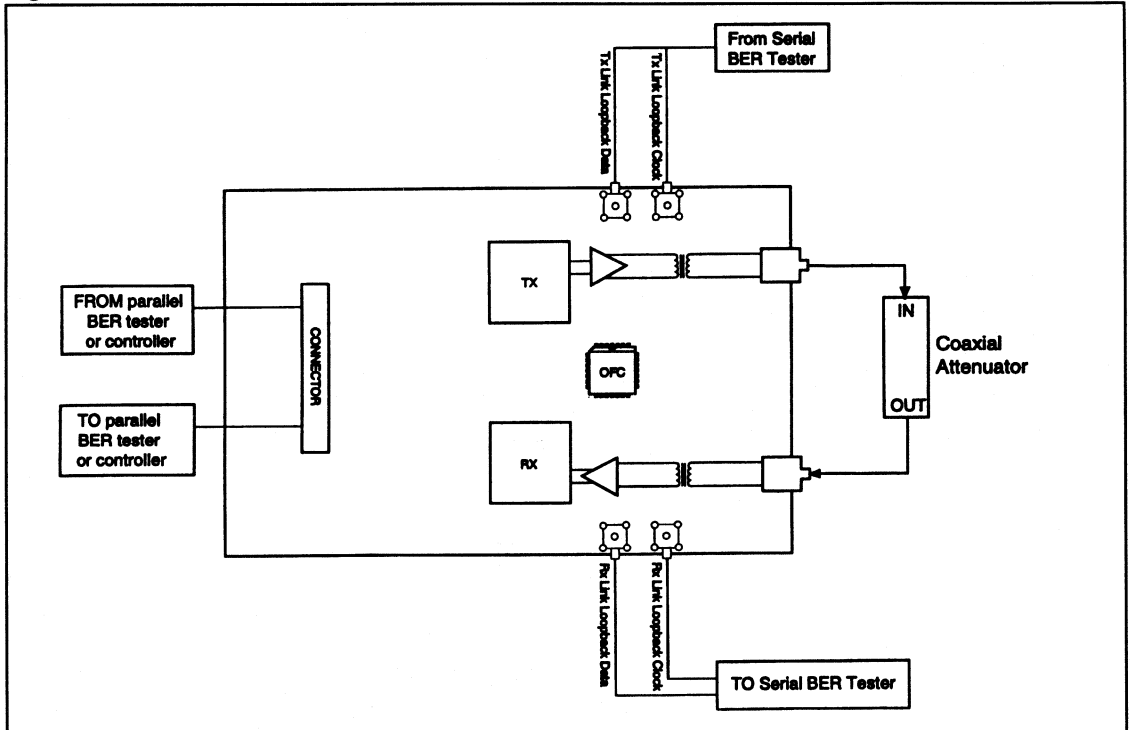
Power supply decoupling is one of the most important elements for jitter minimization. Decoupling should be applied on a per-pin basis. Ceramic-chip capacitors and ferrite beads should be used in the board design.

The phase-locked loops (PLLs) are especially sensitive to power supply noise (as well as noise on input signals). AMCC circuits have special requirements for the isolation and decoupling of the signal and power pins associated with the analog functions of the PLL. In addition, external loop filter capacitors must be placed on the circuit board. The capacitor

connections are sensitive to coupled noise at the nanovolt level. Ground ring isolation should be employed to isolate this capacitor from board traces carrying switching signals or power/ground supply currents. The ring should have only one connection point, to avoid voltage gradients across it. Refer to AMCC Application Note #4, *PLL Board Layout Guidelines*, for more details on layout issues.

The following sections discuss jitter management and measurement issues for each individual link component.

Figure 8. General Electrical Test Setup for Jitter Measurement



MANAGING AND MEASURING JITTER IN A GIGABIT LINK

Reference Clocks

Jitter Management

Good jitter management begins with the selection of the reference clock source. The transmitter reference clock is the most important in terms of noise management. Some attention, however, must be paid to the receiver reference clock, namely that it be accurately on frequency.

The use of a TTL reference source or a backplane clock as a reference source for the transmitter PLL increases the random jitter of the transmitter data. Using a differential ECL oscillator located adjacent to the transmitter PLL removes the jitter components caused by TTL buffers and backplane noise. Good edge rates and low noise are crucial. If you are using a system clock and attempting to clean it up for use as the reference clock, *you must ensure that the signal is clean and stable*. Good termination techniques are particularly important.

Suitable crystal oscillators can be obtained from numerous suppliers.

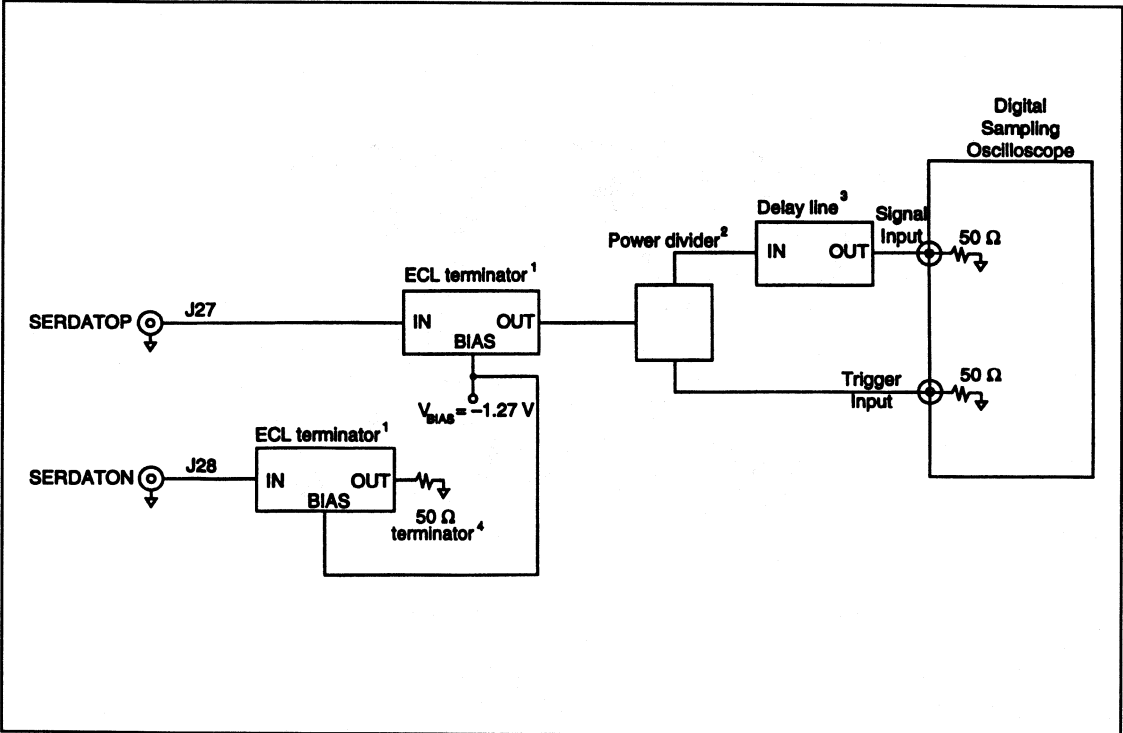
Jitter Measurement

Jitter characteristics of the reference clocks can be viewed using an oscilloscope or spectrum analyzer. (Hewlett-Packard Product Note 54120-2, *Jitter Analysis Using The HP Family of Digitizing Oscilloscopes*, offers detailed information on measuring jitter with an oscilloscope and is a good reference). Table 1 shows the electrical characteristics and jitter generation characteristics that should be exhibited by the reference clock sources.

Table 1. Expected Reference Clock Electrical and Jitter Characteristics

Maximum Reference Clock Jitter in 12 KHz to 1 MHz Band	Operating Modes
14 ps	STS-12
28 ps	STS-3 CMI
56 ps	STS-3

Figure 9. Oscilloscope Connections



Electrical Transmitter

Jitter Management

The jitter introduced at the electrical transmitter to optical transmitter interface is typically duty cycle distortion caused by the inherent rise and fall mismatch of typical ECL emitter-follower drivers. This problem is alleviated in AMCC's Fibre Channel and SONET chipsets through the use of high-speed source-terminated ECL-compatible I/O drivers that have significantly less pulse width distortion than standard ECL drivers.

In the board layout, it is important to follow these basic guidelines:

- Use short traces on the printed circuit board.
- Pay particular attention to component placement. Avoid having crossovers of gigabit and analog signal traces.
- Use the power and ground planes in multilayer PC boards for isolation.
- Treat all traces carrying gigabit signals as transmission lines. Use controlled-impedance, correctly terminated lines.
- Do not use series-terminated transmission lines, as it reduces the effective bandwidth of the line.

Jitter Measurement

Since the transmitter is the simpler PLL system it is usually the easiest to debug first.

First, ensure that the serial clock out of the transmitter is really locked to the reference frequency. (Not all AMCC transmitters have a lock detect output.) If the serial clock is used in a retiming (clocked) electro-optic interface, make certain that the correct sense is used to meet the electro-optic module's setup and hold specifications. In addition, make sure that the data is in the correct sense (both to the electro-optic module and directly to the test set).

The jitter in the transmitted data should be less than 0.01 Unit Interval (UI) rms (for both Fibre Channel and SONET). If this limit is exceeded, further analysis is required in the frequency domain. Observe the serial clock in the frequency domain with a spectrum analyzer. The serial clock should be at the correct frequency, and the "spurs," due to the reference clock, should be at least -30dBc (relative to the serial clock frequency signal).

A digital sampling oscilloscope may be used to view the serial data out of the transmitter. The oscilloscope bandwidth should be at least 1 GHz.

Figure 10.
Expected Fibre Channel Transmitter Eye Diagram

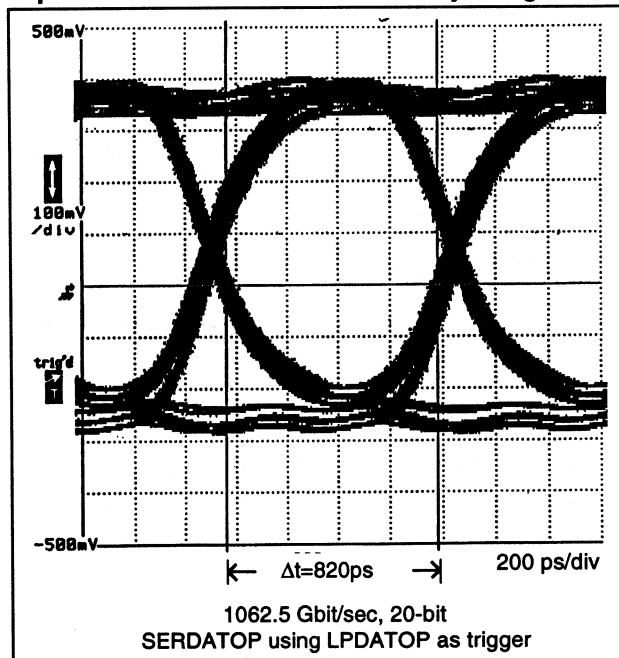


Figure 10 shows a Fibre Channel eye diagram for a transmitter exhibiting “good” jitter characteristics. Figure 11 shows a Sonet transmitter eye diagram exhibiting good jitter levels. Figures 12 and 13 show the corresponding jitter histograms.

Laser (Optical Transmitter) to Optical Receiver Interface

Jitter Management

Jitter caused by the optical interface can be minimized by selecting the proper laser source, the optimum fiber connector type, and the correct fiber optic cable to meet the distance requirements of the system.

The most crucial laser selection options are:

- Short or long wavelength
- Fabry-Perot (FP) or Distributed Feedback (DFB)
- Coherence length

The short-wavelength laser (700-850 nm) provides a higher initial power output, but suffers from higher attenuation in the fiber optic cable than the long-wavelength laser (1270-1350 nm). The Fabry-Perot laser has higher chromatic dispersion in the fiber optic cable than the DFB laser. (Chromatic dispersion

results in DDJ on the optical signal). A laser with a short coherence length minimizes the jitter caused by modal noise and relative intensity noise on multimode fibers.

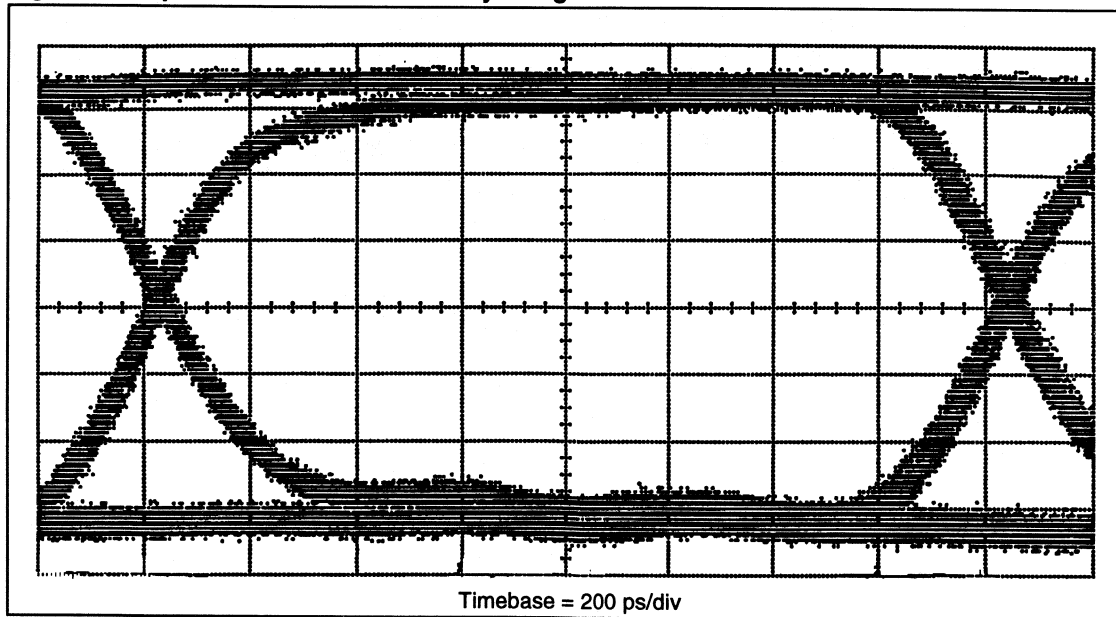
Using splices and/or low-loss connectors for fiber connections reduces relative intensity and modal dispersion noise, as well as overall system attenuation. Splices will, however, make the system much more difficult to reconfigure.

In selecting the fiber optic cable, the designer must consider the cable attenuation characteristics, and must decide between multimode or single-mode. At longer distances (above 500 m) a single-mode fiber is required to minimize the effects of modal dispersion. However, at shorter distances a multimode fiber will deliver more power to the fiber optic receiver. Fiber optic cable attenuation should be optimized to match the selected laser wave length.

Jitter Measurement

Refer to Figure 7 for the general optical test connections. This basic setup will allow you to verify that the optics modules are functioning properly and that the optical-to-electrical-to-PLL interface for the clock recovery is working as it should.

Figure 11. Expected Sonet Transmitter Eye Diagram



Electrical Receiver

Jitter Management

The basic layout techniques discussed in the electrical transmitter section apply here as well. This includes:

- Taking care with the routing from the electro-optic receiver.
- Using proper terminations and designing for transmission line effects.
- Making careful component selection.
- Using the lowest noise operating mode appropriate to the environment.

Jitter Measurement

The test connections shown for the electrical transmitter apply as well as to the electrical receiver. Several possible serial port errors can occur at the receiver. The following checklist may help in locating them:

1. Has the receiver been properly initialized with a 10-ms reset?
2. Have the correct operating frequency, operating mode, and reference been selected via the control signals (SONET) or control register (Fibre Channel) settings?

With the serial input data disabled, observe the Link Loop clock output (if available) or Word Clock/Parallel Output Clock and confirm that it is locked to the reference clock input. In the frequency domain, the clock out of the receiver should appear as a well-defined line with amplitude significantly greater than the reference harmonics and other features.

3. When serial data is applied to the receiver, is the proper input enabled? If the receiver is equipped with a local loop input as well as the normal serial input, there is the possibility of crosstalk if switching activity occurs on the unselected input. Under condi-

tions of minimum amplitude on the selected signal, the energy from the unselected signal could cause degradation in clock recovery performance or even loss of phase lock. This can be prevented by disabling the source of the local loop signal (usually the local loop output of the adjacent transmitter device).

4. Is the serial data bit rate within 1% of the specified rate determined by the reference clock to achieve proper clock recovery? If the bit rate is outside this 1% window, the PLL will appear to lock to other frequency artifacts if the data is a pseudo-random string. A reset cycle is required to recover from this class of false lock.

The spectral domain should again be examined when the receiver is locked to data to confirm that sources of possible contamination, such as reference oscillators and unselected data inputs, are significantly below the amplitude of the recovered clock (bit clock or word clock).

Expected receiver electrical/jitter characteristics for a Fibre Channel link are shown in Figure 12, and for a Sonet link in Figure 13.

REFERENCES

AMCC Application Note #4, *PLL Board Layout Guidelines*.

ANSI X3T9.3 Fibre Channel Standard Document.

Bellcore Synchronous Optical Network (SONET) Transport Systems, Common Generic Criteria, Technical Reference TR-TSX-000253.

CCITT Blue Book, Vol. III - Fascicle 111.4, General Aspects of Digital Systems; Terminal Equipments, G.707-G.709, p. 107-173.

HP Product Note 54120-2, August 1989, *Jitter Analysis Using the HP Family of Digitizing Oscilloscopes*.

Figure 12. Jitter Characteristics for a Fibre Channel Receiver

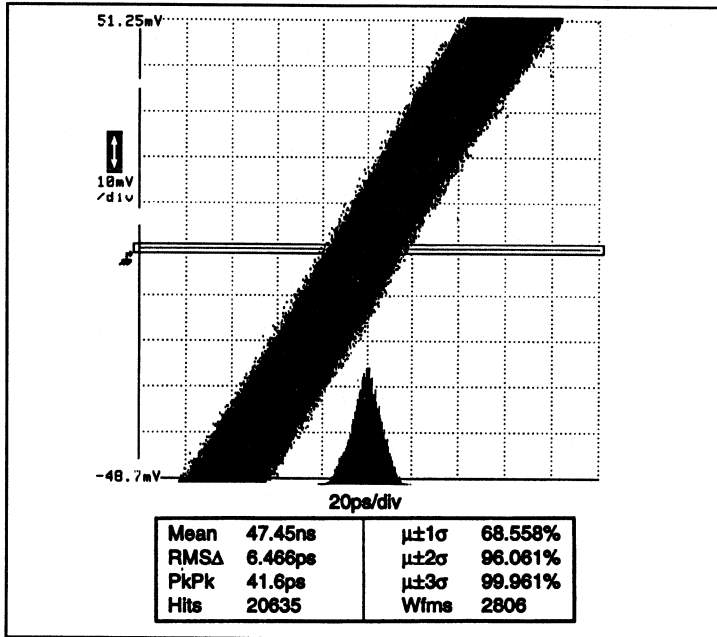
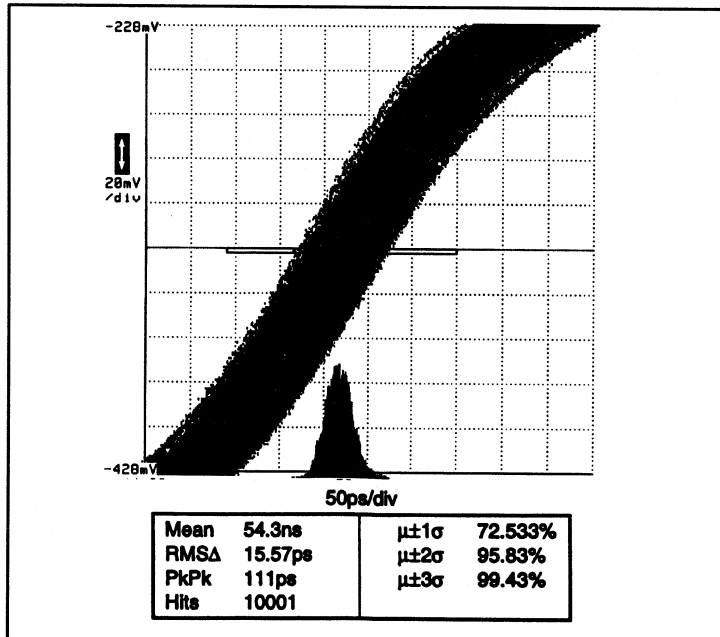


Figure 13. Jitter Characteristics for a Sonet Receiver



INTRODUCTION

One of the principal challenges facing a digital design engineer at either the device or system level is that of assuring that high speed/high bandwidth signals actually pass through the packaging interface in a usable form. The edge rates achievable with Bipolar and BiCMOS I/O structures combined with VLSI and ULSI packages supporting 200 to 300 pins require transmission line techniques to be considered at the die to package and package to board boundaries. At the same time, TTL clocks and data busses are now pushing into the 50 to 100 MHz range. Using the inherently unsymmetrical TTL outputs at the frequency range that was previously the domain of relatively well behaved ECL only adds to the challenges for the designer.

These challenges are similar to those faced by microwave transmission line designers for more than a decade. Fortunately, the nature of digital signals allows for some simplification of the analysis techniques. After some review of the available literature, we have found some tools that only require moderate algebraic manipulation and your scientific calculator and are sufficient for signals through the 500 MHz regime. For signals of 1 GHz and greater, the digital simplifications (uniform high and low levels, pulse duration greater than 3x the transition time, etc.) no longer apply. Here the full treatment, Smith Charts and all, is needed.

TRANSMISSION LINE DISCONTINUITIES

Any conductor having a length and effective propagation delay greater than the transition time of the signal it carries should be considered a transmission line. For a 1 nsec transition time and dielectric materials such as FRP, this length is on the order of 15 cm or 5.9 inches. The exact form is:

$$L = \frac{c \times T}{\sqrt{\epsilon_{\text{eff}}}} \quad (1)$$

Where T is the transition time, L is the length, c is 2.997 x 10⁸ m/sec and ϵ_{eff} is the dielectric permittivity of the surrounding medium.

Transmission lines are usually described in terms of their characteristic impedance, Z₀. This impedance can be described in terms of the distributed inductance and capacitance as:

$$Z_0 = \sqrt{\frac{L_d}{C_d}} \quad (2)$$

If two transmission lines of differing impedances are joined, a portion of the energy of a signal encountering the discontinuity will be reflected. The ratio of the reflected signal to the incident signal is the reflection coefficient:

$$\rho = \frac{Z_2 - Z_1}{Z_2 + Z_1} \quad (3)$$

Where Z₁ is the impedance of the incident transmission line, and Z₂ is the impedance of the second line or the load. This expression can be used directly in the time domain if the impedances are not frequency dependent. For frequency dependent impedances caused by lumped inductive or capacitive reactances, a similar expression is used in the complex frequency domain (S):

$$\rho(s) = \frac{Z_2(s) - Z_1(s)}{Z_2(s) + Z_1(s)} \quad (4)$$

DISTRIBUTED LOADING

A typical analysis problem is that of determining the loading effect of a series of capacitive loads distributed at regular intervals along a transmission line. This configuration is most frequently encountered in the form of a device output driving an address or data line to an array of memory devices.

If the arrangement of the memory devices is reasonably regular, the driven circuit can be approximated as a transmission line with additional distributed capacitance. If the load capacitances are spaced close together relative to the transition time of the signal, the resulting combined structure is again a transmission line but with a new, lower impedance, Z₃. It is in effect a delay line with reduced phase velocity and significant filtering or rise time degradation at the far end.

If we assume that the added capacitance has little effect on the distributed inductance of the line, the new impedance is:

$$Z_3 = \sqrt{\frac{L_d}{C_d + CD}} \quad (5)$$

Where CD is the distributed capacitance of the load. Equations (2) and (5) can be combined and an expression for Z3 without the inductance term can be formed as:

$$Z_3 = \frac{Z_0}{\sqrt{1 + \frac{CD}{C_d}}} \quad (6)$$

This new impedance is the one that is seen by the output of the source device. If the package trace was optimized for the assumed unloaded transmission line Z0, equation (3) can be used to analyze the mismatch at that boundary.

The propagation delay of the combined structure can be represented as:

$$tD = t_d \times \sqrt{1 + \frac{CD}{C_d}} \quad (7)$$

Where tD is the loaded time delay per unit length and t_d is the unloaded delay. This equation also suggests an experimental way of evaluating the radical in equation (6) by use of easily measured delay times.

The impedance and capacitance of the unloaded line can be derived either experimentally or analytically. Typical C_d values for representative transmission lines are:

Z ₀	C _d	w/h
50 Ohms	1.30 pF/cm,	3.3 pF/in 1.50
75 Ohms	0.83 pF/cm,	2.1 pF/in 0.75
100 Ohms	0.61 pF/cm,	1.5 pF/in 0.36

These values have been calculated assuming FR4 material with a relative permittivity, E, of 5.0. The width to thickness ratio, w/h, has been included for reference. The structure is assumed to approximate a microstrip, i.e., a trace of width w over a ground plane at separation h through the referenced board material.

If the added loads are evenly positioned and their spacing meets the rise time and prop delay criteria described above, this loaded line model is valid. The impedance of the resulting structure, and thus the load it presents to the output, can be predicted. Unfortunately, this structure is still only an approximation of a transmission line. The new "line" does not have the uniform TEM (Transverse ElectroMagnetic) propagation that is characteristic of the ideal line. The structure is a delay line and low pass filter with a cutoff frequency that decreases as the load capacitance increases.

The degradation of rise time resulting from this filter occurs even if the driving output is perfectly matched to the resulting "line" impedance. As an example, for a 50 Ohm line, a distributed load of 1.3 pF/cm (effectively doubling the unloaded distributed capacitance) limits the rise time to 1 nsec after 20 cm. By comparison, a distributed load of 10 pF/cm on a 50 Ohm line would result on a rise time of 2.4 nsec after 20 cm.

Although a precise analysis of the rise time degradation is complex, it appears that a relationship similar to that for propagation delay can be successfully used for added distributed capacitances up to 10 times the unloaded line capacitance:

$$RT = r_t \times \sqrt{1 + \frac{CD}{C_d}} \quad (8)$$

Here RT is the resulting rise time degradation per unit length of the combined structure and r_t is the rise time degradation of the unloaded line. This relationship is only approximate and appears to work best at points located four or more "load stations" down the line from the source.

LUMPED LOADING

If the spacing between the added capacitances is irregular, but still closer than a rise time propagation delay, the resulting structure will have a varying and difficult to predict impedance. This is definitely not a recommended structure for critical signal transmission.

If the propagation delay spacing of the added loads is greater than the transition times of the signal, the effective impedance of the line reverts to Z₀, the unloaded impedance, during the actual transition. Each point load capacitance is, however, a point of impedance discontinuity, and thus a source of reflection.

Since the load is capacitive, the reflections are negative, and can cause errors in any input that precedes

a large discrete load. A survey paper written by P.G. Tumms developed a useful example of a finite rise time signal encountering a discrete capacitive load.

The signal is a simple linear rising edge starting from 0 (logic low level) and reaching a stable level of E (the logic high level) at t_r , the rise time for the signal, and remaining at E after that time. This signal can be expressed as:

$$e^+(t) = (E/t_r)t u(t) - (E/t_r)(t - t_r) u(t - t_r) \quad (9)$$

The expression is the difference of two ramp functions, one starting at time 0 and the other starting at time t_r .

The reflected pulse in terms of ρ from equation (3) is:

$$e^-(t) = e^+(t) \rho \quad (10)$$

Since the discrete load is capacitive reactance, the complex frequency for ρ in equation (4) should be used. The $Z_1(s)$ is the transmission line impedance Z_0 . The load impedance $Z_2(s)$ is the parallel of the discrete load capacitive reactance, $1/Cs$, and the rest of the transmission line, Z_0 .

After appropriate algebraic manipulations, the complex reflectance is:

$$\rho(s) = \frac{-s}{s + 2/(Z_0 C)} \quad (11)$$

and the input signal transforms to:

$$E^+(s) = \frac{E}{t_r s^2} (1 - e^{-t_r s}) \quad (12)$$

If these two expressions are inserted in equation (10), simplified, and inverse transformed back to the time domain, the reflected pulse is:

$$e^-(t) = (E/a t_r) [- (1 - e^{-at}) u(t) + (1 - e^{-a(t - t_r)}) u(t - t_r)] \quad (13)$$

where (a) is defined as $2/(Z_0 C)$.

According to Tumms, the maximum amplitude of this reflected signal occurs at $t = t_r$ and is:

$$|e^-(t)|_{\max} = (E/a t_r) (1 - e^{-at_r}) \quad (14)$$

and for many applications, $at_r > 2.3$, implying that the rise time of the input signal is greater than or equal to the ZOC time constant of the line impedance and load capacitance. Under this condition, equation (14)

may be approximated as:

$$|e^-(t)|_{\max} = (E/at_r) \quad (15)$$

The duration of the reflected signal (between half amplitude points) can be derived from equation (13) as:

$$W = (1/a) \ln \frac{e^{at_r} - e^{-at_r}}{1 - e^{-at_r}} \quad (16)$$

and when $at_r > 2.3$, this reduces to:

$$W = t_r \quad (17)$$

This maximum amplitude and half-amplitude pulse width characterization is very useful in determining the signal energy available to force a logic input to the opposite state or to constructively or destructively interfere with a periodically repeating signal at the output.

Note that if the rise time to time constant condition is met, the reflected signal maximum is less than 40% of the original step amplitude. For values of at_r near 1.5, the reflected signal reaches the half logic swing value at its maximum. At the extreme, at_r values near 0.1, implying ZOC time constants 20 times the rise time, the reflected signal reaches 95% of the logic swing.

The effect of such a large pulse on the originating output would be the equivalent of a switching contention. If the output was in the TTL high state, the reflected low pulse would appear as a short to logic low through impedance Z_0 for a duration of W.

Tumms continues the analysis to develop the transmitted signal to additional loads and inputs further down the line. The transmitted signal is the sum of the incident and reflected signals. The form is:

$$e(t)_T = e^+(t) + e^-(t) \quad (18)$$

The resulting time domain expression, in spite of its complexity, can be seen to be the linear combination of equations (9) and (13):

$$e(t)_T = (E/a t_r) \{ [at + (e^{-at} - 1)] u(t) + [-1 + a(t - t_r) e^{-a(t - t_r)}] u(t - t_r) \} \quad (19)$$

which indicates for $0 < t < t_r$:

$$e(t)_T = (E/a t_r) [at + (e^{-at} - 1)] \quad (20)$$

and for $t > t_r$:

$$e(t)_T = (E/a t_r) [at_r + e^{-at} (1 - e^{+at_r})] \quad (21)$$

These equations can be used to develop simpler ex-

pressions for the rise time and delay of the transmitted signal. In the extreme case of the time constant much larger than the rise time, the input signal approaches a step function and the added delay to the half logic swing level would be:

$$\Delta t = 0.693 / a \quad (22)$$

and the rise time from 10% to 90% logic swing of the transmitted signal would be:

$$t_R = 2.2 / a \quad (23)$$

In actual practice, the input rise times can be comparable to or greater than the load time constant. If the input signal rise time is more than four times the load time constant, equation (20) gives:

$$t_{RO} / 2 = t_r / 2 + 1 / a \quad (24)$$

where $t_{ro} / 2$ is the time required for the output signal to reach half swing. The delay due to the discrete load is thus:

$$\Delta t = t_{RO} / 2 - t_r / 2 \quad (25a)$$

$$\Delta t = 1 / a \quad (25b)$$

Although equation (19) indicates that the output wave form is actually a summation of exponentials, the simplifications of digital logic can come to our rescue. If we approximate the output as a ramp which has the same half amplitude rise time as the pulse described by equation (19), the rise time of the proposed output ramp function would be:

$$t_{ro} = 2 (t_{ro} / 2) \quad (26a)$$

$$\text{or } t_{ro} = t_r + (2 / a) \quad (26b)$$

We now have a simple tool that can approximate the delay and rise time degradation effects of the successive discrete loads in terms of the arriving signal rise time and the ZOC time constant of the load.

Note that this technique can be used in the package to circuit board interface to account for transitional parasitics of the package pin.

As an example of the use of this distributive load equivalent impedance technique, we will examine a design problem of specifying, matching, and terminating a TTL output. The TTL signal is driving the address line of an array of memory devices.

The specified input capacitance of the memories is 10 pF and they are distributed at 2 inch intervals on the circuit board. The ASIC macro library specifies the capacitive drive capability of the TTL output macro as a function of frequency.

For typical circuit board material and line widths, the 2 inch (5 cm) spacing represents a time delay of 300 to 400 psec. Since this is significantly less than the rise/fall times of a TTL output, the reduced impedance delay line model is the appropriate one to use.

If the unloaded trace is a 100 Ohm line ($w/h = 0.36$), the capacitance per unit length, C_d , is 0.61 pF/cm. The added capacitance of 10 pF every 2 inches or 5 cm gives an effective CD value of 2 pF/cm. If we insert these values in equation (6):

$$Z_3 = \frac{100 \text{ Ohms}}{\sqrt{1 + \frac{2 \text{ pF/cm}}{0.61 \text{ pF/cm}}}} \quad (27)$$

$$= 100 / 2.07 = 48 \text{ Ohms}$$

This is the effective impedance of the combined delay line structure. Additionally, the original nominal propagation delay of 350 psec/5 cm or 70 psec/cm is now 145 psec/cm or 725 psec/5 cm.

Since the drive capability of the output macro is given as capacitive load as a function of frequency, the effective impedance should be considered as an equivalent capacitive reactance at a specified frequency. If a 100 nsec period for the address line is assumed, the effective frequency is on the order of 10 MHz. For this frequency, the equivalent capacitive load is:

$$C = \frac{1}{2 \text{ pf} \times f_c} \quad (28)$$

$$= 1 / (2 * 3.1459 * 10 \text{ MHz} * 48 \text{ Ohms})$$

$$= 330 \text{ pF}$$

As a comparison, if the frequency of operation were 30 MHz, the effective load capacitance would be:

$$C = 1 / (2 * 3.1459 * 30 \text{ MHz} * 48 \text{ Ohms}) \quad (29)$$

$$= 110 \text{ pF}$$

If the spacing of the 10 pF capacitors is increased to 10 cm, the resulting impedance is 61 Ohms. At 10 MHz the effective capacitance drops to 261 pF.

If the distance to the first added capacitive load is increased such that the round-trip delay is greater than the rise time of the signal, the model is one of two sections of transmission line, the first of unloaded impedance (100 Ohms), and the second of loaded impedance (48 Ohms). The first section presents a load on the TTL output of:

$$C = 1 / (2 * 3.1459 * 10 \text{ MHz} * 100 \text{ Ohms}) \\ = 160 \text{ pF} \quad (30)$$

For these impedances, the reflected signal from the discontinuity is approximately 35%. If the distance just meets the rise time criteria ($2 \times T_{pd} = 3 \text{ nsec}$), then the reflected signal represents an additional load component phase shifted by approximately 10 degrees. This phase shift slightly decreases the additional loading effect to 34%.

As the distance (and phase shift) increases, the additional loading effect will drop off until there is actu-

ally an increase in the effective impedance at 180 degrees (and at 360 degree multiples thereafter). This area of operation for TTL outputs begins at approximately 9 inches of line length before the added loads.

The 180 degree shift point at 10 MHz operation would require over 160 inches (13 feet) of line length, so the cancellation effects (not to mention the multiple resonance points) are not likely to be observed in a practical system application.

For TTL outputs and moderate frequencies this distributed load equivalent impedance method is reasonably accurate. This procedure allows the use to determine whether a desired load configuration complies with capacitive load limits established to assure signal integrity or device reliability. While they do give some idea of resultant rise time degradation, a detailed analysis for wave shape requires simulation techniques such as SPICE™.

THERMAL MANAGEMENT

Thermal management is the orderly design approach to removing the excess heat generated in high performance logic circuits. For AMCC's datacom and telecom devices, thermal management includes power optimization of the design of the device, selection of the appropriate package for the device, identification of added heatsinks if required, and identification of the appropriate airflow needed. While the first two techniques are under the control of the device designer, the last two involve both the device designer and the board and system designer.

AMCC devices range in power dissipation levels from less than 1 watt to greater than 5 watts. For the lowest power devices conduction cooling via the package leads into the printed circuit board is sufficient. Modern multi-layer boards form an effective large area radiator for the excess heat. The table indicates that this is the case for devices through the 1.5 watt level. For devices greater than 2 watts, some combination of moving air and/or heatsink must be considered.

SYSTEM APPLICATIONS ISSUES

The trend toward small outline surface mount devices and small daughterboard approaches to net interface modules may place limitations on circuit board conduction as a thermal management technique. Similarly, the smaller geometries of these module designs may also reduce the volume available for heatsinks and the effectiveness of moving air.

The Thermal Management Table describes the various AMCC networking devices, intrinsic package thermal impedance (Θ_{jc}) from junction to case, the still air thermal impedance (Θ_{ja}) from junction to ambient (including the effect of any attached heatsink), the total internal power dissipation (worst case), and the recommended ambient temperature/airflows required for specified operation. This table should give the reader a good idea of the feasibility of a specific thermal environment. For a detailed final design please consult your AMCC representative for specific airflow vs. thermal impedance curves and other heatsink options.

Table 1.

Device	Package	Θ_{jc}	Θ_{ja} Still Air	Power	Max Still Air ¹	Air/70°C ² (min)	Air/85°C ³ (min)	Air/70°C for 100°C T _J (min)
S3011A	80 HPQFP	n/a	40°C/W	1.1 W	85°C	n/a	n/a	n/a
S3012A	80 HPQFP	n/a	40°C/W	1.6 W	75°C	n/a	100 LFPM	n/a
S3005A	68 LDCC	2.5°C/W	34°C/W	2.4 W	49°C	200 LFPM	500 LFPM	750 LFPM
	w/ 45-20 HS		264°C/W	2.4 W	66°C	<50 LFPM	150 LFPM	200 LFPM
S3005D	80 TEP	2.0°C/W	30°C/W	2.4 W	58°C	200 LFPM	700 LFPM	(not recmd)
	w/ 45-28 HS		23°C/W	2.4 W	75°C	n/a	200 LFPM	300 LFPM
S3006A	68 LDCC	2.5°C/W	34°C/W	2.6 W	42°C	310 LFPM	600 LFPM	900 LFPM
	w/ 45-20HS		28°C/W	2.6 W	61°C	100 LFPM	150 LFPM	250 LFPM
S3006D	80 TEP	2.0°C/W	30°C/W	2.6 W	52°C	300 LFPM	750 LFPM	(not recmd)
	w/ 45-28 HS		23°C/W	2.6 W	70°C	n/a	250 LFPM	400 LFPM

1. Max ambient temperature permitted in still air to maintain T_J <130°C

2. Airflow required in 70°C ambient conditions to maintain T_J <130°C

3. Airflow required in 85°C ambient conditions to maintain T_J <130°C

Table 1. (continued)

Device	Package	θ_{jc}	θ_{ja} Still Air	Power	Max Still Air ¹	Air/70°C ² (min)	Air/85°C ³ (min)	Air/70°C for 100°C TJ (min)
S3014D	44 TEP	1.8°C/W	28°C/W	1.2 W	85°C	n/a	n/a	n/a
S3017A	52 TEP	2.2°C/W ⁴	40°C/W ⁴	1.3 W	80°C	n/a	n/a	n/a
S3018A	52 TEP	2.2°C/W ⁴	40°C/W ⁴	1.6 W	70°C	n/a	n/a	n/a
S3015A	52 TEP	2.2°C/W ⁴	40°C/W ⁴	1.2 W	80°C	n/a	n/a	n/a
S3016A	52 TEP	2.2°C/W ⁴	40°C/W ⁴	1.4 W	75°C	n/a	n/a	n/a
S2016A	120 TEP	1.0°C/W	20°C/W	5.8 W	14°C	600 LFPM	n/a	n/a
	w/ 45-10 HS		18°C/W	5.8 W	25°C	150 LFPM	250 LFPM	600 LFPM

1. Max ambient temperature permitted in still air to maintain TJ <130°C

2. Airflow required in 70°C ambient conditions to maintain TJ <130°C

3. Airflow required in 85°C ambient conditions to maintain TJ <130°C

4. Preliminary Package Thermal Impedance value.

GENERAL DESCRIPTION

This application note gives recommendations and examples of how to connect the S3015/16 chipset to the supporting circuitry in a coaxial cable application. Included in these recommendations are the connections to the controller, line interface unit, and the monitor transformer. The S3015 provides the major components on-chip for the CMI encoder and clock synthesis functions. The S3016 provides clock recovery and CMI decoder functions.

In order to guarantee compliance to the G.703 specification for output waveform integrity and input sensitivity, the line interface unit must be correctly specified and routed. In addition, the noise levels of the critical circuits must be minimized through the use of power supply decoupling at specific frequencies. The combination of correct component selection, layout and decoupling should result in a highly integrated solution for the front end of E4 or STS-3 CMI interfaces.

SYSTEMS INTERFACE

The system interface block diagram is shown in Figure 1. The description of each of the blocks is as follows:

(For pins not listed, refer to the appropriate vendor data sheet.)

Controller: This block contains the protocol circuitry for the interface. The inputs from the S3016 are serial 155 Mbps/sec clock and data and the loss of signal indication. The outputs to the S3015 are the serial 155 Mbps/sec NRZ data stream.

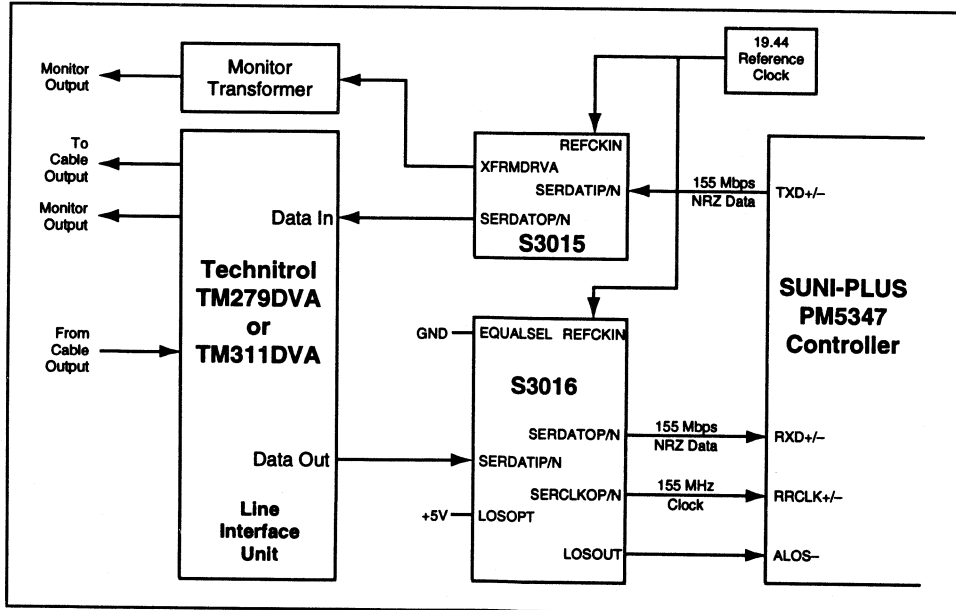
Reference Clock: This is the backup reference clock for both the S3015 and the S3016. It is not used except at power up and when data is not present.

Line Interface Unit: The line interface unit contains all of the required circuitry to both transmit and receive over the coaxial cable interface.

The receive interface consists of a transformer followed by the termination network, the line equalizer, and the bandpass filter. The output data from the line interface unit is differential PECL levels.

The transmit interface consists of a differential PECL input followed by a line conditioning circuit and a transformer.

Figure 1.



PHYSICAL LAYER INTERFACE SCHEMATICS:

Figure 2 shows a schematic of the components required to implement the transformer driver circuit for the monitor interface. This output is used for test purposes.

COMPONENT SELECTION:

Controller devices:

The S3015/16 chipset is compatible with any controller device that supports a 139 or 155 Mbit/sec serial interface. AMCC currently recommends the use of the PMC-Sierra PM5437 SUNI-PLUS device.

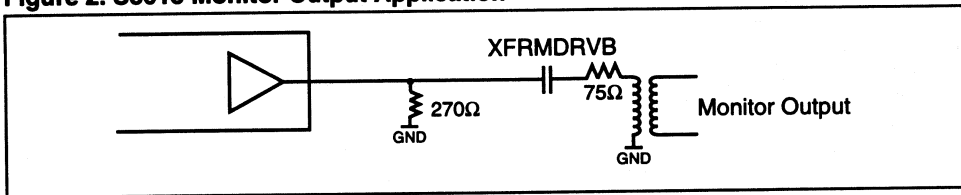
Line Interface Unit:

AMCC recommends the use of the Technitrol part #TM279DVA for E4 applications and Part #TM311DVA for STS-3 CMI applications.

This part meets the critical requirements for insertion loss and frequency response.

Figures 3 and 4 show the recommended decoupling and layout considerations to follow when using the S3015/16 parts.

Figure 2. S3015 Monitor Output Application



E4/STM-1/OC-3/ATM S3015/S3016 Examples

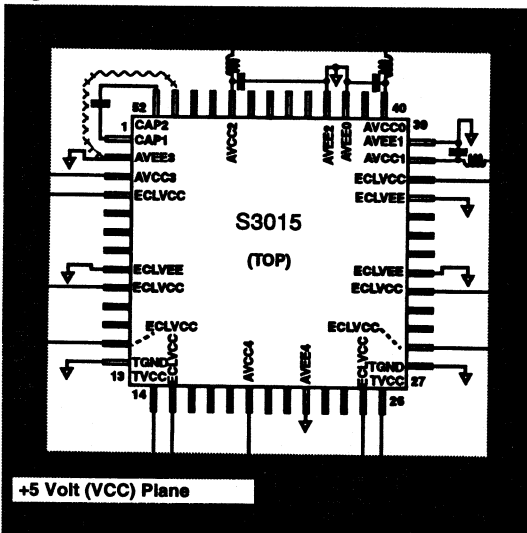
The S3015 and S3016 have similar power pin footprints. The CAP1/CAP2 capacitor should be 0.01 μ F for the S3015. For the S3016, the CAP1/CAP2 capacitor should be 0.1 μ F. Figure 3 illustrates the connections for the S3015 transmitter device and Figure 4 for the S3016 receiver device. In addition, please note that AVEE4, AVEE5, AVCC4, and AVCC5 are not connected on the S3016. The ring should be completed under the device connecting pins 51 and 2. Please note that pin 2 should be directly connected to the ground plane to avoid current through the ground ring.

High Freq/Low Freq Decoupling

Capacitors shown in the drawing should be paralleled 100pf/0.1 μ f ceramic chip capacitors for broad-band decoupling. X7R or BX dielectric is acceptable.

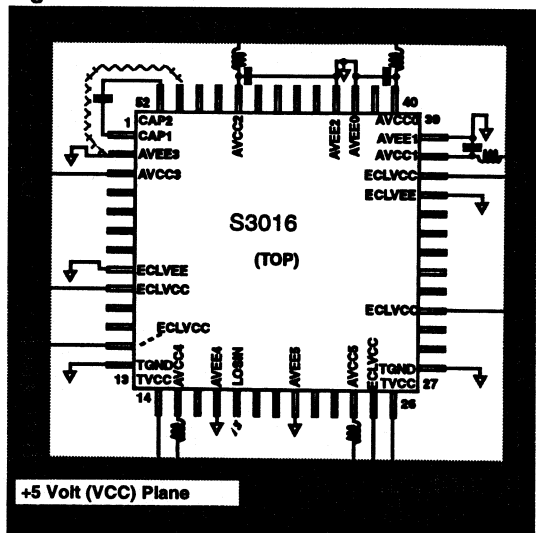
These decoupling networks are in addition to the decoupling of the Digital power pins required in good design practice, ie; 0.01 to 0.1 μ f per core or I/O power pin and 1 μ f/watt of low frequency within 1 cm of the device.

Figure 3.



↓ = Connection to Ground Plane

Figure 4.



↓ = Connection to Ground Plane

↘ = Ground for Digital Interface, LOSIN for Analog Interface

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The design of high speed TTL/CMOS systems is often made more challenging and more difficult than their ECL and GaAs counterparts due to the poor transmission line behavior of the TTL device inputs. Since inputs from either TTL or CMOS devices provide essentially no termination to a given signal path (transmission line), reflections at the end of the line are a certainty. Nowhere in a system is this more noticeable and disastrous than when it occurs on the system's clock. It is here that the wrong choice for the clock driver can cripple the chance for success of a design.

There are many contradictions imposed on the "ideal" TTL clock driver. For example, slower edge rates reduce undershoot, ringing and plateau effects at the expense of duty cycle, frequency and clock skew; while faster edge rates cause overshoot, noise injection, and greater EMI radiation while trying to improve frequency, duty cycle and clock skew.

AMCC has solved this dilemma with an output driver circuit that is best described as having two modes for controlling the clock edges. This patented method produces a fast, crisp edge during the transition phase of the output waveform and then immediately slows the edge and becomes a closer match to the impedance of the external PC board. Figure 1 shows the representative effect of the "dual slope" on the falling edge of the clock. The output driver actually uses the reflected wave to determine the appropriate inflection point for the slope and virtually eliminates "ground bounce".

Figure 1. "Dual Sloped" Output Driver Eliminates "Ground Bounce"

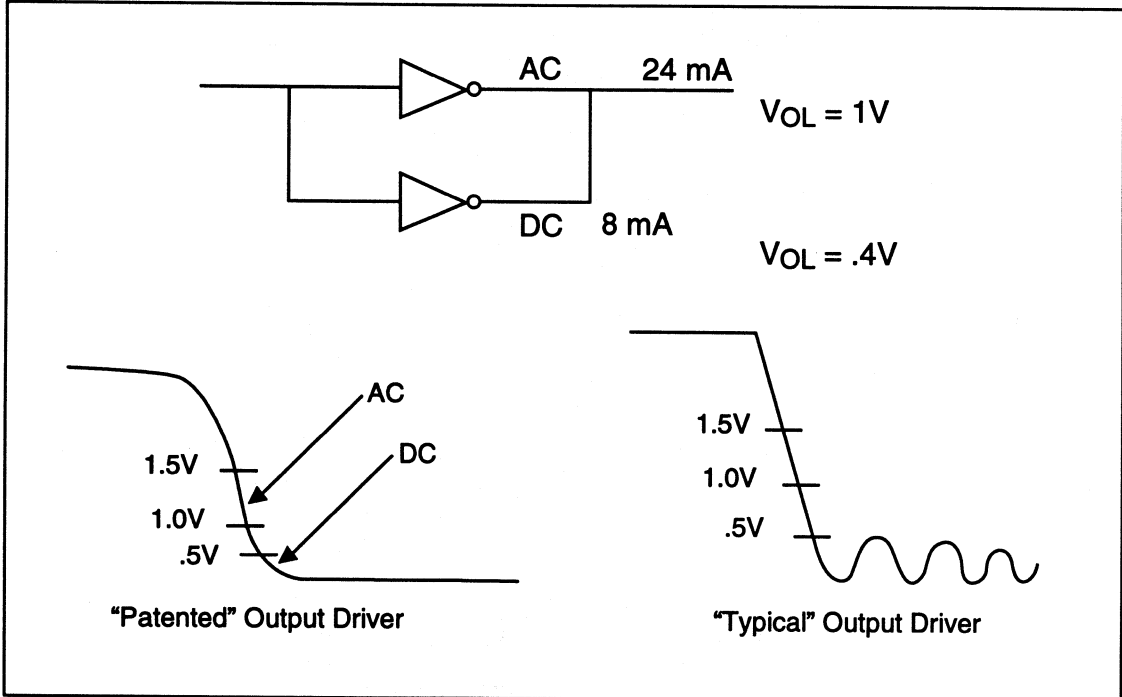


Figure 2 shows the representative effect of dynamically adjusting source series termination on the rising edge. By adjusting the built-in termination to individual loading environments, AMCC's clock drivers prevent "ringing" without the use of any additional onboard termination.

Figure 3 shows an unterminated 66MHz output of an SC35XX Series Driver. Conventional TTL output stages, with or without serial termination resistors, cannot attain both the **edge rates** and the **impedance matching** qualities achieved with the AMCC method.

Figure 2. Built-in, On-Chip Source (Series) Termination Minimizes "Overshoot"

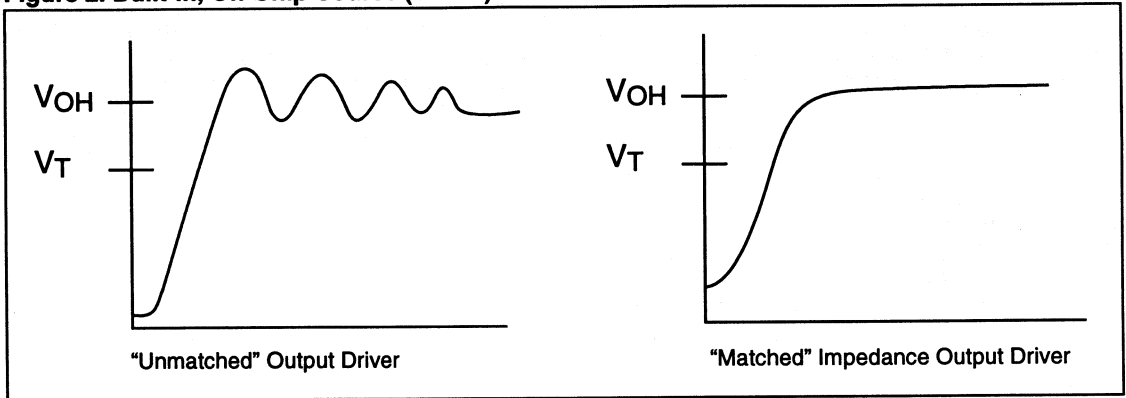
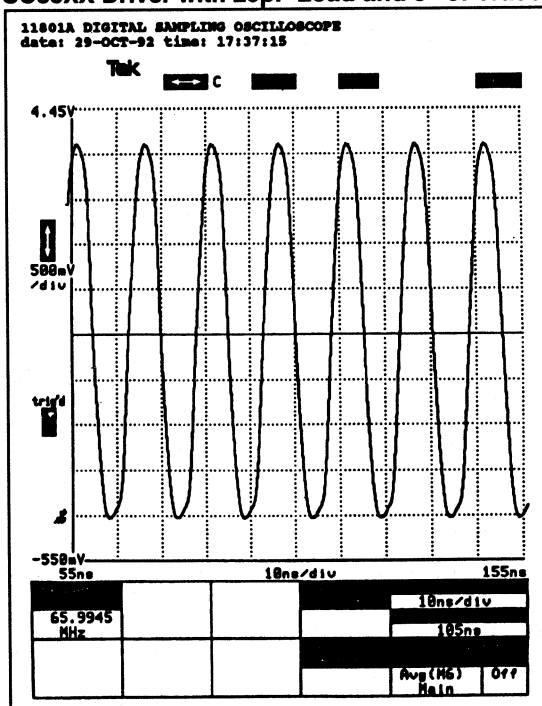


Figure 3. SC35XX Driver with 20pF Load and 8" of Trace



FEATURES

- **20 clock outputs:**
 - Ten outputs at primary frequency, up to 80 MHz
 - Five outputs at primary or 1/2 primary frequency
 - Five outputs at either 1/2 or 1/4 primary frequency
- **Leading edge skew for all outputs ≤ 0.5 ns**
- **Proprietary output drivers with:**
 - Complementary 24 mA peak outputs, source and sink
 - 50-75 Ω source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

- **Datacom and Telecom networks**
- **Compatible with Intel's Pentium™ processor**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**

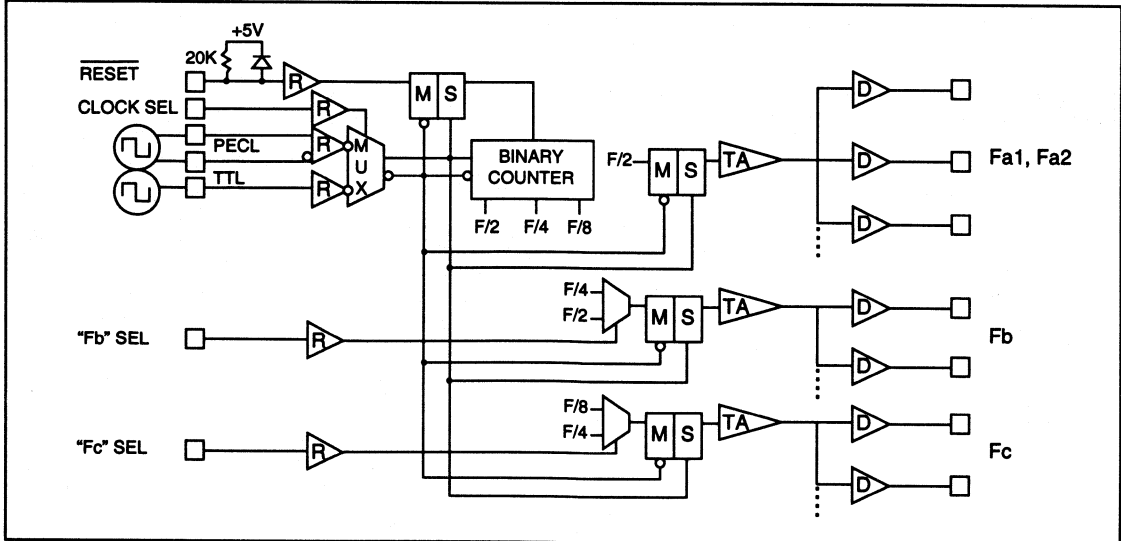
GENERAL DESCRIPTION

The SC3500 is a precision clock fan out driver. It requires a 2X frequency clock input from either a single-ended TTL or an ECL differential source operating between +5V and ground (PECL). This 2X reference frequency input is received and distributed to symmetrical, divide-by-two master-slave flip-flops. The resultant output is distributed to the clock output drivers.

The 20 clock outputs are divided into three groups. The first group of ten outputs are unconditionally at the primary frequency, "Fa1" and "Fa2" = F input/2. The second group of five outputs, "Fb", can be selected to be either identical to or at 1/2 the frequency of the "Fa" outputs. The third group of five outputs, "Fc", must be selected to be at either 1/2 or 1/4 of the "Fa" outputs.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output switching noise and distortion.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

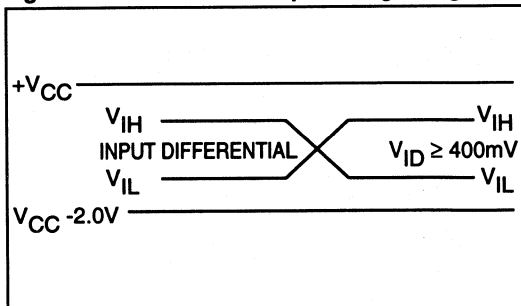
Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	Reset	V _{IN} = 2.4V		-200	µA
	TTL, CSEL, BSEL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	µA
	CLKSEL	V _{IN} = 0.4V		50	µA
	Reset	V _{IN} = 0.5V		-325	µA
	TTL, CSEL, BSEL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 80MHz max C _L = 10pF	2.4		V
V _{OL}	Output LOW Voltage	F _{OUT} = 80MHz max C _L = 10pF		0.6	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{IOLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 4 @ 70°C, Typ Pwr 370 mW		600	mW

1. Maximum test duration, one second.
2. The SC3500 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The SC3500 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic “high drive, totem pole outputs” and AMCC’s dynamically adjusting source series terminated outputs. As a result of this, the SC3500 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -8mA	2.4V	
V _{OL}	I _{OL} = 4mA		0.6V

Table 2. AC Specifications—Using Figure 4, AC Test/Evaluation Circuit

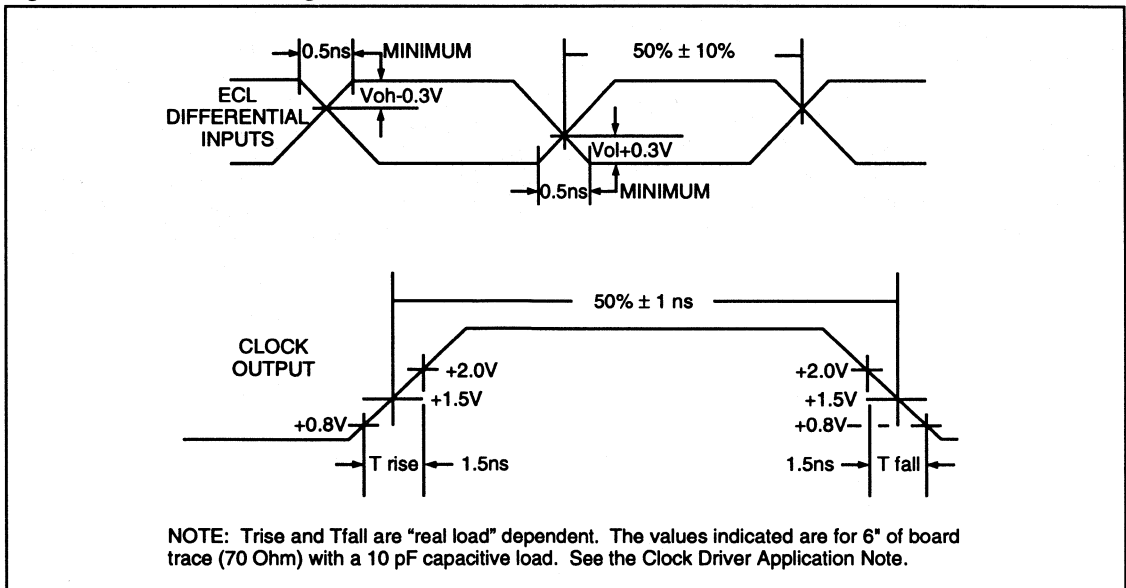
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10pF$

Parameter	SC3500-1	SC3500	Units
Maximum Skew Across All Outputs	0.5	1.0	ns
Maximum Skew Across Fa1 Outputs	0.25	0.25	ns
Maximum Skew Across Fa2 Outputs	0.25	0.25	ns
Maximum Skew Across Fb Outputs	0.25	0.25	ns
Maximum Skew Across Fc Outputs	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry	± 1.0	± 1.0	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum PECL Differential Input Frequency	160	160	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be effected by voltage, temperature, and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50 ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pf capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
5. Parameters guaranteed by design and characterization.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION
(Refer to Logic Diagram)

AMCC has developed a single-chip clock shape and 20-output fan-out device using AMCC's advanced BiCMOS process. This design has been optimized for clock symmetry and absolute minimum skew across all twenty outputs. Three harmonic clock frequency groups are provided that are user selectable.

For highest performance this approach requires a 2X clock source input from a crystal-controlled oscillator (XCO) located adjacent to this clock driver. This oscillator, operating between +5V and ground, can provide either differential ECL inputs (referenced to +5V, PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This 2X input clock will be fanned out to a divide-down counter and to master-slave flip-flops for synchronization (refer to Figure 1, Logic Diagram). Using this methodology the output duty cycle asymmetry becomes largely a function of output driver slew rate into the AC load.

Two user-select pins, "B select" and "C select", provide the "Fb" and "Fc" output (sub-harmonic) frequencies by way of multiplexor selection into the final resynchronizing flip-flops. The divide-down counter outputs are 50% duty cycle decoded. The output resynchronizing flip-flops are keyed for leading edge alignment. These outputs are amplified to fan out to AMCC's complementary source-terminated TTL output drivers.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor ($4.7\mu\text{F} = \sim 100\text{ ms}$) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the

clock outputs becoming active. At the onset of RESET (low) the outputs will go low following five falling edge clock inputs. At the expiration of RESET (high) outputs will resume, after five falling edge clock inputs, from a high (leading edge) count origin (see Figure 5, Reset To Output Timing in the Clock Driver Application Note).

The output drivers are rise and fall slew rate controlled to $\sim 1.5\text{V/ns}$ to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination ($\sim 40\text{ Ohms}$) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance ($>25\text{pF}$ with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes ($>3.5\text{ Volts}$), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current.

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance +V_{CC} and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3500 will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

Table 3. Output Clock Frequency Selection

"B" SEL	"C" SEL	XCO FREQ	Fa	Fb	Fc
LO	LO	F	F/2	F/4	F/8
HI	LO	F	F/2	F/2	F/8
LO	HI	F	F/2	F/4	F/4
HI	HI	F	F/2	F/2	F/4

Note: XCO is the input frequency for either the PECL inputs or the TTL input. Non-crystal oscillator sources may be used at the user's discretion. See Application Note #1.

Power Management

The overall goal of managing the power dissipated by the SC3500 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3500 is determined by the load that each output drives and the frequency that each output is running. Table 4 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The output power must be added to the core power (600 mW) of the SC3500 to determine the total power being dissipated by the SC3500. This total power is then multiplied by the SC3500's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3500. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3500 is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3500 with 8 Fa outputs driving 10 pF loads at 66 MHz, 3 Fb outputs driving 5 pF loads at 33 MHz and 2 Fc outputs driving 15 pF loads at 33 MHz. Total chip power is calculated as follows:

Core Power	=	600 mW
8 Fa, 10 pF, 66 MHz = (8 x 47 mW)	=	376 mW
2 Fa, no load, 66 MHz = (2 x 16 mW)	=	32 mW
3 Fb, 5 pF, 33 MHz = (3 x 19 mW)	=	57 mW
2 Fb, no load, 33 MHz = (2 x 12 mW)	=	24 mW
2 Fc, 15 pF, 33 MHz = (2 x 24 mW)	=	48 mW
3 Fc, no load, 33 MHz = (3 x 12 mW)	=	36 mW
Total Power	=	1173 mW

The design specifies a 70°C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2°C/watt. The SC3500's junction temperature would then be:

$$70^{\circ}\text{C} + (1.173 \text{ watts} \times 46.2^{\circ}\text{C/watt}) = 124^{\circ}\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 4. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

Figure 4. AC Test/Evaluation Circuit

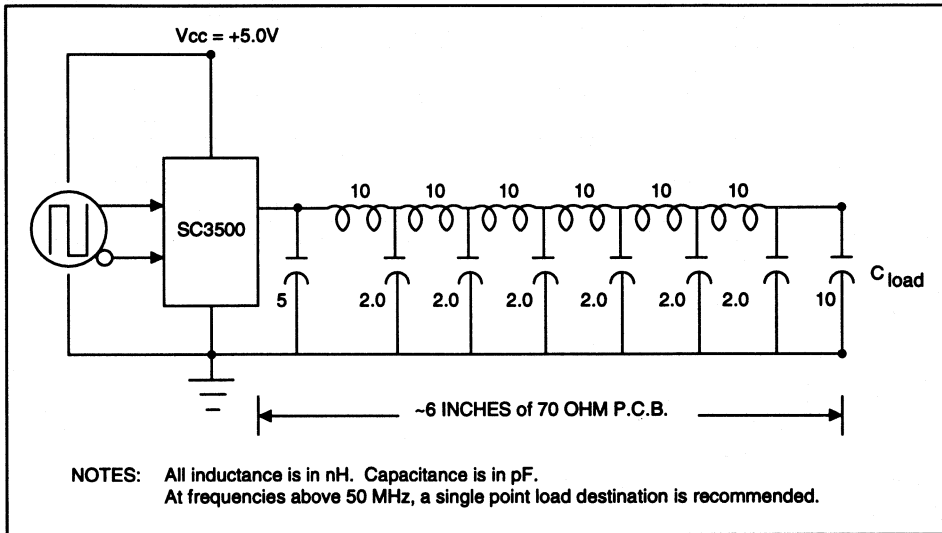


Figure 5. Relative Output Timing

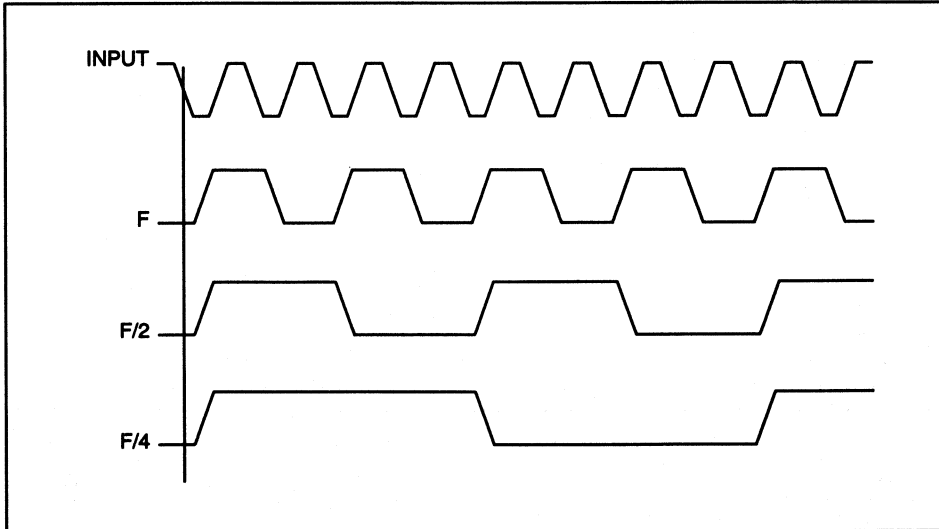
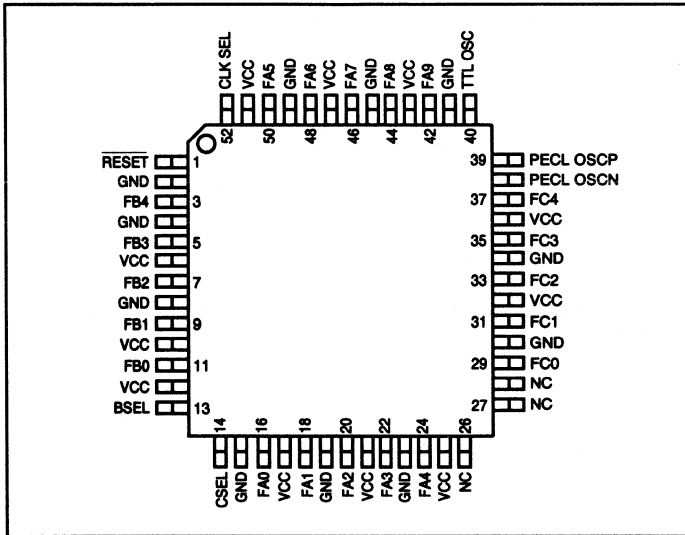


Figure 6. SC3500 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (If applicable)**
- **Optional Shipping Configuration**

SC3500

Q

-1

/TD

Optional Shipping Configuration

Blank = 84-unit matrix tray

/D = dry pack

/TD = tape, reel and dry pack

Skew Option

Blank = 1.0 ns output-output skew

- 1 = 500 ps output-output skew

Package Option

Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: SC3500Q-1/D

52-pin PQFP package, 500 ps output-output skew,
shipped dry packed in the standard matrix tray.

FEATURES

- **20 clock outputs:**
 - Ten outputs at primary frequency, up to 80 MHz
 - Ten outputs at 1/2 primary frequency
- **Leading edge skew for all outputs ≤ 0.5 ns**
- **Proprietary output drivers with:**
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 Ω source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

- **Datacom and Telecom networks**
- **Compatible with Intel's Pentium™ processor**
- **PCI Bus clock distribution**
- **Workstation and server systems with clock fanout**

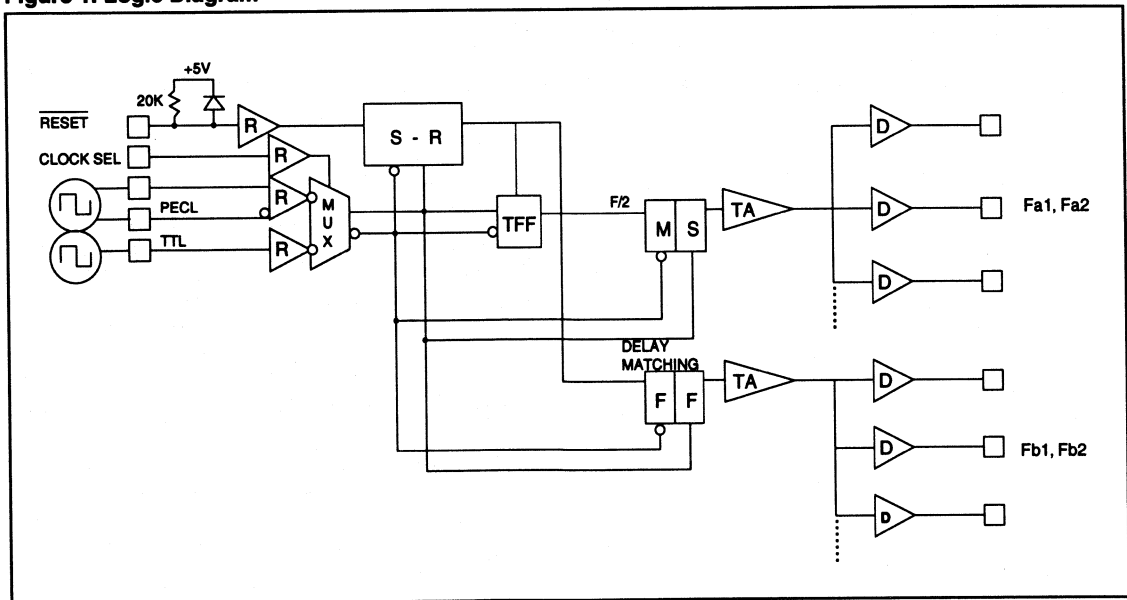
GENERAL DESCRIPTION

The SC3506 is a precision low skew clock driver with 20 outputs. It employs a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to symmetrical, divide-by-two master-slave flip-flops. The resultant output is distributed to the clock output drivers.

The 20 outputs are divided into two groups: Group Fb is at the primary frequency, equal to the input; group Fa is at one half of the primary input frequency.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise and distortion.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

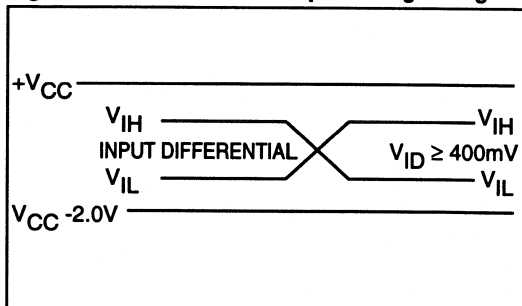
Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source-PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source-PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	Reset	V _{IN} = 2.4V		-200	µA
	TTL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	µA
	CLKSEL	V _{IN} = 0.4V		25	µA
	Reset	V _{IN} = 0.5V		-325	µA
	TTL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 80MHz max C _L = 10pF	2.4		V
V _{OL}	Output LOW Voltage	F _{OUT} = 80MHz max C _L = 10pF		0.6	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3 @ 70°C, Typ Pwr 350 mW		550	mW

1. Maximum test duration, one second.
2. The SC3506 features source series termination of approximately 40 Ohms to assist in matching 50-75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The SC3506 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3506 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -8mA	2.4V	
V _{OL}	I _{OL} = 4mA		0.6V

Table 2. AC Specifications — Using Figure 4, AC Test/Evaluation Circuit

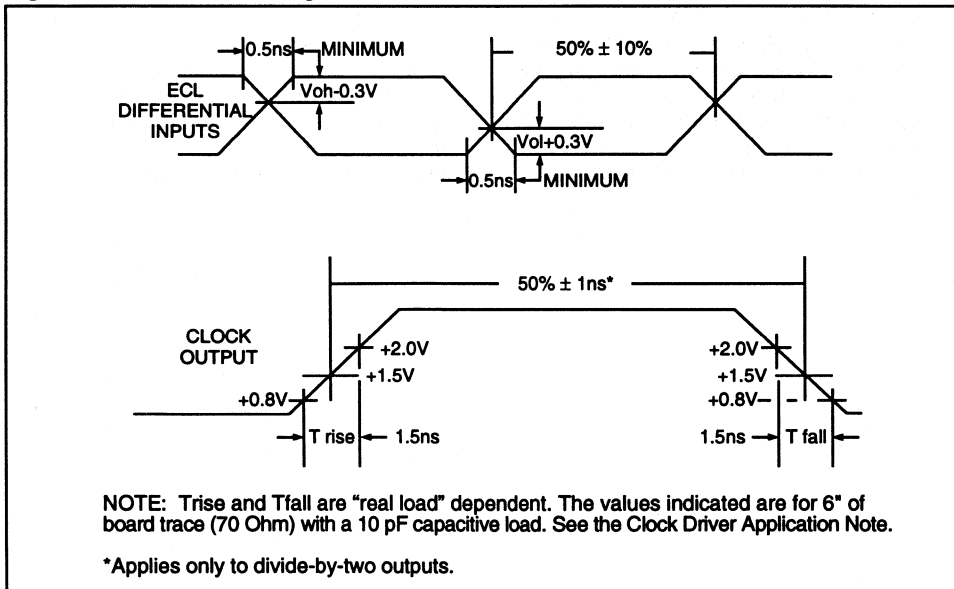
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10pF$

Parameter	SC3506-2	SC3506-1	SC3506	Units
Maximum Skew Across All Outputs	0.5	0.5	1.0	ns
Maximum Skew Chip to Chip	1.0	—	—	ns
Maximum Skew Across Fa1 Outputs	0.25	0.25	0.25	ns
Maximum Skew Across Fa2 Outputs	0.25	0.25	0.25	ns
Maximum Skew Across Fb1 Outputs	0.25	0.25	0.25	ns
Maximum Skew Across Fb2 Outputs	0.25	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry	± 1.0	± 1.0	± 1.0	ns
Maximum TTL Input Frequency	80	80	80	MHz
Maximum PECL Differential Input Frequency	80	80	80	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Chip-to-chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 0.5 ns/V and 10 ps/ $^\circ C$. Chip-to-chip skew tested at 70 $^\circ C$.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
6. Parameters guaranteed by design and characterization.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION

(Refer to Logic Diagram)

AMCC has developed a single-chip, twenty-output fanout device using AMCC's advanced BiCMOS process. This design has been optimized for clock symmetry and absolute minimum skew across all twenty outputs. Two harmonic clock frequency groups are provided.

For highest performance this approach requires a clock source input from a crystal controlled oscillator (XCO) located adjacent to this clock driver. This oscillator can provide either differential ECL inputs (referenced to +5V, PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to a toggle flip-flop and to output flip-flops for synchronization (refer to Figure 1, Logic Diagram). Using this methodology, the output duty cycle for the F/2 or Fa group becomes largely a function of output driver slew rate into the AC load.

The Fb group duty cycle is governed by the input source clock. The output flip-flops are reset keyed for leading edge alignment. These outputs are amplified to fan out to AMCC's complementary source terminated TTL output drivers.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor ($4.7\mu\text{F} = \sim 100\text{ ms}$) is connected between this pin and ground, the device will respond with a "power up reset" — a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling-edge clock inputs. At the expiration of RESET

(high) the outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin (see Figure 5, Reset to Output Timing in the Clock Driver Application Note).

The output drivers are rise and fall slew rate controlled to $\sim 1.5\text{V/ns}$ to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination ($\sim 40\text{ Ohms}$) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance ($>25\text{pF}$ with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes ($>3.5\text{ Volts}$), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 24 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3506 will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

Power Management

The overall goal of managing the power dissipated by the SC3506 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3506 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The output power must be added to the core power (550 mW) of the SC3506 to determine the total power being dissipated by the SC3506. This total power is then multiplied by the SC3506's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3506. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3506 is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3506 with 8 Fb outputs driving 10 pF loads at 66 MHz, 3 Fa outputs driving 5 pF loads at 33 MHz and 2 Fa outputs driving 15 pF loads at 33 Mhz. Total chip power is calculated as follows:

Core Power	= 550 mW
8 Fb, 10 pF, 66 MHz = (8 x 47 mW)	= 376 mW
2 Fb, no load, 66 MHz = (2 x 16 mW)	= 32 mW
3 Fa1, 5 pF, 33 MHz = (3 x 19 mW)	= 57 mW
2 Fa1, no load, 33 MHz = (2 x 12 mW)	= 24 mW
2 Fa2, 15 pF, 33 MHz = (2 x 24 mW)	= 48 mW
3 Fa2, no load, 33 MHz = (3 x 12 mW)	= 36 mW
Total Power	= 1123mW

The design specifies a 70°C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the θ_{ja} for still air is 46.2°C/watt. The SC3506's junction temperature would then be:

$$70^{\circ}\text{C} + (1.123 \text{ watts} \times 46.2^{\circ}\text{C/watt}) = 122^{\circ}\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

Figure 4. AC Test/Evaluation Circuit

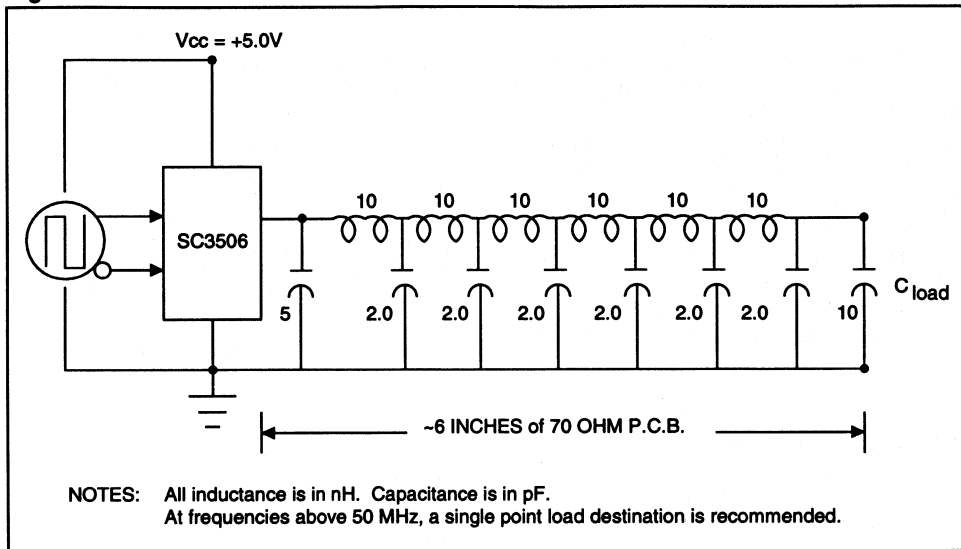


Figure 5. Relative Output Timing

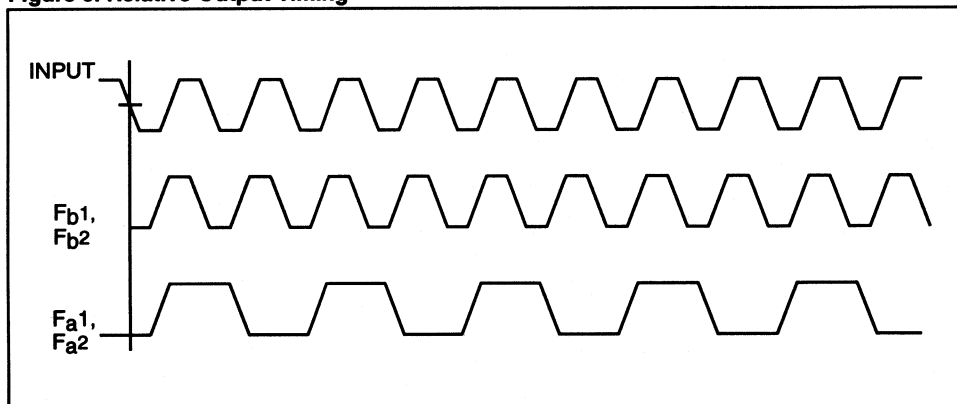
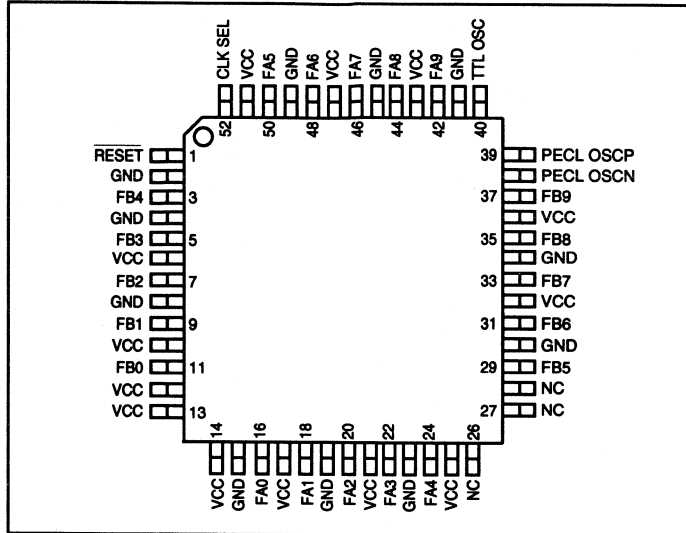


Figure 6. SC3506 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC3506

Q

- 1

/TD

Optional Shipping Configuration

Blank = 84-unit matrix tray
 /D = dry pack
 /TD = tape, reel and dry pack

Skew Option

Blank = 1.0 ns output-output skew
 - 1 = 500 ps output-output skew

Package Option

Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: SC3506Q-1/D

52-pin PQFP package, 500 ps output-output skew, shipped dry packed in the standard matrix tray.

FEATURES

- **20 clock outputs:**
 - Ten outputs at primary frequency, up to 80 MHz
 - Ten outputs at primary or 1/2 primary frequency, in two groups of five outputs
- **Leading edge skew for all outputs ≤ 0.5 ns**
- **Proprietary output drivers with:**
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

- **Datacom and Telecom networks**
- **Compatible with Intel's Pentium™ processor**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**

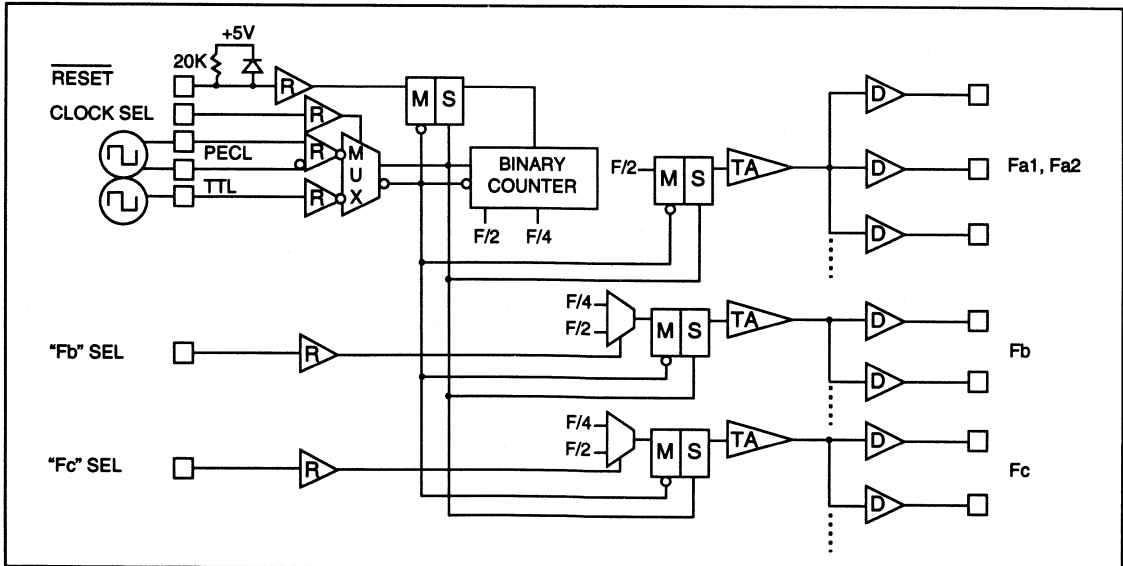
GENERAL DESCRIPTION

The SC3507 is a precision low skew driver with 20 outputs. It requires a 2X frequency clock input from either a single-ended TTL or an ECL differential source operating between +5V and ground (PECL). This 2X reference frequency input is received and distributed to symmetrical, divide-by-two master-slave flip-flops. The resultant output is distributed to the clock output drivers.

The 20 clock outputs are divided into three groups. The first group of ten outputs are unconditionally at the primary frequency, "Fa1" and "Fa2" = F input/2. The second group of five outputs, "Fb", can be selected to be either identical to or at 1/2 the frequency of the "Fa" outputs. Similarly, the third group of five outputs, "Fc", can be selected to be at either equal to or 1/2 of the "Fa" outputs.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise and distortion.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

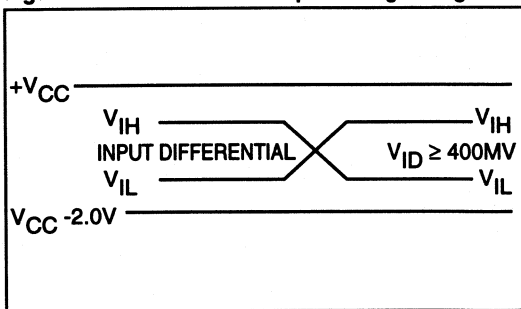
Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source-PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source-PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	uA
	CLKSEL	V _{IN} = V _{CC} (max)		350	uA
	RESET	V _{IN} = 2.4V		-200	uA
	TTL, CSEL, BSEL	V _{IN} = 2.4V		15	uA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	uA
	CLKSEL	V _{IN} = 0.4V		25	uA
	RESET	V _{IN} = 0.5V		-325	uA
	TTL, CSEL, BSEL	V _{IN} = 0.4V		15	uA
V _{OH}	Output HIGH Voltage	F _{OUT} = 80MHz max C _L = 10pF	2.4		V
V _{OL}	Output LOW Voltage	F _{OUT} = 80MHz max C _L = 10pF		0.6	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 4 @ 70°C, Typ Pwr=370mW		600	mW

1. Maximum test duration, one second.
2. The SC3507 features source series termination of approximately 40 Ohms to assist in matching 50-75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The SC3507 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3507 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -8mA	2.4V	
V _{OL}	I _{OL} = 4mA		0.6V

Table 2. AC Specifications — Using Figure 4, AC Test/Evaluation Circuit

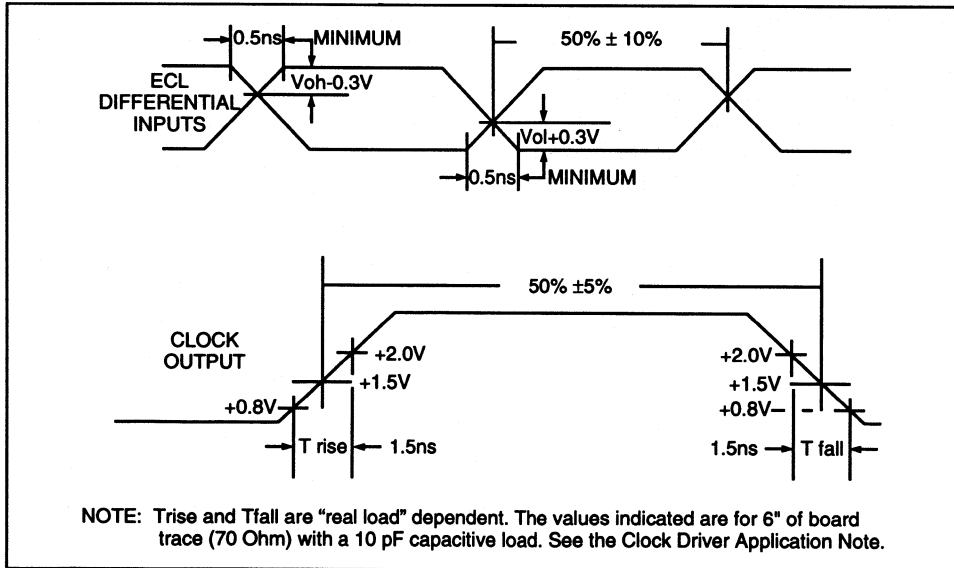
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10pF$

Parameter	SC3507-1	SC3507	Units
Maximum Skew Across All Outputs	0.5	1.0	ns
Maximum Skew Across Fa1 Outputs	0.25	0.25	ns
Maximum Skew Across Fa2 Outputs	0.25	0.25	ns
Maximum Skew Across Fb Outputs	0.25	0.25	ns
Maximum Skew Across Fc Outputs	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry	± 1.0	± 1.0	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum PECL Differential Input Frequency	160	160	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
5. Parameters guaranteed by design and characterization.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION

(Refer to Logic Diagram)

AMCC has developed a single-chip clock driver with twenty outputs using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across all twenty outputs.

For best performance this approach requires a clock source input from a crystal controlled oscillator (XCO) located adjacent to this clock driver. This oscillator, operating between +5V and ground, can provide either differential ECL inputs (referenced to +5V, PECL), or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to a toggle flip-flop and to output flip-flops for synchronization (refer to Figure 1, Logic Diagram). The output duty cycle asymmetry becomes largely a function of the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor ($4.7\mu\text{F} = \sim 100\text{ ms}$) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. On the first falling edge clock input after RESET goes low, the outputs will go low in sequence (the output divide count continues, but once an output goes low, it is held low). When RESET is released (high), the outputs will resume counting, after five falling-edge clock input delays, from their low state (see Figure 5, Reset To Output Timing in the Clock Driver Application Note).

The output drivers are rise and fall slew rate controlled to $\sim 1.5\text{V/ns}$ to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination ($\sim 40\text{ Ohms}$) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance ($>25\text{pF}$ with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes ($>3.5\text{ Volts}$), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3507 will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

Table 3. Output Clock Frequency Selection

“B” SEL	“C” SEL	XCO FREQ	Fa1, Fa2	Fb	Fc
LO	LO	F	F/2	F/4	F/4
HI	LO	F	F/2	F/2	F/4
LO	HI	F	F/2	F/4	F/2
HI	HI	F	F/2	F/2	F/2

Note: XCO is the input frequency for either the PECL inputs or the TTL input. Non-crystal oscillator sources may be used at the user's discretion. See Application Note #1.

Power Management

The overall goal of managing the power dissipated by the SC3507 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3507 is determined by the load that each output drives and the frequency that each output is running. Table 4 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The output power must be added to the core power (600 mW) of the SC3507 to determine the total power being dissipated by the SC3507. This total power is then multiplied by the SC3507's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3507. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3507 is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3507 with 8 Fa outputs driving 10 pF loads at 66 MHz, 3 Fb outputs driving 5 pF loads at 33 MHz and 2 Fc outputs driving 15 pF loads at 33 MHz. Total chip power is calculated as follows:

Core Power	= 600 mW
8 Fa, 10 pF, 66 MHz = (8 x 47 mW)	= 376 mW
2 Fa, no load, 66 MHz = (2 x 16 mW)	= 32 mW
3 Fb, 5 pF, 33 MHz = (3 x 19 mW)	= 57 mW
2 Fb, no load, 33 MHz = (2 x 12 mW)	= 24 mW
2 Fc, 15 pF, 33 MHz = (2 x 24 mW)	= 48 mW
3 Fc, no load, 33 MHz = (3 x 12 mW)	= 36 mW

Total Power = 1173 mW

The design specifies a 70°C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2°C/watt. The SC3507's junction temperature would then be:

$70^{\circ}\text{C} + (1.173 \text{ watts} \times 46.2^{\circ}\text{C/watt}) = 124^{\circ}\text{C}$

Note this is below the 140°C maximum junction temperature.

Table 4. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

Figure 4. AC Test/Evaluation Circuit

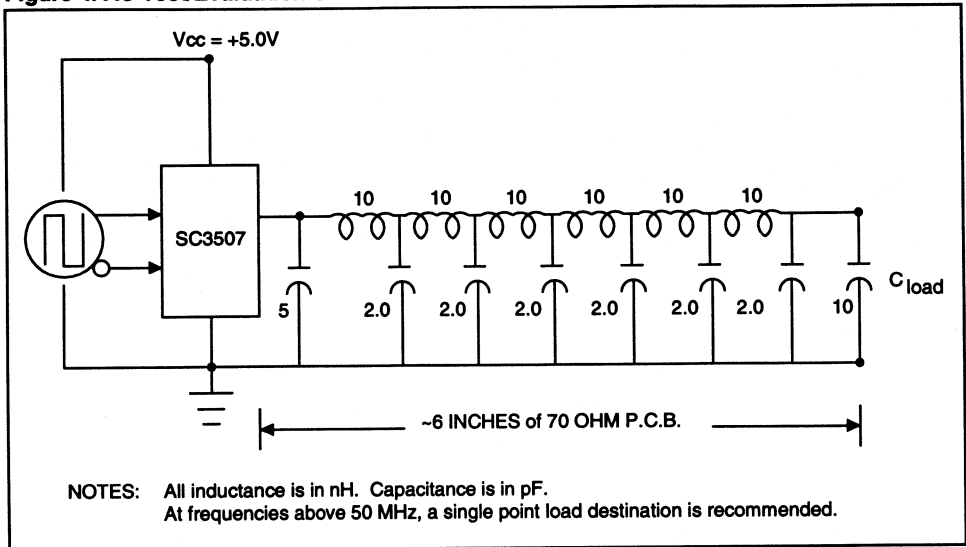


Figure 5. Relative Output Timing

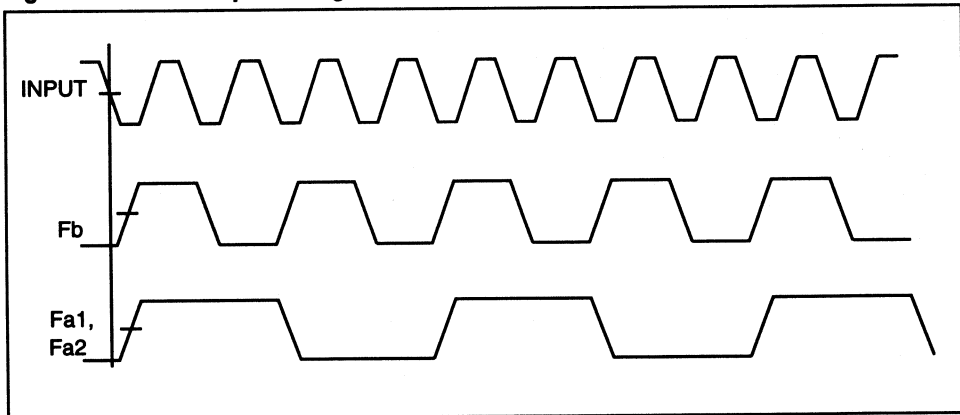
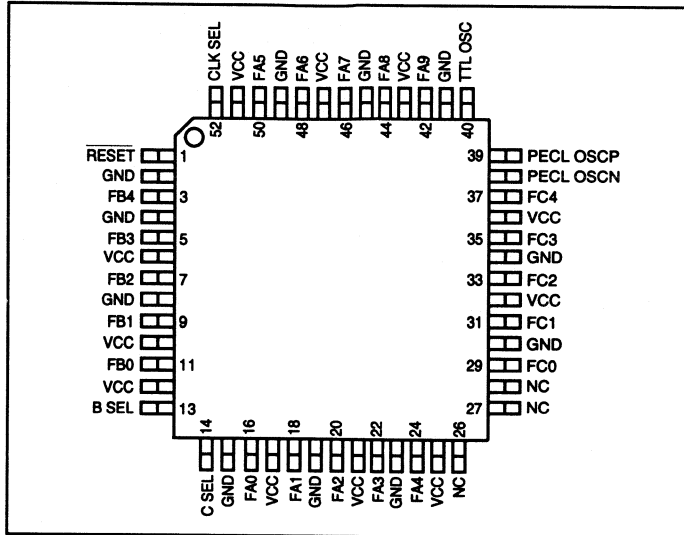


Figure 6. SC3507 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC3507

Q

-1

/TD

Optional Shipping Configuration
 Blank = 84-unit matrix tray
 /D = dry pack
 /TD = tape, reel and dry pack

Skew Option
 Blank = 1.0 ns output-output skew
 -1 = 500 ps output-output skew

Package Option
 Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: SC3507Q-1/D

52-pin PQFP package, 500 ps output-output skew,
 shipped dry packed in the standard matrix tray.

FEATURES

- **20 clock outputs at primary frequency up to 80 MHz**
- **Leading edge skew for all outputs ≤ 0.5 ns**
- **Proprietary output drivers with:**
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 Ω source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

GENERAL DESCRIPTION

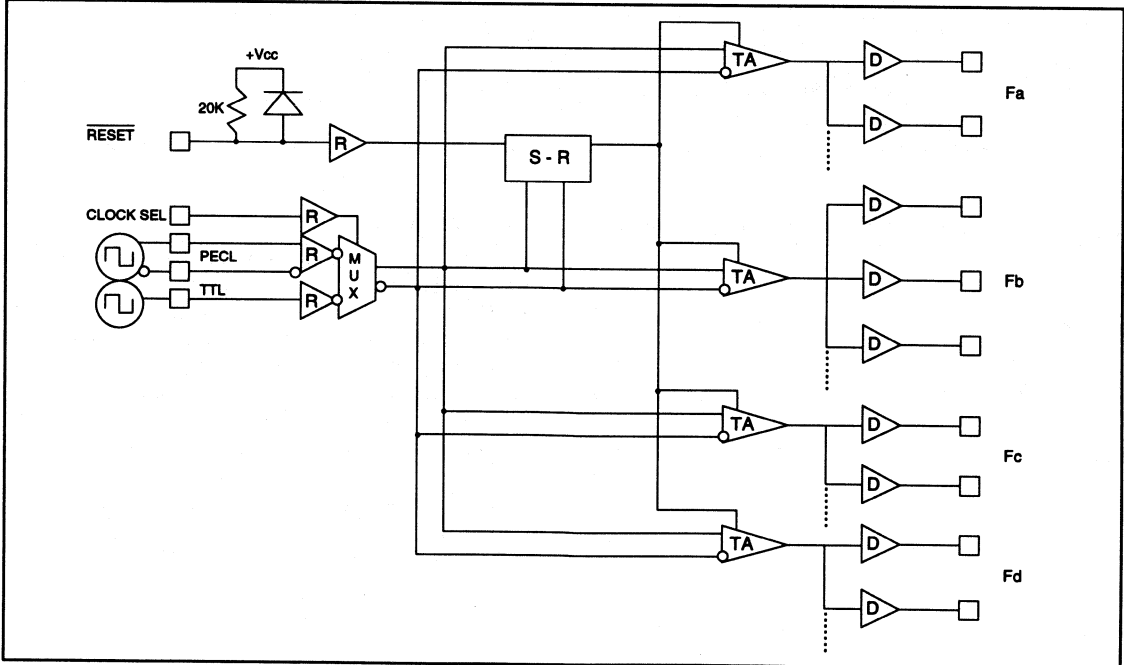
The SC3508 is a minimum skew clock driver with 20 outputs. It can employ a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide “source (series) termination” at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise and distortion.

APPLICATIONS

- **Datacom and Telecom networks**
- **Compatible with Intel’s Pentium™ processor**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

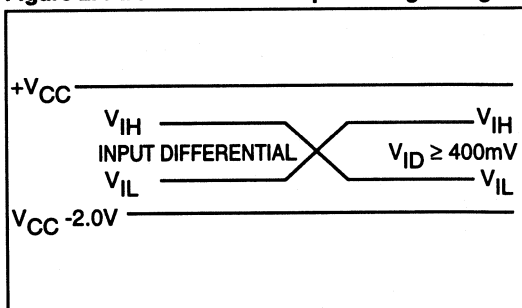
Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source-PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs including Clock	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source-PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs including Clock	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	Reset	V _{IN} = 2.4V		-200	µA
	TTL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	µA
	CLKSEL	V _{IN} = 0.4V		25	µA
	Reset	V _{IN} = 0.5V		-325	µA
	TTL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 80MHz max C _L = 10pF	2.4		V
V _{OL}	Output LOW Voltage	F _{OUT} = 80MHz max C _L = 10pF		0.6	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3 @ 70°C, Typ Pwr=340mW		550	mW

- Maximum test duration, one second.
- The SC3508 features source series termination of approximately 40 Ohms to assist in matching 50-75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The SC3508 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3508 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -8mA	2.4V	
V _{OL}	I _{OL} = 4mA		0.6V

Table 2. AC Specifications—Using Figure 4, AC Test/Evaluation Circuit

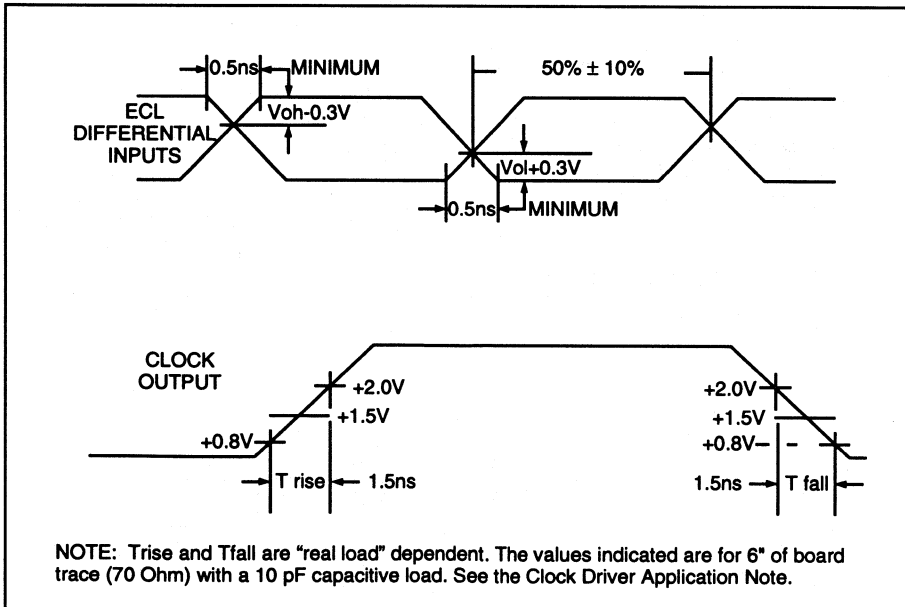
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $70^\circ C$, $C_{LOAD} = 10pF$

Parameter	SC3508-2	SC3508-1	SC3508	Units
Maximum Skew Across All Outputs	0.5	0.5	1.0	ns
Maximum Skew Chip to Chip	1.0	—	—	ns
Maximum Skew Across Fa, Fb, Fc, or Fd Outputs	0.25	0.25	0.25	ns
Maximum TTL Input Frequency	80	80	80	MHz
Maximum PECL Differential Input Frequency	80	80	80	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Chip-to-chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 0.5 ns/V and 10 ps/°C. Chip-to-chip skew tested at 70°C.
3. The SC3508 output symmetry follows input symmetry. Output Duty Cycle will also be affected by voltage and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
6. Parameters guaranteed by design and characterization.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION

(Refer to Logic Diagram)

AMCC has developed a single-chip clock buffer and twenty-output fanout driver using AMCC's advanced BiCMOS process. This design has been optimized for absolute minimum skew across all twenty outputs.

For best performance, this approach will require a clock source input from a crystal controlled oscillator (XCO) located adjacent to this clock driver. This oscillator can provide either differential ECL inputs (referenced to +5V, PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to translation amplifiers and output drivers, (refer to the Figure 1, Logic Diagram). The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

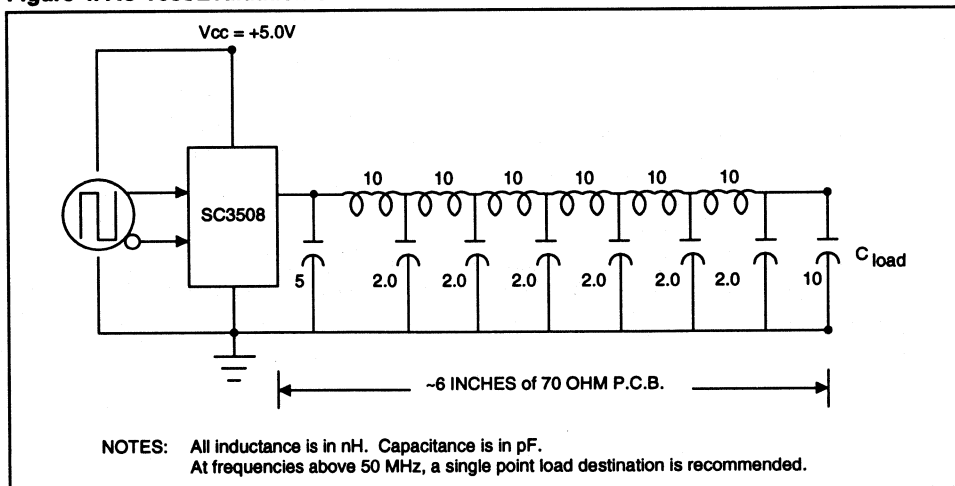
The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high) outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 24 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance +V_{CC} and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to ensure that the SC3508 will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

Figure 4. AC Test/Evaluation Circuit



Power Management

The overall goal of managing the power dissipated by the SC3508 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3508 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The output power must be added to the core power (550 mW) of the SC3508 to determine the total power being dissipated by the SC3508. This total power is then multiplied by the SC3508's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3508. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3508 is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3508 with 12 outputs driving 15 pF loads at 50 MHz. Total chip power is calculated as follows:

$$\begin{aligned} \text{Core Power} &= 550 \text{ mW} \\ 12 \text{ outputs, } 15 \text{ pF, } 50 \text{ MHz} &= (12 \times 39 \text{ mW}) = 468 \text{ mW} \\ 8 \text{ outputs, no load, } 50 \text{ MHz} &= (8 \times 14 \text{ mW}) = 112 \text{ mW} \\ \text{Total Power} &= 1130 \text{ mW} \end{aligned}$$

The design specifies a 70°C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2°C/watt. The SC3508's junction temperature would then be:

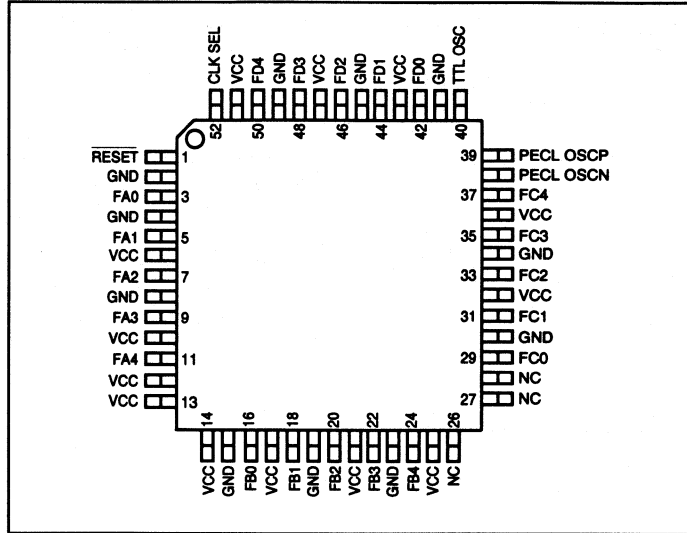
$$70^\circ\text{C} + (1.13 \text{ watts} \times 46.2^\circ\text{C/watt}) = 122^\circ\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

Figure 5. SC3508 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC3508

Q

-1

/TD

Optional Shipping Configuration

Blank = 84-unit matrix tray
 /D = dry pack
 /TD = tape, reel and dry pack

Skew Option

Blank = 1.0 ns output-output skew
 -1 = 500 ps output-output skew

Package Option

Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: SC3508Q-1/D

52-pin PQFP package, 500 ps output-output skew, shipped dry packed in the standard matrix tray.

FEATURES

- **Ten clock outputs:**
 - Five outputs at primary frequency, up to 80 MHz
 - Five outputs at primary or 1/2 primary frequency
- **Leading edge skew for all outputs ≤ 0.5 ns**
- **Proprietary output drivers with:**
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 Ω source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

- **Datacom and Telecom networks**
- **Compatible with Intel's Pentium™ processor**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**

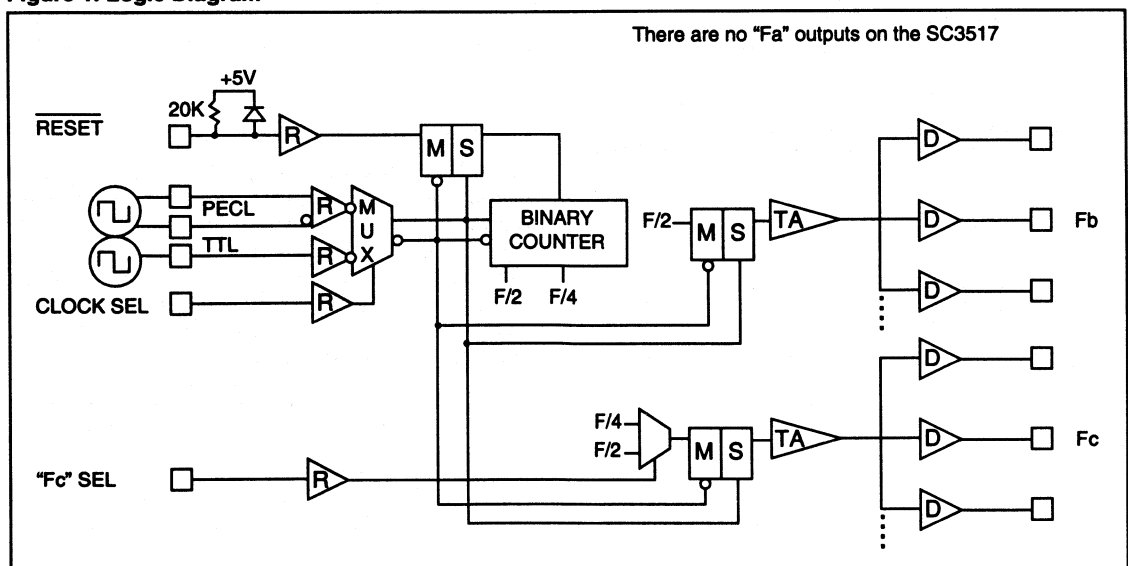
GENERAL DESCRIPTION

The SC3517 is a precision low skew clock driver with ten outputs. It requires a 2X frequency clock input from a single-ended TTL or an ECL differential source operating between +5V and ground. This 2X reference frequency input is received and distributed to symmetrical, divide-by-two master-slave flip-flops. The resultant output is distributed to the clock output drivers.

The ten clock outputs are divided into two groups. The first group of five (5) outputs are unconditionally at the primary frequency, "Fb" = F input/2. The second group, "Fc", of five outputs can be selected to be either identical to "Fb" or at 1/2 the frequency of "Fb". There are no "Fa" outputs on the SC3517.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise and distortion.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

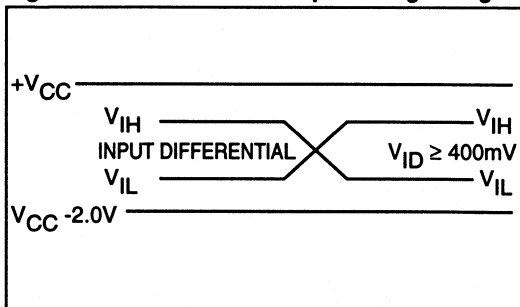
Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source-PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source-PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	uA
	CLKSEL	V _{IN} = V _{CC} (max)		350	uA
	RESET	V _{IN} = 2.4V		-200	uA
	TTL, CSEL	V _{IN} = 2.4V		15	uA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	uA
	CLKSEL	V _{IN} = 0.4V		25	uA
	RESET	V _{IN} = 0.5V		-325	uA
	TTL, CSEL	V _{IN} = 0.4V		15	uA
V _{OH}	Output HIGH Voltage	F _{OUT} = 80MHz max C _L = 10pF	2.4		V
V _{OL}	Output LOW Voltage	F _{OUT} = 80MHz max C _L = 10pF		0.6	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 4 @ 70°C, Typ Pwr 370 mW		600	mW

1. Maximum test duration, one second.
2. The SC3517 features source series termination of approximately 40 Ohms to assist in matching 50-75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The SC3517 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3517 will dynamically adjust source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -8mA	2.4V	
V _{OL}	I _{OL} = 4mA		0.6V

Table 2. AC Specifications — Using Figure 4, AC Test/Evaluation Circuit

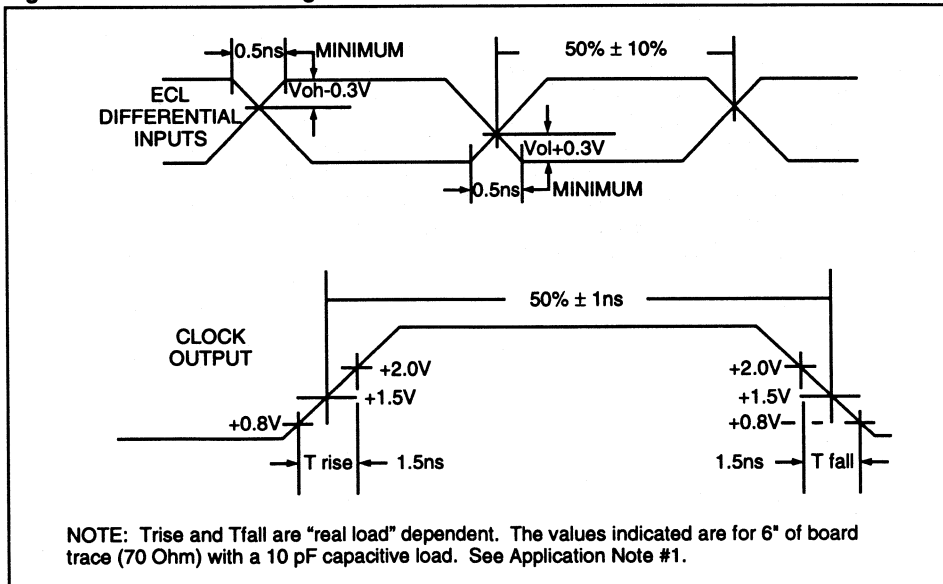
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $70^\circ C$, $C_{LOAD} = 10pF$

Parameter	SC3517-1	SC3517	Units
Maximum Skew Across All Outputs	0.5	1.0	ns
Maximum Skew Across Fb Outputs	0.25	0.25	ns
Maximum Skew Across Fc Outputs	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry	± 1.0	± 1.0	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum PECL Differential Input Frequency	160	160	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50 ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pf capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
5. Parameters guaranteed by design and characterization.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION

(Refer to Logic Diagram)

AMCC has developed a single-chip clock driver with ten outputs using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across all ten outputs.

For best performance this approach will require a 2X clock source input. This input frequency source, operating between +5V and ground, can provide either differential ECL inputs (referenced to +5V, PECL) or single-ended TTL (CMOS) input level to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") select TTL and logic HIGH selects PECL. This 2X input clock will be fanned out to a divide counter and to flip-flops for synchronization, then to the translation amplifiers and output drivers (refer to Figure 1, Logic Diagram). The output duty cycle asymmetry is largely a function of the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor ($4.7\mu\text{F} = \sim 100\text{ ms}$) is connected between this pin and ground, the device will respond with a "power up reset" — a delay in the clock outputs becoming active. On the first falling edge clock input after RESET goes low, the outputs will go low in sequence (the output divide count continues, but once an output goes low, it is held low). When RESET is released (high), the outputs will resume counting, after five falling-edge clock input delays, from their low state (see Figure 5, Reset To Output Timing in the Clock Driver Application Note).

The output drivers are rise and fall slew rate controlled to $\sim 1.5\text{V/ns}$ to minimize noise and distortion resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination ($\sim 40\text{ Ohms}$) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two I.C. input package receiver pins). When applications require large load capacitance ($>25\text{pF}$ with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes ($>3.5\text{ Volts}$), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note).

Power and ground are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{\text{CC}}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3517 will exhibit skews less than the specified maximum. A plastic 28-lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

Table 3. Output Clock Frequency Selection

"C" SEL	XCO FREQ	Fb	Fc
LO	F	F/2	F/4
HI	F	F/2	F/2

Note: XCO is the input frequency for either the PECL Inputs or the TTL Input. Non-crystal oscillator sources may be used at the user's discretion. See Application Note #1.

Power Management

The overall goal of managing the power dissipated by the SC3517 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3517 is determined by the load that each output drives and the frequency that each output is running. Table 4 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The output power must be added to the core power (600 mW) of the SC3517 to determine the total power being dissipated by the SC3517. This total power is then multiplied by the SC3517's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3517. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3517 is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3517 with 5 Fa outputs driving 10 pF loads at 66 MHz and 4 Fb outputs driving 15 pF loads at 33 MHz. Total chip power is calculated as follows:

Core Power	=	600 mW
5 Fa, 10 pF, 66 MHz = (5 x 47 mW)	=	235 mW
4 Fb, 15 pF, 33 MHz = (4 x 24 mW)	=	96 mW
1 Fb, no load, 33 MHz = (1 x 12 mW)	=	12 mW

Total Power = 1173 mW

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The SC3517's junction temperature would then be:

$70^{\circ}\text{C} + (0.943 \text{ watts} \times 57.7^{\circ}\text{C/watt}) = 124^{\circ}\text{C}$

Note this is below the 140°C maximum junction temperature.

Table 4. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

Figure 4. AC Test/Evaluation Circuit

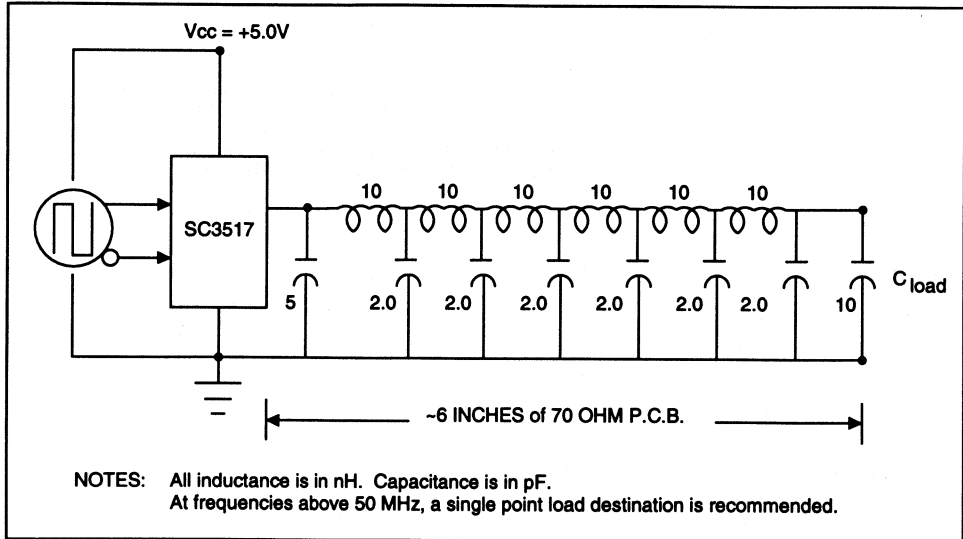
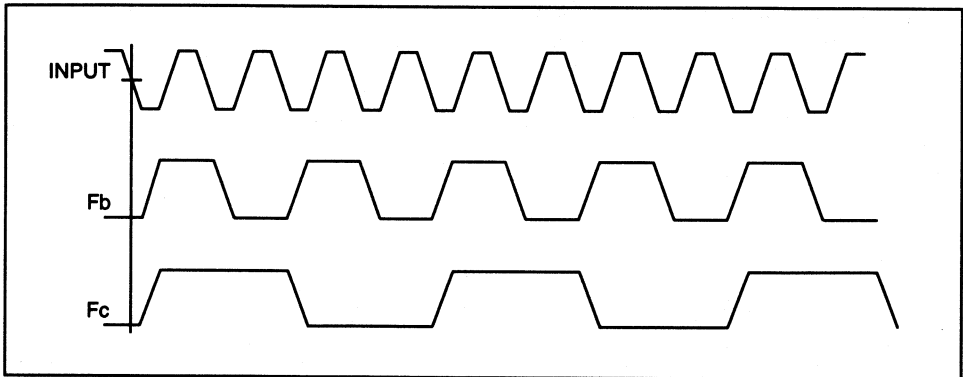
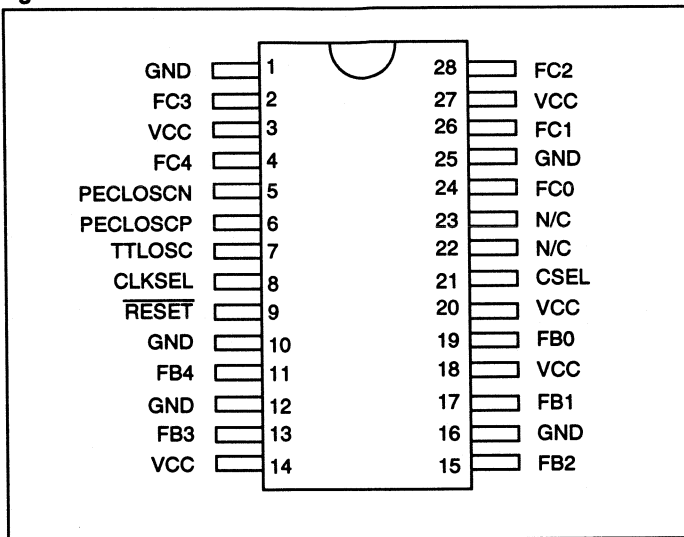


Figure 5. Relative Output Timing



The outputs of the SC3517 are nominally centered to provide a clean 50% duty cycle, symmetrical waveform at the +1.5V threshold reference (see Figure 3, Threshold Crossing Characteristics, for the conditions).

Figure 6. SC3517 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC3517

S

-1

/TD

Optional Shipping Configuration

Blank = 25-unit tube

/D = dry tape

/TD = tape and reel, dry pack

Skew Option

Blank = 1.0 ns output-output skew

- 1 = 500 ps output-output skew

Package Option

S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: SC3517S-1/D
28-pin SOIC package, 500 ps output-output skew,
shipped dry packed in the standard tube.

FEATURES

- Ten clock outputs at primary frequency up to 80 MHz
- Leading edge skew for all outputs ≤ 0.5 ns
- Proprietary output drivers with:
 - Complementary 24 mA peak outputs, source and sink
 - 50-75 Ω source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers

APPLICATIONS

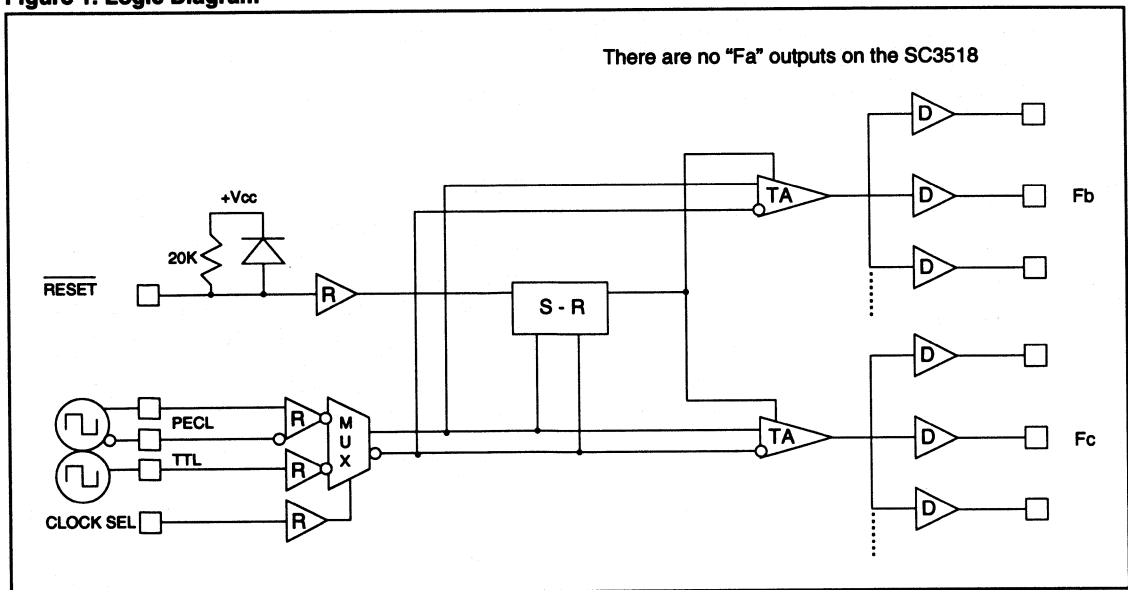
- Datacom and Telecom networks
- Compatible with Intel's Pentium™ processor
- PCI Bus clock distribution
- Workstation and server systems with high clock fanout

GENERAL DESCRIPTION

The SC3518 is a minimum skew clock driver with ten outputs. It can employ a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground. This reference frequency input is received and distributed to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise and distortion.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

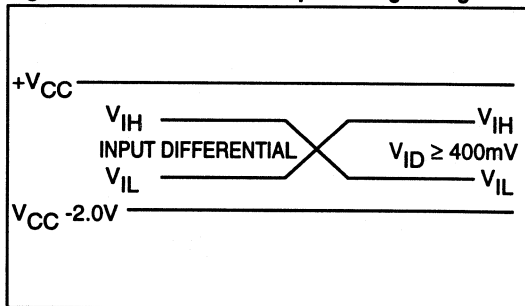
Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source-PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source-PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	µA
	CLKSEL	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 80MHz max C _L = 10pF	2.4		V
V _{OL}	Output LOW Voltage	F _{OUT} = 80MHz max C _L = 10pF		0.6	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3 @ 70°C, Typ Pwr 250 mW		425	mW

1. Maximum test duration, one second.
2. The SC3518 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The SC3518 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic “high-drive, totem-pole outputs” and AMCC’s dynamically adjusting source series terminated outputs. As a result of this, the SC3518 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -8mA	2.4V	
V _{OL}	I _{OL} = 4mA		0.6V

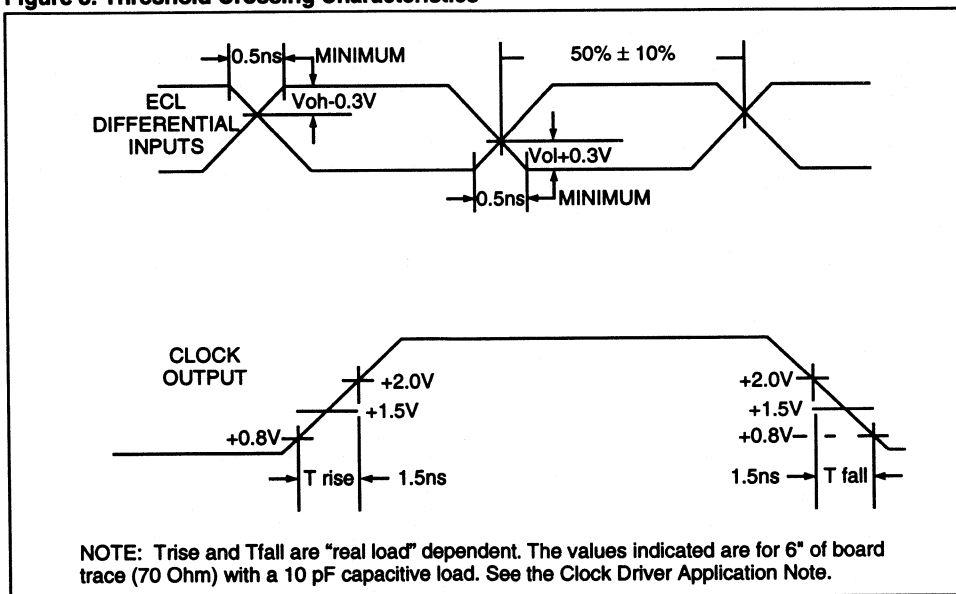
Table 2. AC Specifications – Using Figure 4, AC Test/Evaluation Circuit
 $V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10pF$

Parameter	SC3518-1	SC3518	Units
Maximum Skew Across All Outputs	0.5	1.0	ns
Maximum Skew Across Fb or Fc Outputs	0.25	0.25	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum Differential PECL Input Frequency	80	80	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The SC3518 output symmetry follows input symmetry. Output duty cycle will also be affected by voltage and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
5. Parameters guaranteed by design and characterization.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single-chip, ten-output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for absolute minimum skew across all ten outputs.

The clock source input for this device may operate between +5V and ground and can provide either differential ECL inputs (referenced to +5V, PECL) or single-ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL. This input clock will be fanned out to translation amplifiers and output drivers, refer to the preceding logic diagram. The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high) the outputs will resume, after four falling-edge clock inputs, from a high (leading edge) count origin.

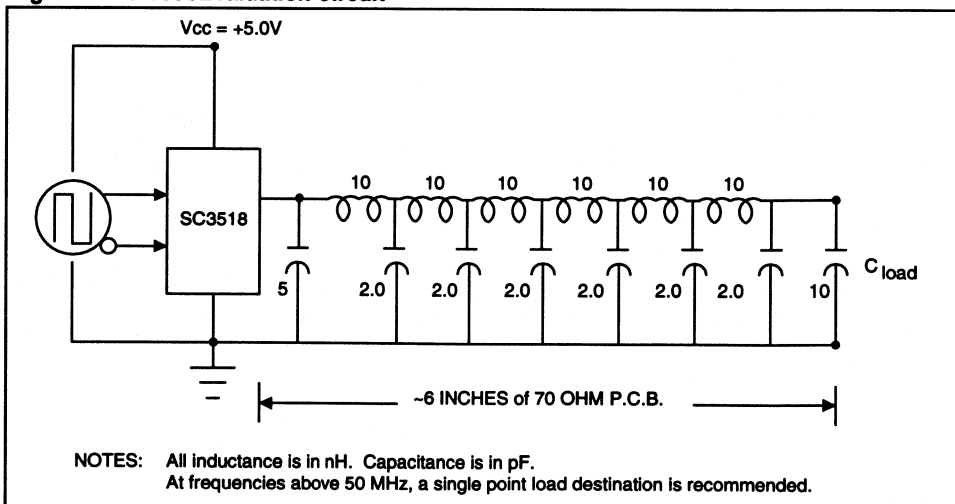
The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion

resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note).

Power and ground are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance +V_{CC} and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3518 will exhibit skews less than the specified maximum. A plastic 28-lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

Figure 4. AC Test/Evaluation Circuit



Power Management

The overall goal of managing the power dissipated by the SC3518 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3518 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The above output power must be added to the core power (425 mW) of the SC3518 to determine the total power being dissipated by the SC3518. This total power is then multiplied by the SC3518's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3518. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3518 is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3518 with 8 outputs driving 10 pF loads at 66 MHz. Total chip power is calculated as follows:

$$\begin{aligned} \text{Core Power} &= 425 \text{ mW} \\ 8 \text{ outputs, } 10 \text{ pF, } 66 \text{ MHz} &= (8 \times 47 \text{ mW}) = 376 \text{ mW} \\ 2 \text{ outputs, no load, } 66 \text{ MHz} &= (2 \times 16 \text{ mW}) = 32 \text{ mW} \\ \text{Total Power} &= 833 \text{ mW} \end{aligned}$$

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The SC3518's junction temperature would then be:

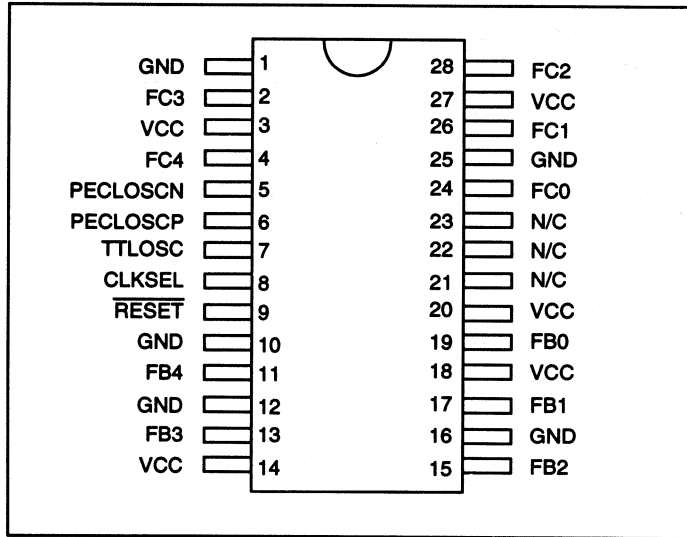
$$70^\circ\text{C} + (0.833 \text{ watts} \times 57.7^\circ\text{C/watt}) = 118^\circ\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

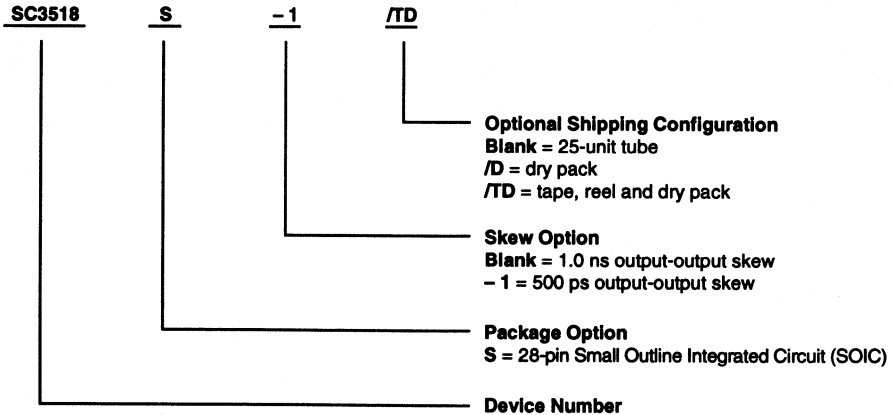
Figure 5. SC3518 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- Device Number
- Package Type
- Skew Option (if applicable)
- Optional Shipping Configuration



Example: SC3518S-1/D
28-pin SOIC package, 500 ps output-output skew,
shipped dry packed in the standard tube.

FEATURES

- **Five clock outputs at reference frequency up to 80 Mhz**
- **Four clock outputs at half reference frequency up to 40 Mhz**
- **Leading edge skew for all outputs <350 ps**
- **Proprietary output drivers with:**
 - Complementary 24 mA peak outputs, source and sink
 - 50–75Ω equivalent source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

GENERAL DESCRIPTION

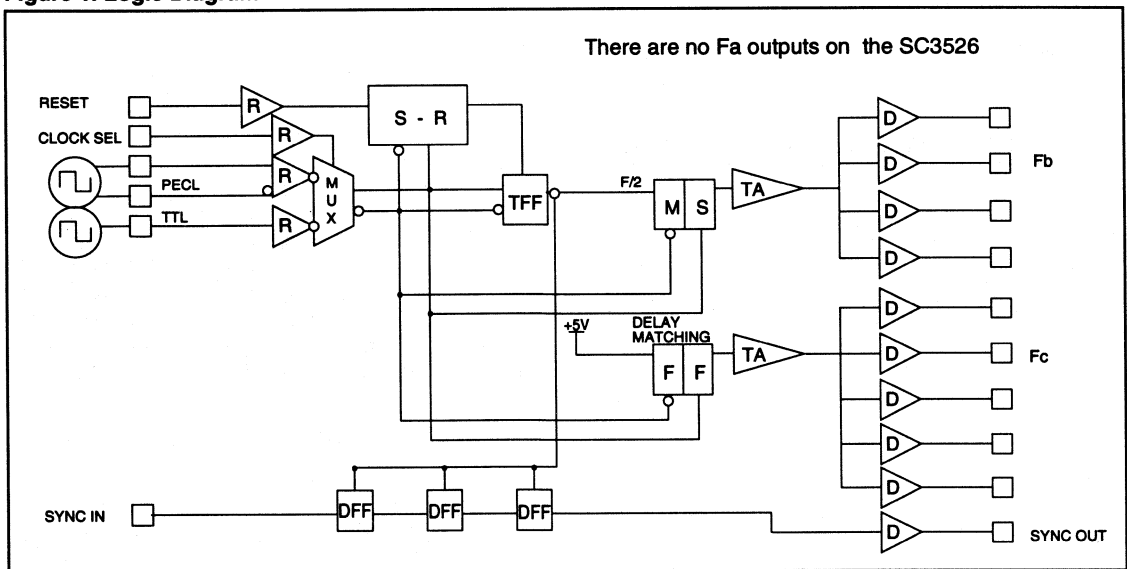
The SC3526 is a low skew clock driver with nine outputs. Five outputs operate at the primary reference frequency and four outputs operate at half the primary reference frequency. A synchronous reset ensures proper phase of the half frequency outputs. It can employ a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide “source (series) termination” at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output-switching noise, distortion, and EMI.

APPLICATIONS

- **Datcom and Telecom networks**
- **Compatible with Intel’s Pentium™ processor**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

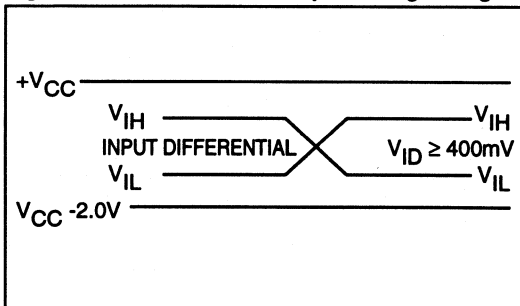
Table 1. Electrical Characteristics

 V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs including clock	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs including clock	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	Reset	V _{IN} = 2.4V		-200	µA
	TTL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	µA
	CLKSEL	V _{IN} = 0.4V		25	µA
	Reset	V _{IN} = 0.5V		-325	µA
	TTL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 66MHz max C _L = 10pF	2.4		V
V _{OL}	Output LOW Voltage	F _{OUT} = 66MHz max C _L = 10pF		0.6	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3 @ 70°C, Typ Pwr=225mW		375	mW

1. Maximum test duration, one second.

2. The SC3526 features source series termination to assist in matching 50–75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range


DC Characteristics

The SC3526 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic “high-drive, totem-pole outputs” and AMCC’s dynamically adjusting source series terminated outputs. As a result of this, the SC3526 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -8mA	2.4V	
V _{OL}	I _{OL} = 4mA		0.6V

Table 2. AC Specifications—Using Figure 4, AC Test/Evaluation Circuit

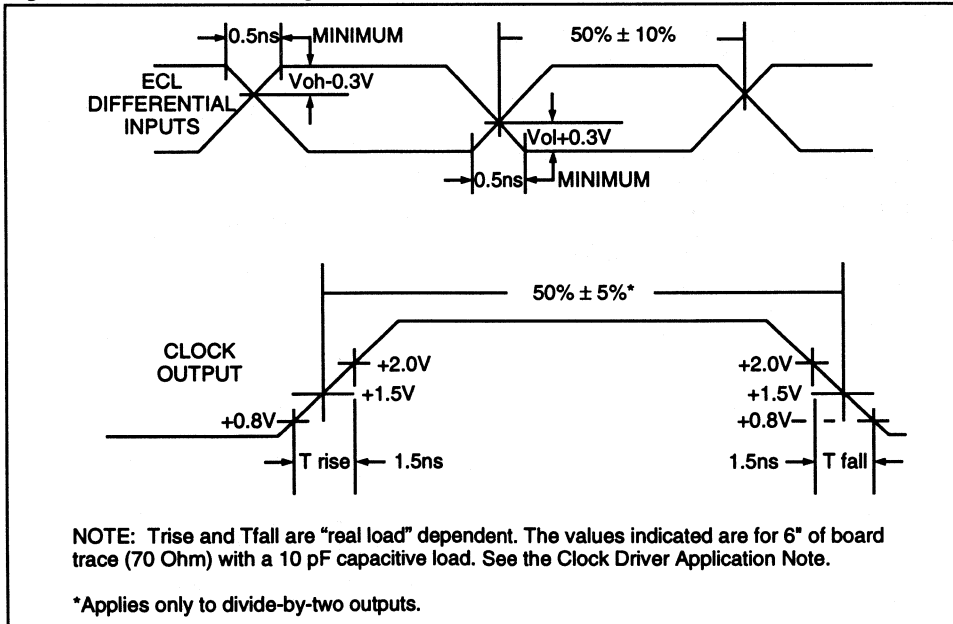
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$, $C_{LOAD} = 10pF$

Parameter	SC3526	Units
Maximum Skew Across All Outputs	350	ps
Maximum Output Duty Cycle Asymmetry	Minimum	45 %
	Maximum	55 %
Maximum TTL Input Frequency	80	MHz
Maximum Differential PECL Input Frequency	80	MHz
Maximum Rising/Falling Edge Rate	1.5	ns
Maximum TTL Output Frequency	80	MHz

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The SC3526 output symmetry follows input symmetry for F_C outputs.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
6. Parameters guaranteed by design and characterization or tested.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single-chip nine-output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across all nine outputs.

The clock source input for this device can provide either differential ECL inputs (referenced to +5V, PECL) or single-ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL. This input clock will be fanned out to translation amplifiers and output drivers (refer to Figure 1, Logic Diagram). The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The synchronization circuit provides three serial flip flops clocked by the internally generated F/2 (half reference frequency) clock which can be used to provide a three-stage metastability filter or a three-cycle delay of the F/2 outputs. The circuit receives its input from the SYNCIN input and feeds the D-input to the first flip-flop; the Q output of the flip-flop feeds the D-input of the second flip-flop which, in turn, feeds the third flip-flop. The Q output of the third flip-flop drives the SYNCOUT pin.

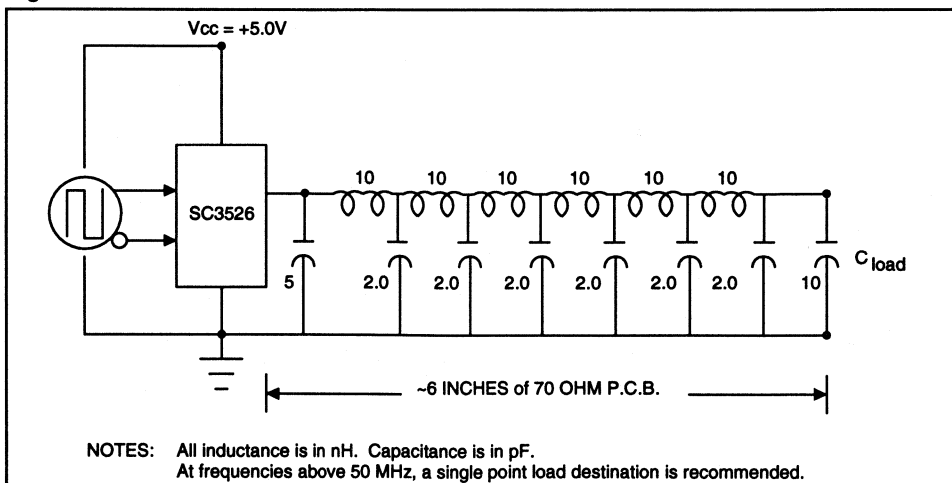
When the RESET input is held high (active), the FA0-4 outputs will continue to run while the FB0-3 outputs will be driven high. When RESET is de-asserted, the FB0-3 outputs will be active after a fixed three-input clock delay, from a leading edge count origin.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the nine outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for simulation results).

To lower noise and maintain signal fidelity, power and ground pins are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance +V_{CC} and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3526 will exhibit skews less than the specified maximum. A plastic 28-lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

Figure 4. AC Test/Evaluation Circuit



Power Management

The overall goal of managing the power dissipated by the SC3526 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3526 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit (for complete load definition).

The individual output power must be added to the static core power (375 mW) of the SC3526 to determine the total power being dissipated by the SC3526. This total power is then multiplied by the SC3526's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3526. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3526 is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3526 with 4 Fb outputs driving 10 pF loads at 33 MHz and 4 Fc outputs driving 15 pF loads at 66 MHz. The Sync Out is not used. Total chip power is calculated as follows:

Core Power		= 375 mW
4 Fb, 10 pF, 33 MHz = (4 x 22 mW)	= 88 mW	
4 Fc, 15 pF, 66 MHz = (4 x 55 mW)	= 220 mW	
1 Fc, no load, 66 MHz = (1 x 16 mW)	= 16 mW	
		Total Power = 699 mW

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The SC3526's junction temperature would then be:

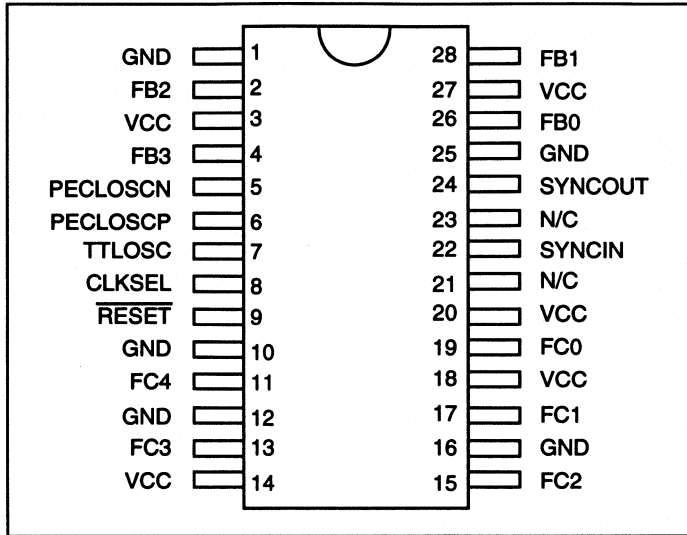
$$70^{\circ}\text{C} + (0.699 \text{ watts} \times 57.7^{\circ}\text{C/watt}) = 110^{\circ}\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

Figure 5. SC3526 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- Device Number
- Package Type
- Optional Shipping Configuration

SC3526

S

/TD

Optional Shipping Configuration

Blank = 25-unit tube

/D = dry pack

/TD = tape, reel and dry pack

Package Option

S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: SC3526S/D

28-pin SOIC package, shipped dry packed in the standard tube.

FEATURES

- Three clock outputs at primary reference frequency up to 80 Mhz
- Seven clock outputs selectable at half primary reference frequency up to 40 Mhz, or at secondary reference frequency up to 80 Mhz
- Selectable single or dual reference frequencies
- Leading edge skew for all F_b outputs <500 ps
- Leading edge skew for all F_c outputs <350 ps
- Proprietary output drivers with:
 - Complementary 24 mA peak outputs, source and sink
 - 50–75Ω equivalent source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers
- Internal ≈ 900 ps delay between F_c and F_b

APPLICATIONS

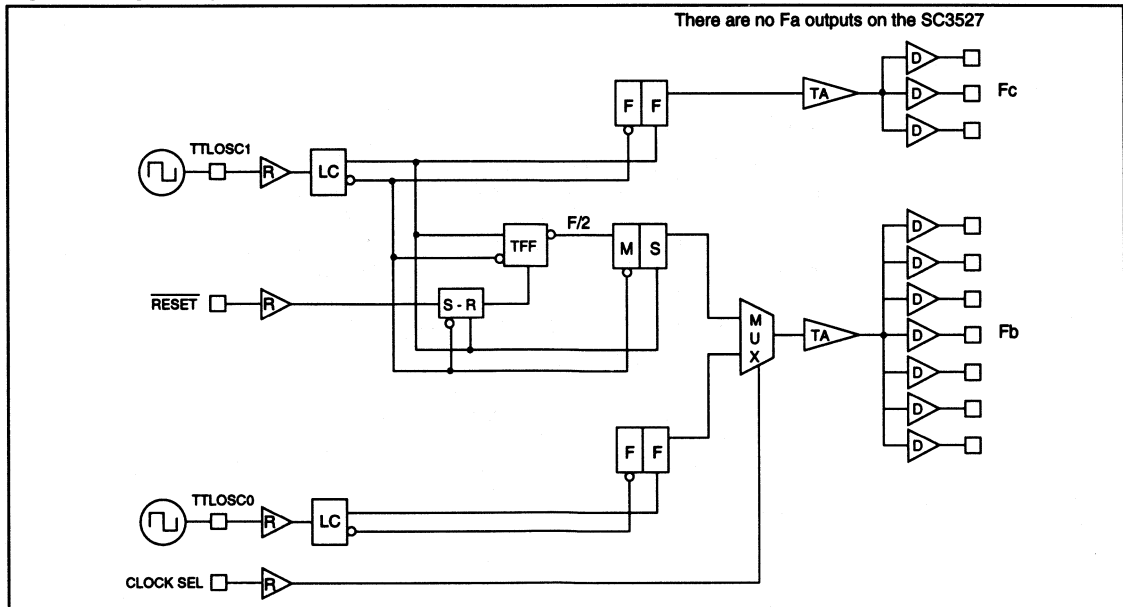
- Datacom and Telecom networks
- Compatible with Intel's Pentium™ processor
- PCI Bus clock distribution
- Workstation and server systems with high clock fanout

GENERAL DESCRIPTION

The SC3527 is a low skew clock driver with ten outputs. Three outputs operate at the primary reference frequency and seven outputs operate at either half the primary reference frequency or at the secondary reference frequency. A synchronous reset ensures proper phase of the half frequency outputs. It can employ clock input from either one or two single-ended TTL sources. These reference frequency inputs are received and distributed to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output-switching noise, distortion, and EMI.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage	All Inputs including Clock	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage	All Inputs including Clock	-0.5	0.8	V
I _{IH}	CLKSEL	V _{IN} = V _{CC} (max)		350	uA
	RESET	V _{IN} = 2.4V		-200	uA
	TTLOSCx	V _{IN} = 2.4V		15	uA
I _{IL}	CLKSEL	V _{IN} = 0.4V		25	uA
	RESET	V _{IN} = 0.5V		-325	uA
	TTLOSCx	V _{IN} = 0.4V		15	uA
V _{OH}	Output HIGH Voltage	F _{OUT} = 66MHz max, C _L = 10pF	2.4		V
V _{OL}	Output LOW Voltage	F _{OUT} = 66MHz max, C _L = 10pF		0.6	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3, Typ Pwr=225mW		350	mW

1. Maximum test duration, one second.
2. The SC3527 features source series termination Ohms to assist in matching 50–75 Ohm P.C. board environments.

DC Characteristics

The SC3527 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic “high drive, totem pole outputs” and AMCC’s dynamically adjusting source series terminated outputs. As a result of this, the SC3527 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -8mA	2.4V	
V _{OL}	I _{OL} = 4mA		0.6V

Table 2. AC Specifications — Using Figure 4, AC Test/Evaluation Circuit

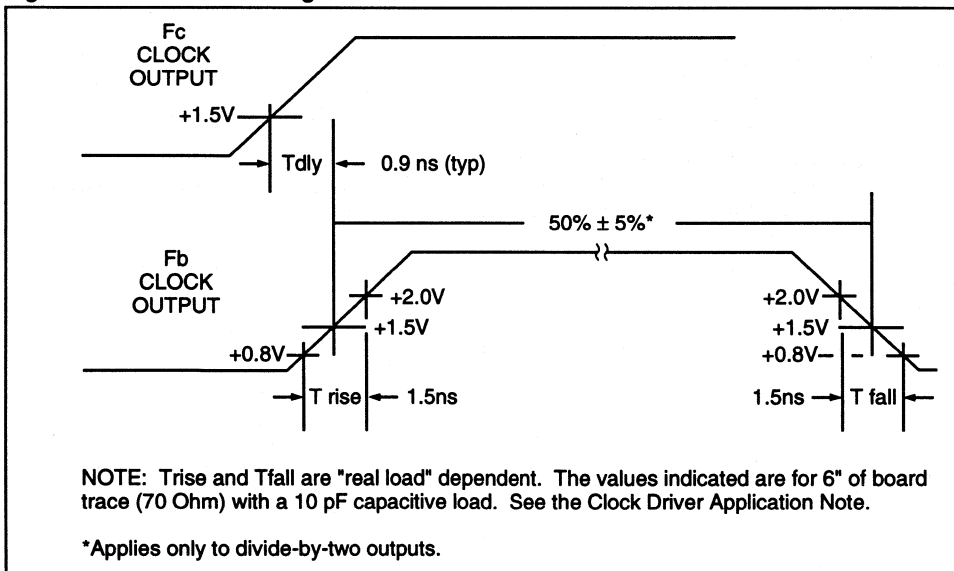
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10pF$
(reference Figure 2, Threshold Crossing Characteristics)

Parameter	SC3527	Units
Maximum Skew Across Fb outputs	500	ps
Maximum Skew Across Fc outputs	350	ps
Delay of Fb from Fc outputs (CLKSEL = 1) [T _{dly}]	Minimum	50
	Typical	0.9
	Maximum	1.7
Maximum Output Duty Cycle Asymmetry	Minimum	45
	Maximum	55
Maximum Rising/Falling Edge Rate [Trise/Tfall]	1.5	ns
Maximum TTL Input Frequency	80	MHz
Maximum TTL Output Frequency	80	MHz

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The SC3527 output symmetry follows input symmetry for F_C outputs.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
6. Parameters guaranteed by design and characterization or tested.

Figure 2. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single-chip ten-output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across outputs of the same frequency.

The clock source input for this device can select either one or two single-ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects the dual reference frequency mode, and logic HIGH selects the single reference frequency (TTLOSC1) mode. This input clock will be fanned out to translation amplifiers and output drivers (refer to the preceding logic diagram). The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

When the $\overline{\text{RESET}}$ input is held low (active), the FB0-6 outputs will be driven low. When $\overline{\text{RESET}}$ is de-asserted, the FB0-6 outputs will be active after a fixed three-input clock delay if the single-reference frequency mode is selected. The reset function is only operational when $\text{CLKSEL} = 1$.

The output drivers are rise and fall slew rate controlled to $\sim 1.5\text{V/ns}$ to minimize noise and distortion resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot

of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance ($>25\text{pF}$ with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for simulation results).

To lower noise and maintain signal fidelity, power and ground pins are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{\text{CC}}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

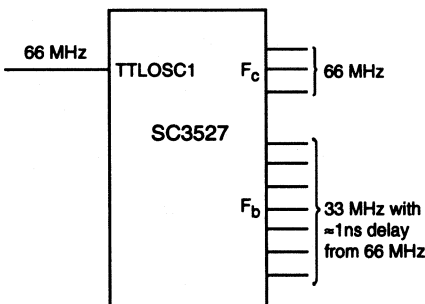
The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3527 will exhibit skews less than the specified maximum. A plastic 28 lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

Figure 3. Application Examples

Example 1.

Low Skew, Single Reference Frequency Mode

Three outputs at the primary frequency and seven outputs at half the primary frequency; each group internally synchronized. The 33 MHz outputs are delayed from the 66 MHz outputs by ≈ 1 ns.

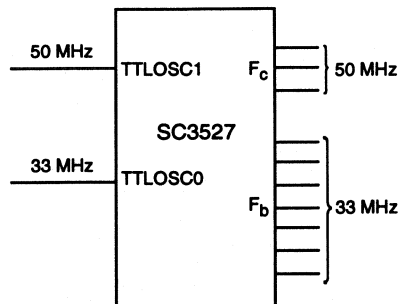


CLKSEL = 1

Example 2.

Dual Reference Frequency Mode, Asynchronous

Three outputs at the primary frequency and seven outputs at the secondary frequency with ≈ 1 ns internal delay at the F_b outputs.



CLKSEL = 0

Power Management

The overall goal of managing the power dissipated by the SC3527 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3527 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit for complete load definition).

The individual output power must be added to the static core power (350 mW) of the SC3527 to determine the total power being dissipated by the SC3527. This total power is then multiplied by the SC3527's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3527. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3527 is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3527 with 3 Fc outputs driving 10 pF loads at 66 MHz and 6 Fb outputs driving 15 pF loads at 33 MHz. Total chip power is calculated as follows:

Core Power	= 350 mW
3 Fc, 10 pF, 66 MHz = (3 x 47 mW)	= 141 mW
6 Fb, 15 pF, 33 MHz = (6 x 24 mW)	= 144 mW
1 Fb, no load, 33 MHz = (1 x 12 mW)	= 12 mW
Total Power	= 647 mW

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The SC3527's junction temperature would then be:

$$70^{\circ}\text{C} + (0.647 \text{ watts} \times 57.7^{\circ}\text{C/watt}) = 107^{\circ}\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

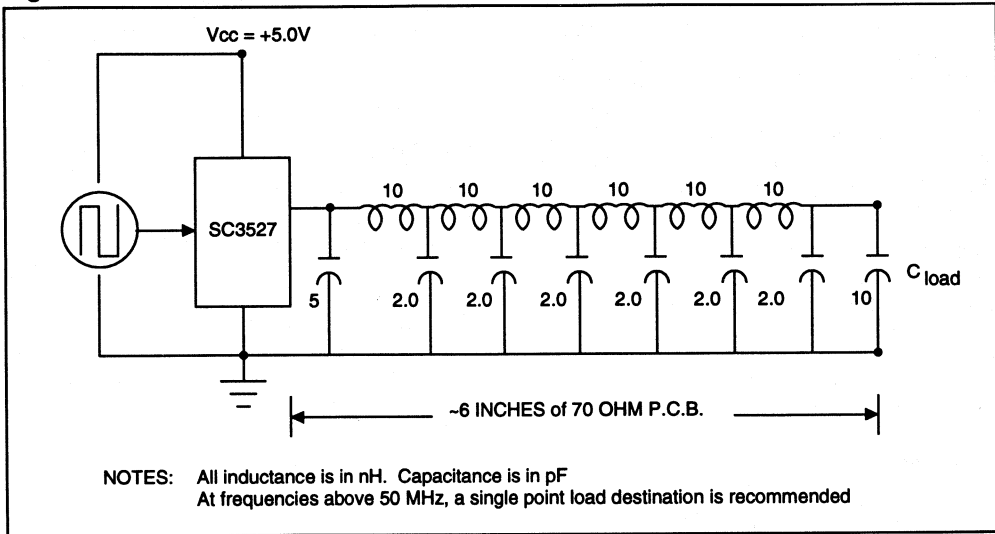
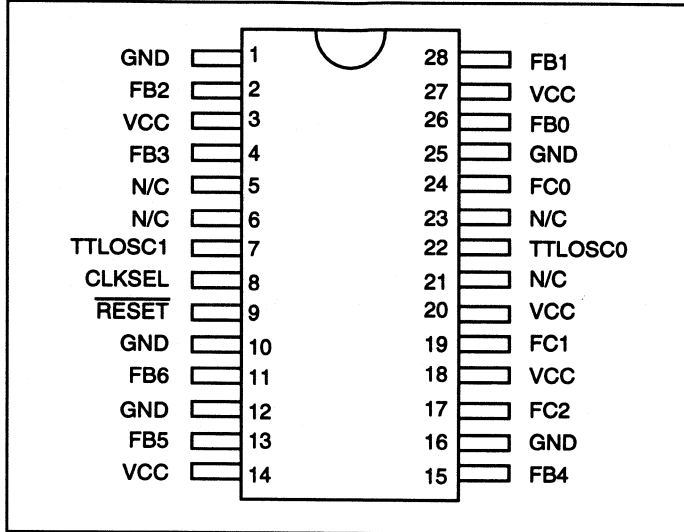
Figure 4. AC Test/Evaluation Circuit

Figure 5. SC3527 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- Device Number
- Package Type
- Optional Shipping Configuration

SC3527

S

/TD

Optional Shipping Configuration

Blank = 25-unit tube

/D = dry pack

/TD = tape, reel and dry pack

Package Option

S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: SC3527S/D

28-pin SOIC package, shipped dry packed in the standard tube.

FEATURES

- **Ten clock outputs at up to 80 MHz**
- **Leading edge skew for all outputs <350 ps**
- **Proprietary output drivers with:**
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 equivalent source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

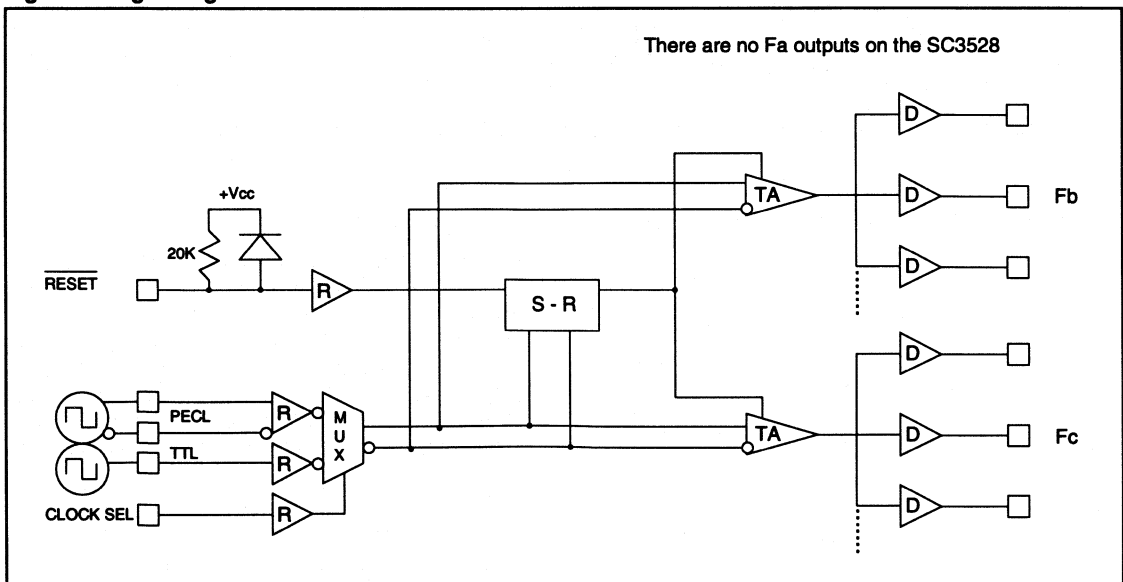
- **Datacom and Telecom networks**
- **Compatible with Intel's Pentium™ processor**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**

GENERAL DESCRIPTION

The SC3528 is a minimum skew clock driver with ten outputs. It can employ a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise, distortion, and EMI.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

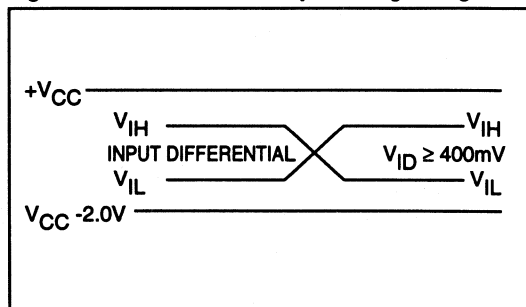
Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source-PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs including clock	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source-PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs including clock	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	µA
	CLKSEL	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 66MHz max C _L = 10pF	2.4		V
V _{OL}	Output LOW Voltage	F _{OUT} = 66MHz max C _L = 10pF		0.6	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3 @ 70°C, Typ Pwr=250mW		425	mW

1. Maximum test duration, one second.
2. The SC3528 features source series termination to assist in matching 50-75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The SC3528 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3528 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -8mA	2.4V	
V _{OL}	I _{OL} = 4mA		0.6V

Table 2. AC Specifications—Using Figure 4, AC Test/Evaluation Circuit

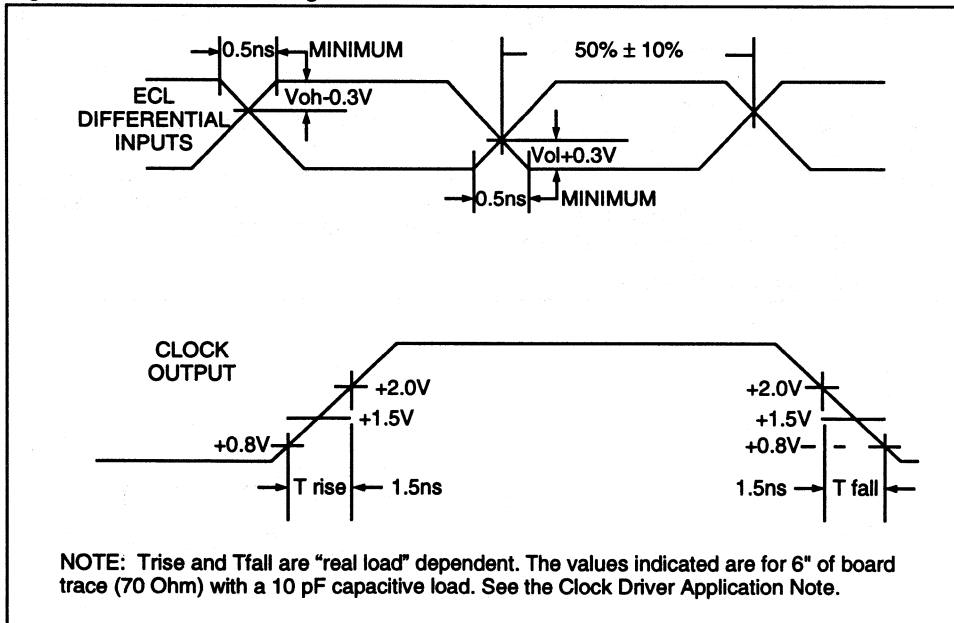
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10pF$

Parameter	SC3528	Units
Maximum Skew Across All Outputs	<350	ps
Maximum TTL Input Frequency	80	MHz
Maximum Differential PECL Input Frequency	80	MHz
Maximum Rising/Falling Edge Rate	1.5	ns
Maximum TTL Output Frequency	80	MHz

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The SC3528 output symmetry follows input symmetry. Output duty will also be affected by voltage and load (including the length of the PC trace).
3. The SC3528 output symmetry follows input symmetry. Output Duty Cycle will also be affected by voltage and load (including the length of the PC trace).
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
5. Parameters guaranteed by design and characterization or tested.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single-chip ten-output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across all ten outputs.

The clock source input for this device can provide either differential ECL inputs (referenced to +5V, PECL) or single-ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL. This input clock will be fanned out to translation amplifiers and output drivers, refer to the preceding logic diagram. The output duty cycle asymmetry becomes largely a function of the input clock wave-shape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power-up reset"—a delay in the clock outputs becoming active. On the fourth falling edge clock input after RESET goes low, the outputs will go low in sequence (the output divide count continues, but once an output goes low, it is held low). When RESET is released (high), the outputs will resume counting, after four falling-edge clock input delays, from their low state.

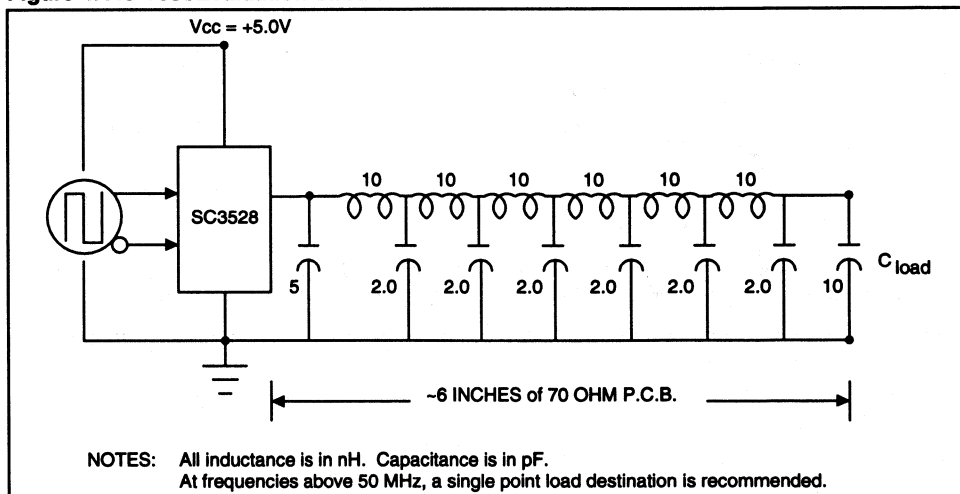
The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion

resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for simulation results).

To lower noise and maintain signal fidelity, power and ground pins are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance +V_{CC} and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3528 will exhibit skews less than the specified maximum. A plastic 28-lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

Figure 4. AC Test/Evaluation Circuit



Power Management

The overall goal of managing the power dissipated by the SC3528 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3528 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The individual output power must be summed and added to the static core power (425 mW) of the SC3528 to determine the total power being dissipated by the SC3528. This total power is then multiplied by the SC3528's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3528. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3528 is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3528 with 9 outputs driving 15 pF loads at 66 MHz. Total chip power is calculated as follows:

$$\begin{aligned} \text{Core Power} &= 425 \text{ mW} \\ 9 \text{ outputs, } 15 \text{ pF, } 66 \text{ MHz} &= (9 \times 55 \text{ mW}) = 495 \text{ mW} \\ 1 \text{ output, no load, } 66 \text{ MHz} &= (1 \times 16 \text{ mW}) = 16 \text{ mW} \\ \hline \text{Total Power} &= 936 \text{ mW} \end{aligned}$$

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The SC3528's junction temperature would then be:

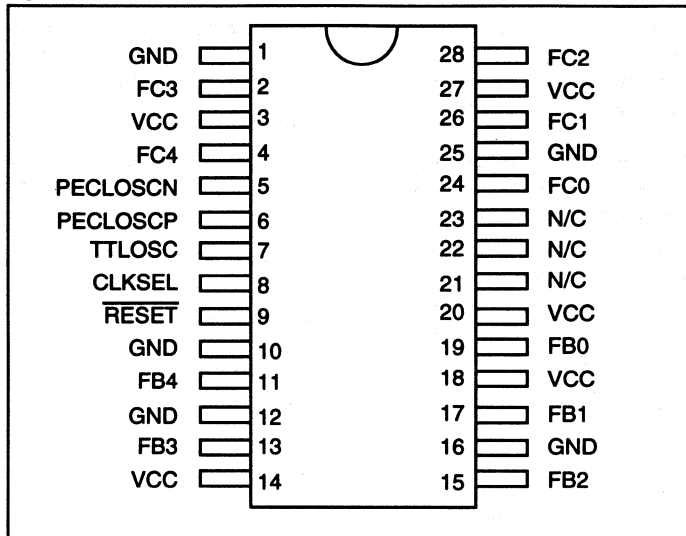
$$70^\circ\text{C} + (0.936 \text{ watts} \times 57.7^\circ\text{C/watt}) = 124^\circ\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

Figure 5. SC3528 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- Device Number
- Package Type
- Optional Shipping Configuration

SC3528

S

/TD

Optional Shipping Configuration

Blank = 25-unit tube

/D = dry pack

/TD = tape, reel and dry pack

Package Option

S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: SC3528S/D

28-pin SOIC package, shipped dry packed in the standard tube.

FEATURES

- Ten clock outputs at up to 80 MHz
- Two control pins enable power-down feature on two, five, or all outputs
- Leading edge skew for all outputs <350 ps
- Proprietary output drivers with:
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 equivalent source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers

APPLICATIONS

- Datacom and Telecom networks
- Compatible with Intel's Pentium™ processor
- PCI Bus clock distribution
- Workstation and server systems with high clock fanout

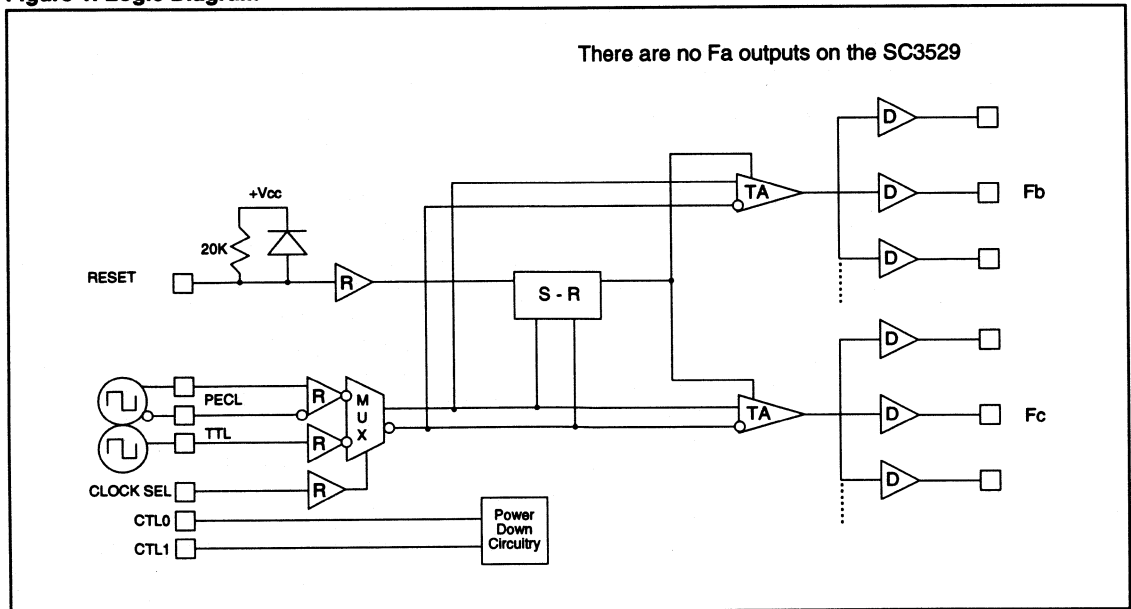
GENERAL DESCRIPTION

The SC3529 is a minimum skew clock driver with ten outputs. It can employ a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to the clock output drivers.

Power-down circuitry is included that allows the disabling of two, five, or all outputs. The two control signals are synchronized to the reference to prevent duty-cycle distortion during power-up or power-down sequencing.

Applied Micro Circuits Corporation (AMCC) uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise, distortion, and EMI.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

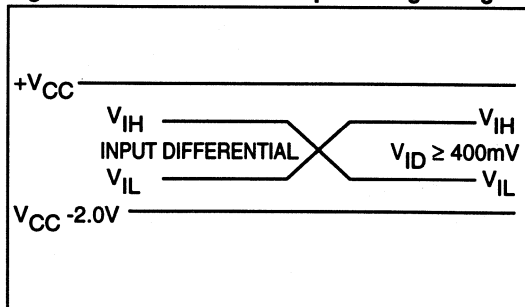
Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source-PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs including clock	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source-PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs including clock	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL, CTLO, CTL1	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	µA
	CLKSEL, CTLO, CTL1	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 66MHz max C _L = 10pF	2.4		V
V _{OL}	Output LOW Voltage	F _{OUT} = 66MHz max C _L = 10pF		0.6	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Disabled Power Dissipation	Ref. Table 4 (Outputs High), Typ Pwr=250mW		425	mW

1. Maximum test duration, one second.
2. The SC3529 features source series termination to assist in matching 50–75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The SC3529 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic “high-drive, totem-pole outputs” and AMCC’s dynamically adjusting source series terminated outputs. As a result of this, the SC3529 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -8mA	2.4V	
V _{OL}	I _{OL} = 4mA		0.6V

Table 2. AC Specifications—Using Figure 4, AC Test/Evaluation Circuit

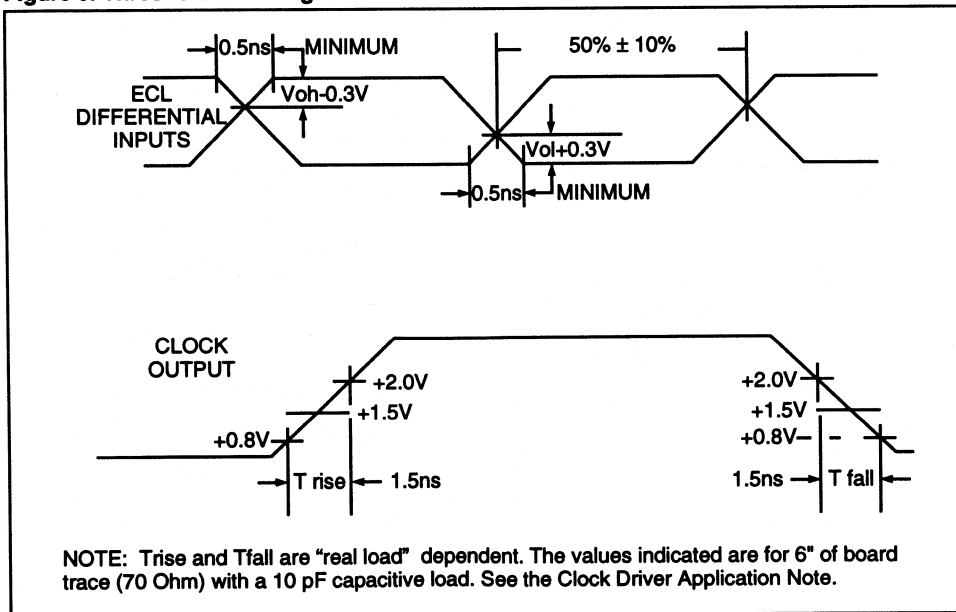
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10pF$

Parameter	SC3529	Units
Maximum Skew Across All Outputs	<350	ps
Maximum TTL Input Frequency	80	MHz
Maximum Differential PECL Input Frequency	80	MHz
Maximum Rising/Falling Edge Rate	1.5	ns
Maximum TTL Output Frequency	80	MHz

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The SC3529 output symmetry follows input symmetry. Output duty cycle will also be affected by voltage and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
5. Parameters guaranteed by design and characterization or tested.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION

(Refer to Logic Diagram)

AMCC has developed a single-chip ten-output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across all ten outputs.

The clock source input for this device can provide either differential ECL inputs (referenced to +5V, PECL) or single-ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL. This input clock will be fanned out to translation amplifiers and output drivers, refer to the preceding logic diagram. The output duty cycle asymmetry becomes largely a function of the input clock wave-shape and the output driver slew rate into the AC load.

The CTL0 and CTL1 inputs can be used to "power down" two, five, or ten of the SC3529's outputs. The control circuitry is designed to be synchronous with the reference clock to prevent duty cycle distortion during power-up or power-down sequencing.

When the inputs are configured per Table 3, the appropriate outputs are driven to the minimum power state (LOW). With all outputs disabled, the power of the device is equal to its static dissipation of 200 mW.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system.

Table 3. Input Configuration

CTL0	CTL1	FUNCTION
0	0	All Outputs enabled
0	1	FC0 – FC4 enabled
1	0	FB0 – FB1 enabled
1	1	All outputs disabled

This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low), the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high) the outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 100 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for simulation results).

To lower noise and maintain signal fidelity, power and ground pins are carefully interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance +V_{CC} and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3529 will exhibit skews less than the specified maximum. A plastic 28-lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

Power Management

The overall goal of managing the power dissipated by the SC3529 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3529 is determined by the load that each output drives and the frequency that each output is running. Table 4 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit for complete load definition).

The individual output power must be summed and added to the static core power (250 mW) of the SC3529 to determine the total power being dissipated by the SC3529. This total power is then multiplied by the SC3529's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3529. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3529 is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3529 with 9 outputs driving 15 pF loads at 66 MHz. Total chip power is calculated as follows:

$$\begin{aligned} \text{Core Power} &= 250 \text{ mW} \\ 9 \text{ outputs, } 15 \text{ pF, } 66 \text{ MHz} &= (9 \times 55 \text{ mW}) = 495 \text{ mW} \\ 1 \text{ output, no load, } 66 \text{ MHz} &= (1 \times 16 \text{ mW}) = 16 \text{ mW} \\ \text{Total Power} &= 936 \text{ mW} \end{aligned}$$

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The SC3529's junction temperature would then be:

$$70^\circ\text{C} + (0.936 \text{ watts} \times 57.7^\circ\text{C/watt}) = 124^\circ\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 4. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

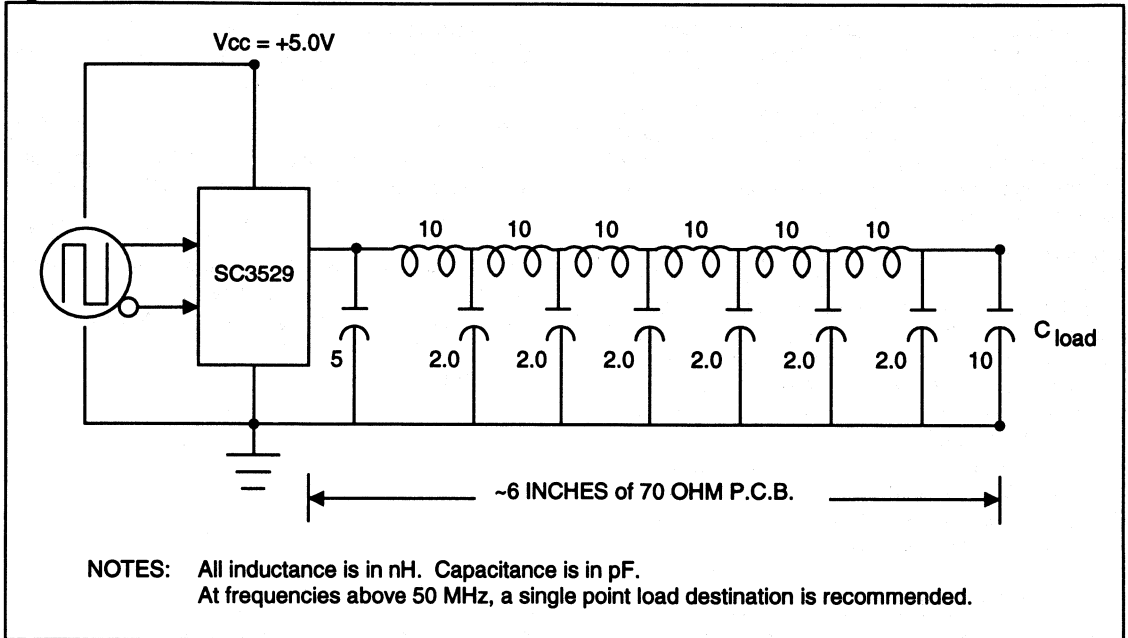
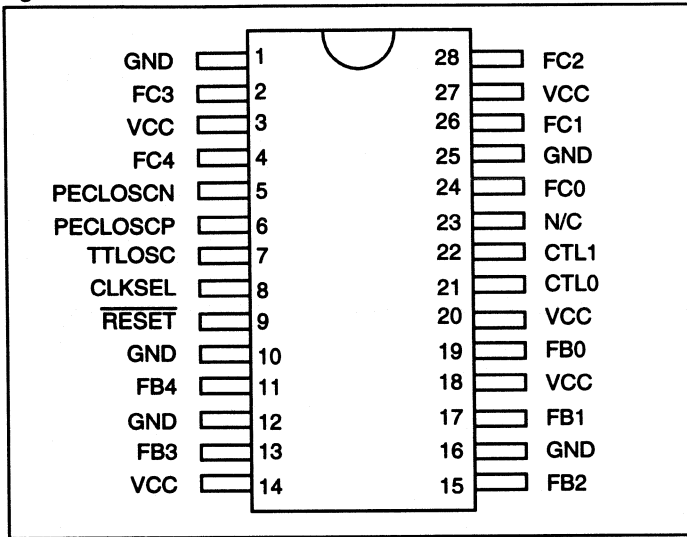
Figure 4. AC Test/Evaluation Circuit

Figure 5. SC3529 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Optional Shipping Configuration**

SC3529

S

/TD

Optional Shipping Configuration

Blank = 25-unit tube

/D = dry pack

/TD = tape, reel and dry pack

Package Option

S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: SC3529S/D

28-pin SOIC package, shipped dry packed in the standard tube.

FEATURES

- **20 clock outputs:**
 - Ten outputs at primary frequency, up to 80 MHz
 - Ten outputs at 1/2 primary frequency
- **All outputs are leading edge synchronized to within ≤ 0.5 ns**
- **Proprietary output drivers with:**
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 Ω source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- **Output levels comply with JEDEC LVTTTL standard**
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

- **Datcom and Telecom networks**
- **Compatible with Intel's Pentium™ and P6 processors**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**

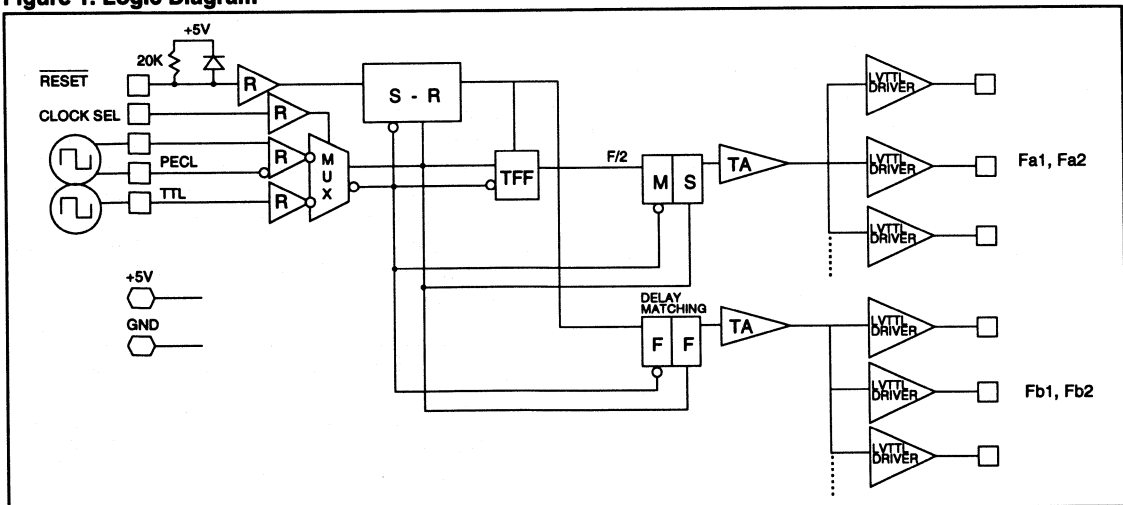
GENERAL DESCRIPTION

The SC3306 is a precision low skew clock driver with 20 outputs. It employs a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to symmetrical, divide-by-two, master-slave flip-flops. The resultant output is distributed to the clock output drivers. All outputs conform with JEDEC LVTTTL levels.

The 20 outputs are divided into two groups: group Fb is at the primary frequency, equal to the input; group Fa is at one half of the primary input frequency.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈ 1.5 V/ns to minimize simultaneous output-switching noise and distortion.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

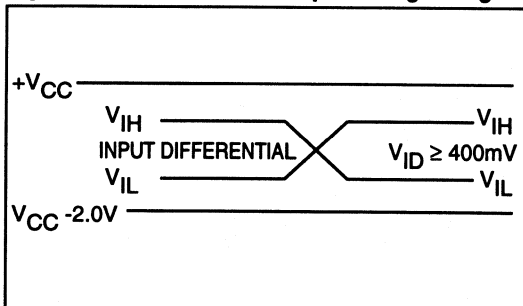
Input Pins	5.0 pF
TTL Output Pins	5.0 pF

Table 1. Electrical Characteristics

 V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source-PECL	V _{IL} +0.4	V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source-PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	µA
	CLKSEL	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 80MHz, C _L = 10pF	2.3	3.65	V
V _{OL}	Output LOW Voltage	F _{OUT} = 80MHz, C _L = 10pF		0.4V	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-45		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3 @ 70°C, Typ Pwr=370mW		600	mW

1. Maximum test duration, one second.
2. The SC3306 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range

DC Characteristics

The SC3306 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic “high-drive, totem-pole outputs” and AMCC’s dynamically adjusting source series terminated outputs. As a result of this, the SC3306 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -2mA	2.1V	
V _{OL}	I _{OL} = 2mA		0.6V

Table 2. AC Specifications—Using Figure 4, AC Test/Evaluation Circuit

$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10pF$

Parameter	SC3306-1	SC3306	Units
Maximum Skew Across All Outputs	0.5	1.0	ns
Maximum Skew Across Fa1 Outputs	0.25	0.25	ns
Maximum Skew Across Fa2 Outputs	0.25	0.25	ns
Maximum Skew Across Fb1 Outputs	0.25	0.25	ns
Maximum Skew Across Fb2 Outputs	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry @ 1.5V	± 1.0	± 1.0	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum Differential PECL Input Frequency	80	80	MHz
Maximum Rising/Falling Edge Rate	1.35/1.5	1.35/1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Output symmetry follows input symmetry for the 1X outputs.
3. Asymmetry is defined as the deviation from a 50% duty cycle measured at 1.5V. Asymmetry will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads. The maximum rising edge rate is specified at 5.0V and must be derated at 1.4ns/V for $V_{CC} < 5.0V$.
6. Parameters guaranteed by design and characterization or tested.

Figure 3. Threshold Crossing Characteristics

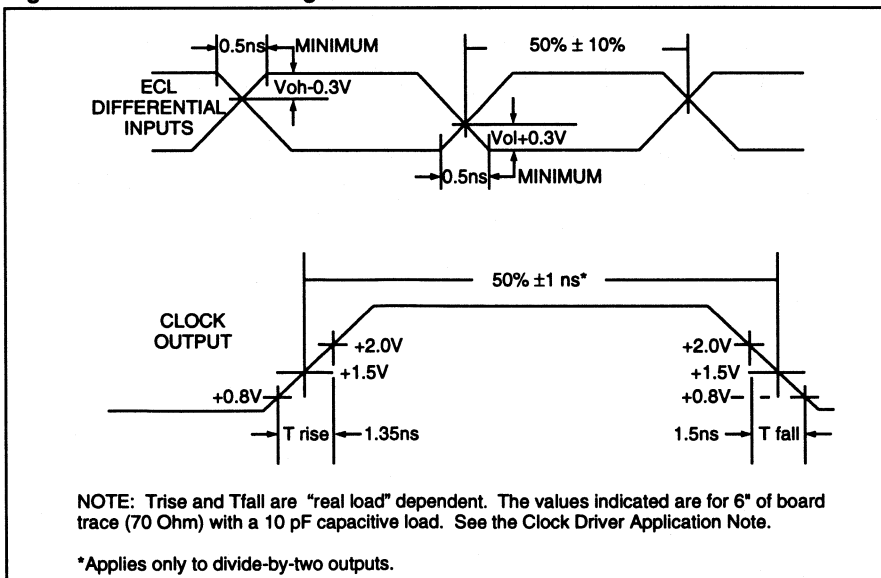


Figure 4. AC Test/Evaluation Circuit

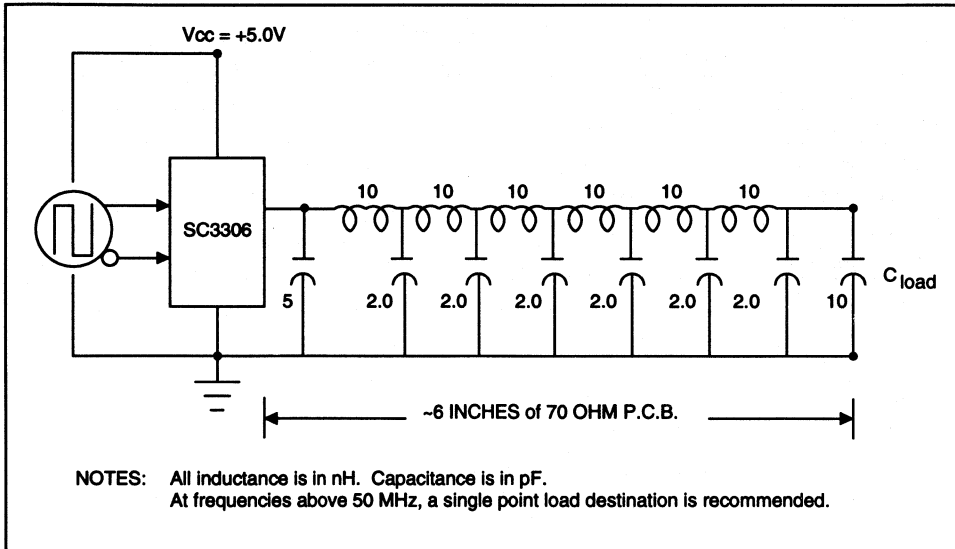
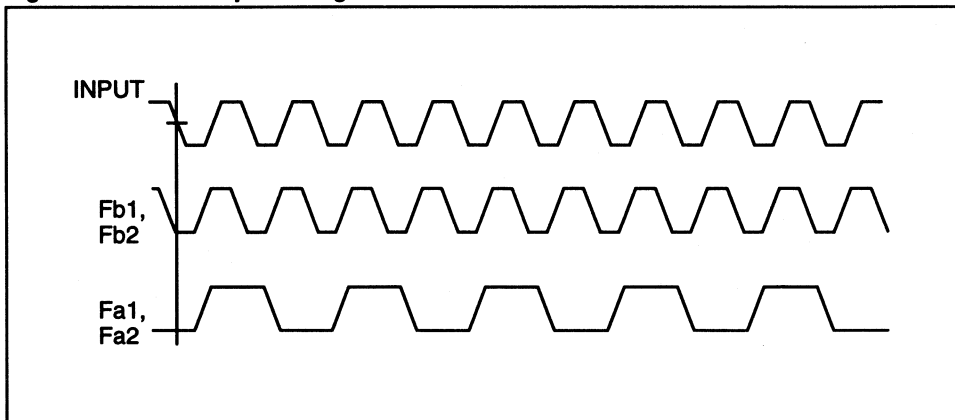


Figure 5. Relative Output Timing



DESCRIPTION OF OPERATION

(Refer to Logic Diagram)

AMCC has developed a twenty-output fan-out device using an advanced BiCMOS process. This design has been optimized for clock symmetry and absolute minimum skew across all twenty outputs. Two harmonic clock frequency groups are provided.

For highest performance this approach requires a clock source input from a crystal-controlled oscillator (XCO) located adjacent to the clock driver. This oscillator can provide either differential ECL inputs (referenced to +5V, PECL) or TTL (CMOS) input levels to the clock driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to a toggle flip-flop and to output flip-flops for synchronization, refer to Figure 1, Logic Diagram. Using this methodology, the output duty cycle for the F/2 or Fa group becomes largely a function of output driver slew rate into the AC load.

The Fb group duty cycle is governed by the input source clock. The output flip-flops are reset keyed for leading edge alignment. These outputs are amplified to fan out to AMCC's complementary source terminated LVTTTL output drivers.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor ($4.7\mu\text{F} = \sim 100\text{ ms}$) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling-edge clock inputs. At the expiration of RESET

(high) outputs will resume, after four falling-edge clock inputs, from a high (leading edge) count origin (see Figure 5, Reset To Output Timing, in the Clock Driver Application Note).

The output drivers are rise and fall slew rate controlled to $\sim 1.5\text{V/ns}$ to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance ($>25\text{pF}$ with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for Spice models).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneously switching outputs, low impedance $+V_{\text{CC}}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3306 will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

Power Management

The overall goal of managing the power dissipated by the SC3306 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3306 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The output power must be added to the core power (600 mW) of the SC3306 to determine the total power being dissipated by the SC3306. This total power is then multiplied by the SC3306's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3306. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3306 is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3306 with 8 Fb outputs driving 10 pF loads at 66 MHz, 3 Fa outputs driving 5 pF loads at 33 MHz and 2 Fa outputs driving 15 pF loads at 33 Mhz. Total chip power is calculated as follows:

Core Power	= 600 mW
8 Fb, 10 pF, 66 MHz = (8 x 33 mW)	= 264 mW
2 Fb, no load, 66 MHz = (2 x 11 mW)	= 22 mW
3 Fa1, 5 pF, 33 MHz = (3 x 13 mW)	= 39 mW
2 Fa1, no load, 33 MHz = (2 x 8 mW)	= 16 mW
2 Fa2, 15 pF, 33 MHz = (2 x 17 mW)	= 34 mW
3 Fa2, no load, 33 MHz = (3 x 8 mW)	= 24 mW
Total Power	= 999 mW

The design specifies a 70°C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2°C/watt. The SC3306's junction temperature would then be:

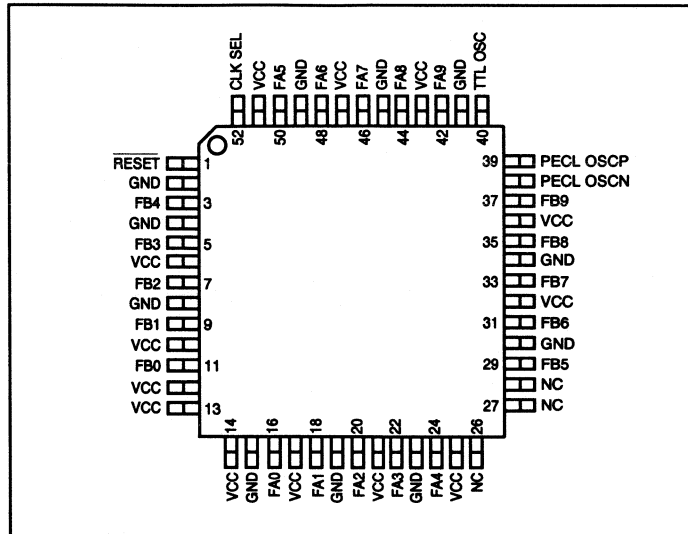
$$70^{\circ}\text{C} + (.999 \text{ watts} \times 46.2^{\circ}\text{C/watt}) = 116^{\circ}\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

Figure 6. SC3306 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC3306

Q

- 1

/TD

Optional Shipping Configuration

Blank = 84-unit matrix tray
/D = dry pack
/TD = tape, reel and dry pack

Skew Option

Blank = 1.0 ns output-output skew
- 1 = 500 ps output-output skew

Package Option

Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: SC3306Q-1/D

52-pin PQFP package, 500 ps output-output skew, shipped dry packed in the standard matrix tray.

FEATURES

- 20 clock outputs at primary frequency up to 80 MHz
- All outputs are leading edge synchronized to within ≤ 0.5 ns
- Proprietary output drivers with:
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 Ω source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- Output levels comply with JEDEC LVTTTL standard
- Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers

APPLICATIONS

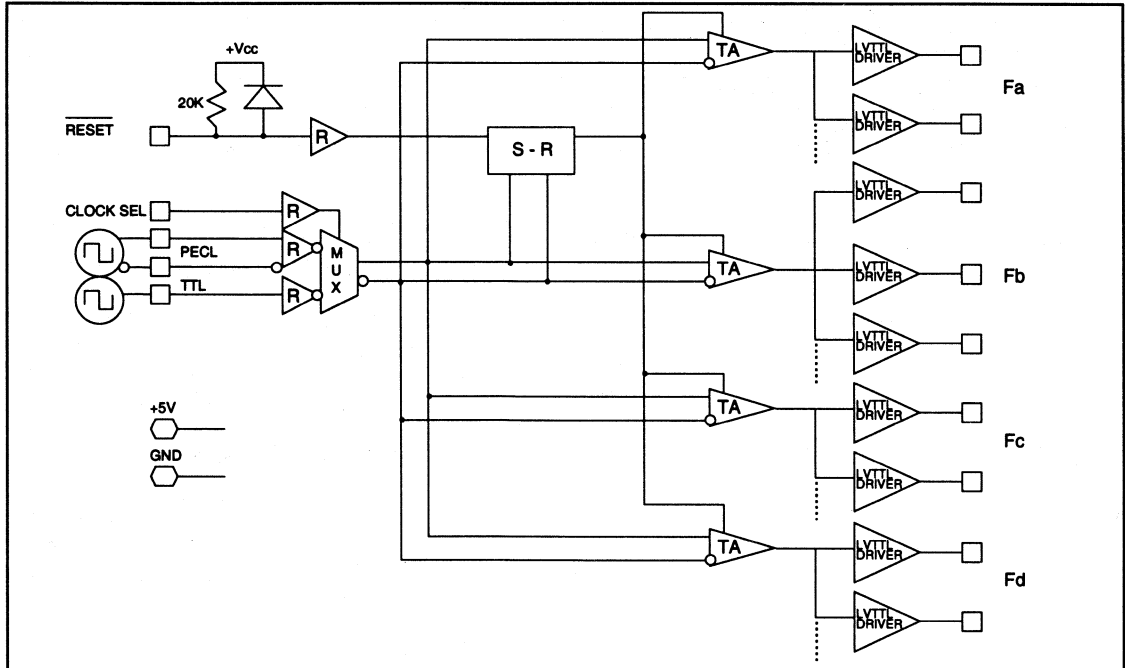
- Datacom and Telecom networks
- Compatible with Intel's Pentium™ and P6 processors
- PCI Bus clock distribution
- Workstation and server systems with high clock fanout

GENERAL DESCRIPTION

The SC3308 is a minimum skew clock driver with 20 outputs. It can employ a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to the clock output drivers. All outputs are "clamped" to conform with JEDEC LVTTTL levels.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise and distortion.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

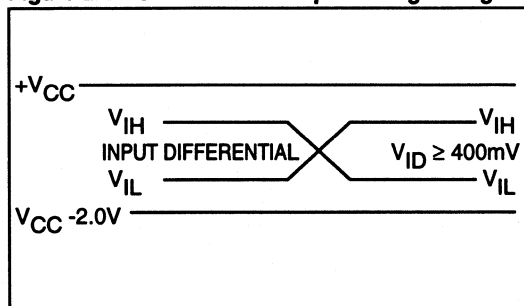
Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	µA
	CLKSEL	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 80MHz, C _L = 10pF	2.3	3.65	V
V _{OL}	Output LOW Voltage	F _{OUT} = 80MHz, C _L = 10pF		0.4V	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-45		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3 @ 70°C, Typ Pwr=370 mW		600	mW

1. Maximum test duration, one second.
2. The SC3308 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The SC3308 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic “high-drive, totem-pole outputs” and AMCC’s dynamically adjusting source series terminated outputs. As a result of this, the SC3308 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -2mA	2.1V	
V _{OL}	I _{OL} = 2mA		0.6V

Table 2. AC Specifications—Using Figure 4, AC Test/Evaluation Circuit

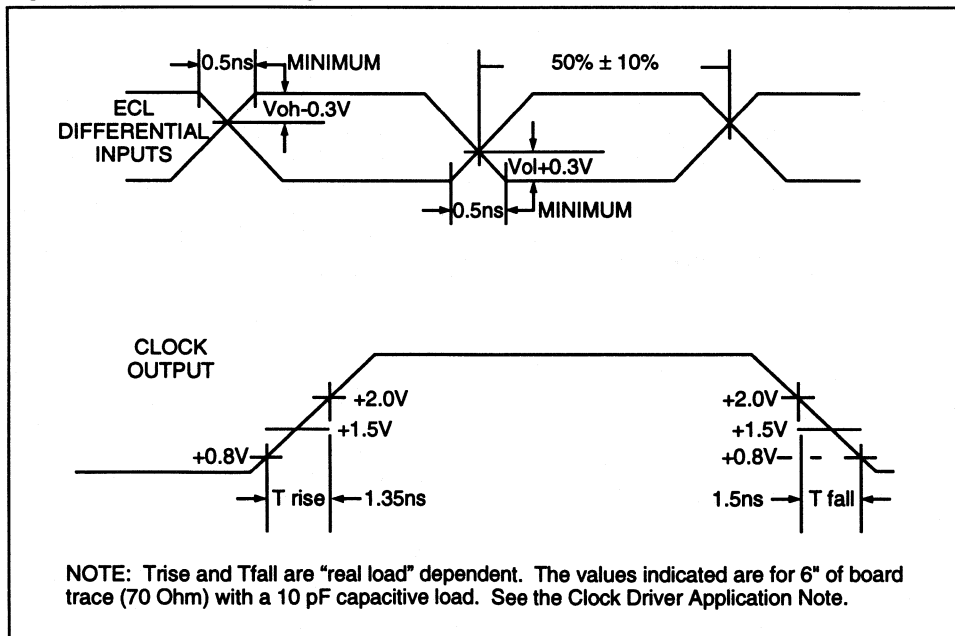
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $70^\circ C$, $C_{LOAD} = 10pF$

Parameter	SC3308-1	SC3308	Units
Maximum Skew Across All Outputs	0.5	1.0	ns
Maximum Skew Across Fa, Fb, Fc, or Fd Outputs	0.25	0.25	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum PECL Differential Input Frequency	80	80	MHz
Maximum Rising/Falling Edge Rate	1.35/1.5	1.35/1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. SC3308 output symmetry follows input symmetry. Output Duty Cycle will also be affected by voltage and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads. The maximum rising edge rate is specified for $V_{CC} = 5.0V$ and must be derated by 1.4ns/V for $V_{CC} < 5.0V$.
5. Parameters guaranteed by design and characterization or tested.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single-chip clock buffer and twenty-output fanout driver using AMCC's advanced BiCMOS process. This design has been optimized for absolute minimum skew across all twenty outputs.

For best performance, this approach will require a clock source input from a crystal-controlled oscillator (XCO) located adjacent to this clock driver. This oscillator can provide either differential ECL inputs (referenced to +5V, PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to translation amplifiers and output drivers, (refer to Figure 1, Logic Diagram). The output duty factor asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

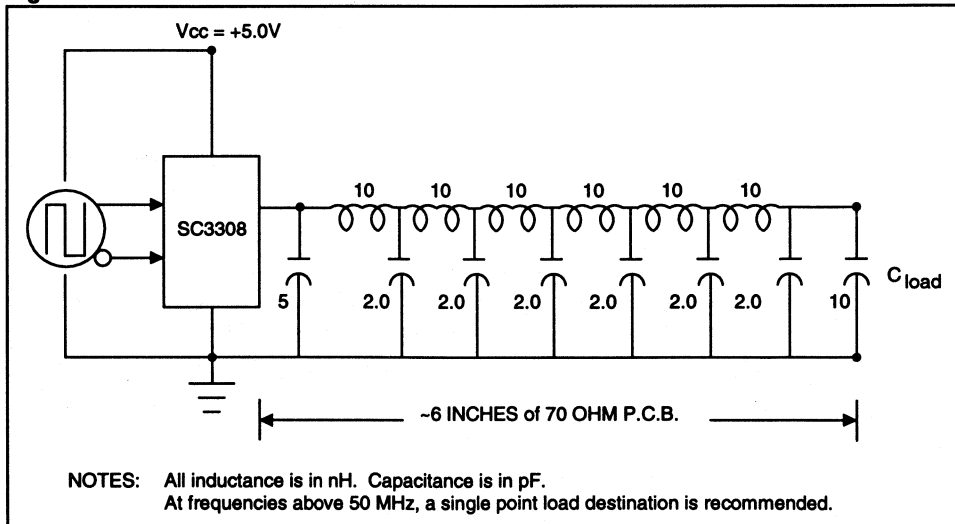
The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high) outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for spice models).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to simultaneously switching outputs, low impedance +V_{CC} and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3308 will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

Figure 4. AC Test/Evaluation Circuit



Power Management

The overall goal of managing the power dissipated by the SC3308 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3308 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The output power must be added to the core power (600 mW) of the SC3308 to determine the total power being dissipated by the SC3308. This total power is then multiplied by the SC3308's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3308. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3308 is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3308 with 12 outputs driving 15 pF loads at 50 MHz. Total chip power is calculated as follows:

$$\begin{aligned} \text{Core Power} &= 600 \text{ mW} \\ 12 \text{ outputs, } 15 \text{ pF, } 50 \text{ MHz} &= (12 \times 27 \text{ mW}) = 324 \text{ mW} \\ 8 \text{ outputs, no load, } 50 \text{ MHz} &= (8 \times 10 \text{ mW}) = 80 \text{ mW} \\ \text{Total Power} &= 1004 \text{ mW} \end{aligned}$$

The design specifies a 70°C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2°C/watt. The SC3308's junction temperature would then be:

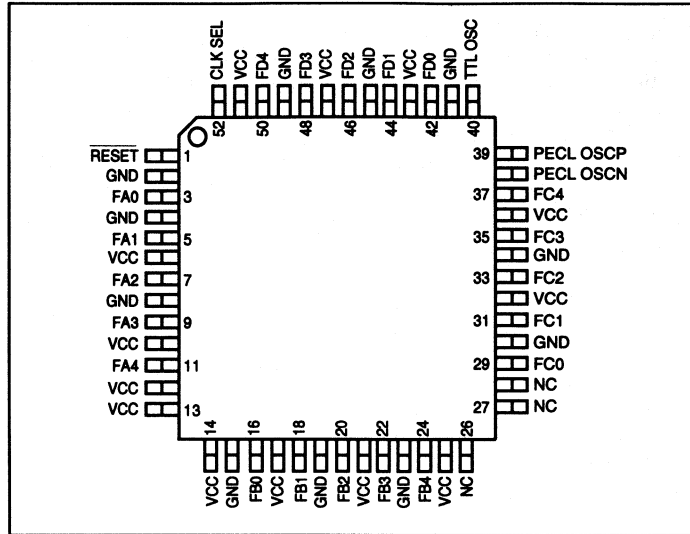
$$70^\circ\text{C} + (1.004 \text{ watts} \times 46.2^\circ\text{C/watt}) = 116^\circ\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

Figure 5. SC3308 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC3308

Q

- 1

/TD

Optional Shipping Configuration

Blank = 84-unit matrix tray

/D = dry pack

/TD = tape, reel and dry pack

Skew Option

Blank = 1.0 ns output-output skew

- 1 = 500 ps output-output skew

Package Option

Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: SC3308Q-1/D

52-pin PQFP package, 500 ps output-output skew, shipped dry packed in the standard matrix tray.

FEATURES

- Ten clock outputs at primary frequency up to 80 MHz
- All outputs are leading-edge synchronized to within ≤ 0.5 ns
- Proprietary output drivers with:
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 Ω source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- Output levels comply with JEDEC LVTTTL standard
- Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers

APPLICATIONS

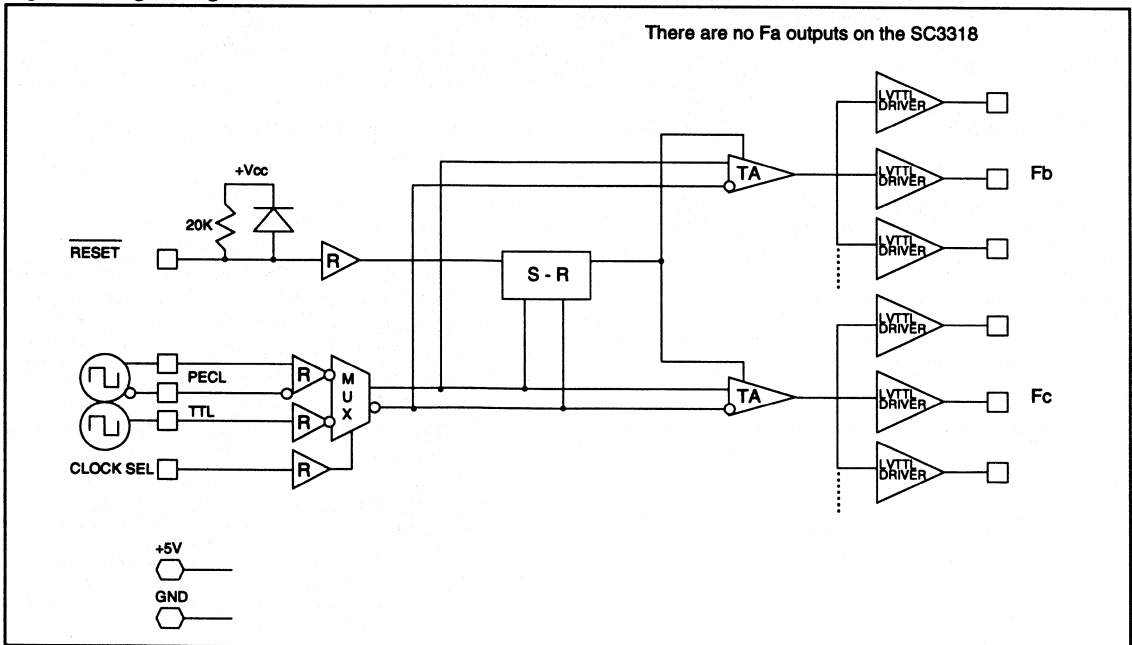
- Datacom and Telecom networks
- Compatible with Intel's Pentium™ and P6 processors
- PCI Bus clock distribution
- Workstation and server systems with high clock fanout

GENERAL DESCRIPTION

The SC3318 is a minimum skew clock driver with ten outputs. It can employ a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground. This reference frequency input is received and distributed to the clock output drivers. All outputs are "clamped" to conform with JEDEC LVTTTL levels.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈ 1.5 V/ns to minimize simultaneous output-switching noise and distortion.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

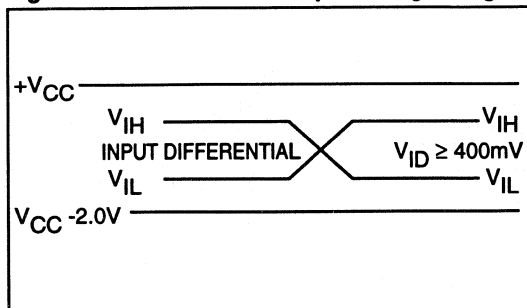
Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source-PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source-PECL	V _{CC} - 2.0	V _{IH} - 0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} - 2.0V		15	µA
	CLKSEL	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 80MHz, C _L = 10pF	2.3	3.65	V
V _{OL}	Output LOW Voltage	F _{OUT} = 80MHz, C _L = 10pF		0.4V	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-45		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3 @ 70°, Typ Pwr=340mW		550	mW

1. Maximum test duration, one second.
2. The SC3318 features source series termination of approximately 40 Ohms to assist in matching 50-75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The SC3318 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3318 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -2mA	2.1V	
V _{OL}	I _{OL} = 2mA		0.6V

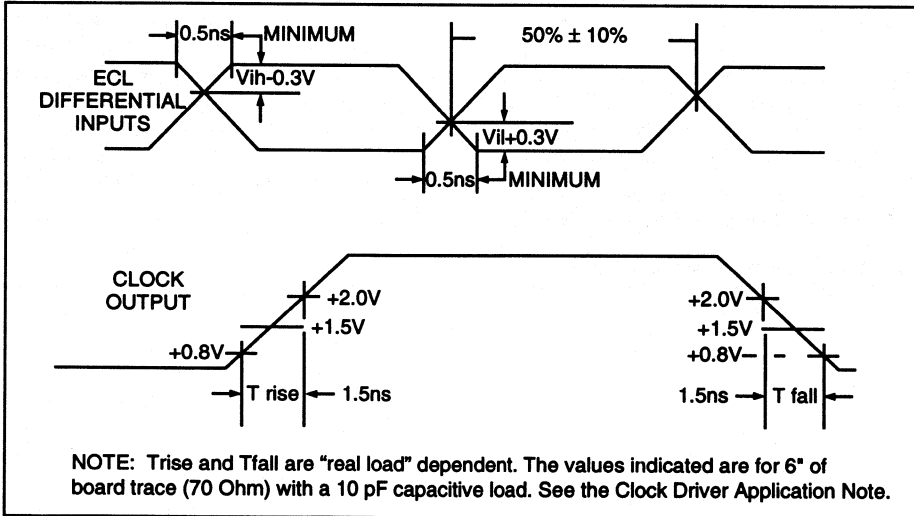
Table 2. AC Specifications—Using Figure 4, AC Test/Evaluation Circuit
 $V_{CC} = +5.0V \pm 5\%$, $T_a = 0^{\circ}C$ to $70^{\circ}C$, $C_{LOAD} = 10pF$

Parameter	SC3318-1	Units
Maximum Skew Across All Outputs	0.5	ns
Maximum Skew Across Fa or Fb Outputs	0.25	ns
Maximum TTL Input Frequency	80	MHz
Maximum Differential PECL Input Frequency	80	MHz
Maximum Rising/Falling Edge Rate	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The SC3318 output symmetry follows input symmetry. Output Duty Cycle will also be affected by voltage and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for high loads.
5. Parameters guaranteed by design and characterization or tested.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION

(Refer to Logic Diagram)

AMCC has developed a single-chip, ten-output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for absolute minimum skew across all ten outputs.

The clock source input for this device may operate between +5V and ground and can provide either differential ECL inputs (referenced to +5V, PECL) or single-ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL. This input clock will be fanned out to translation amplifiers and output drivers, refer to Figure 1, Logic Diagram. The output duty factor asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7 μ F = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low), the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high), the outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin.

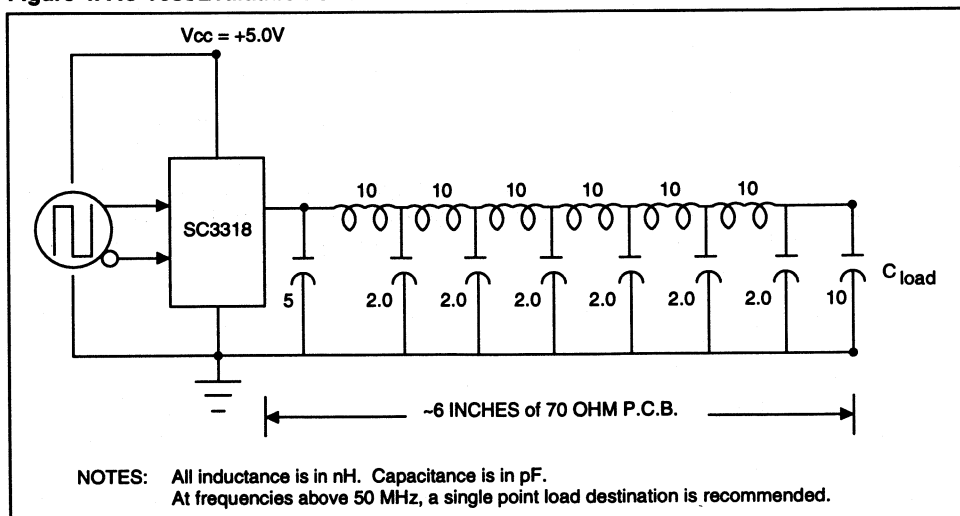
The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion

resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for spice models).

Power and ground are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance +V_{CC} and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3318 will exhibit skews less than the specified maximum. A plastic 28-lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

Figure 4. AC Test/Evaluation Circuit



Power Management

The overall goal of managing the power dissipated by the SC3318 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3318 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The output power must be added to the core power (550 mW) of the SC3318 to determine the total power being dissipated by the SC3318. This total power is then multiplied by the SC3318's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3318. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3318 is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3318 with 8 outputs driving 10 pF loads at 66 MHz. Total chip power is calculated as follows:

$$\begin{aligned} \text{Core Power} &= 550 \text{ mW} \\ 8 \text{ outputs, } 10 \text{ pF, } 66 \text{ MHz} &= (8 \times 33 \text{ mW}) = 264 \text{ mW} \\ 2 \text{ outputs, no load, } 66 \text{ MHz} &= (2 \times 11 \text{ mW}) = 22 \text{ mW} \\ \hline \text{Total Power} &= 836 \text{ mW} \end{aligned}$$

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The SC3318's junction temperature would then be:

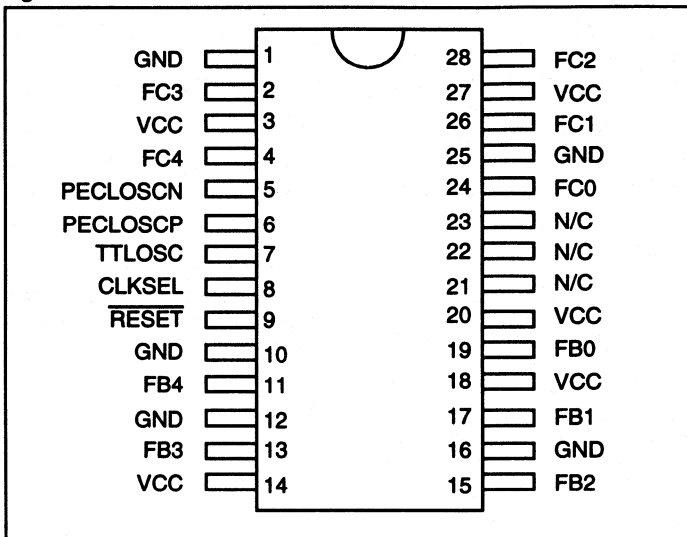
$$70^\circ\text{C} + (0.836 \text{ watts} \times 57.7^\circ\text{C/watt}) = 118^\circ\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

Figure 5. SC3318 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- Device Number
- Package Type
- Skew Option (if applicable)
- Optional Shipping Configuration

SC3318

S

-1

/TD

Optional Shipping Configuration

Blank = 25-unit tube

/D = dry pack

/T = tape, reel and dry pack

Skew Option

- 1 = 500 ps output-output skew

Package Option

S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: SC3318S-1/D

28-pin SOIC package, 500 ps output-output skew,
shipped dry packed in the standard tube.

FEATURES

- Three (3) clock outputs at primary reference frequency up to 80 Mhz
- Seven (7) clock outputs selectable at half primary reference frequency up to 40 Mhz, or at secondary reference frequency up to 80 Mhz
- Selectable single or dual reference frequencies
- Leading edge skew for all F_b outputs <700 ps
- Leading edge skew for all F_c outputs <500 ps
- Proprietary output drivers with:
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 Ω equivalent source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- Output levels compatible with JEDEC LVTTTL standard
- Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers
- Internal \approx 900 ps delay between F_c and F_b

APPLICATIONS

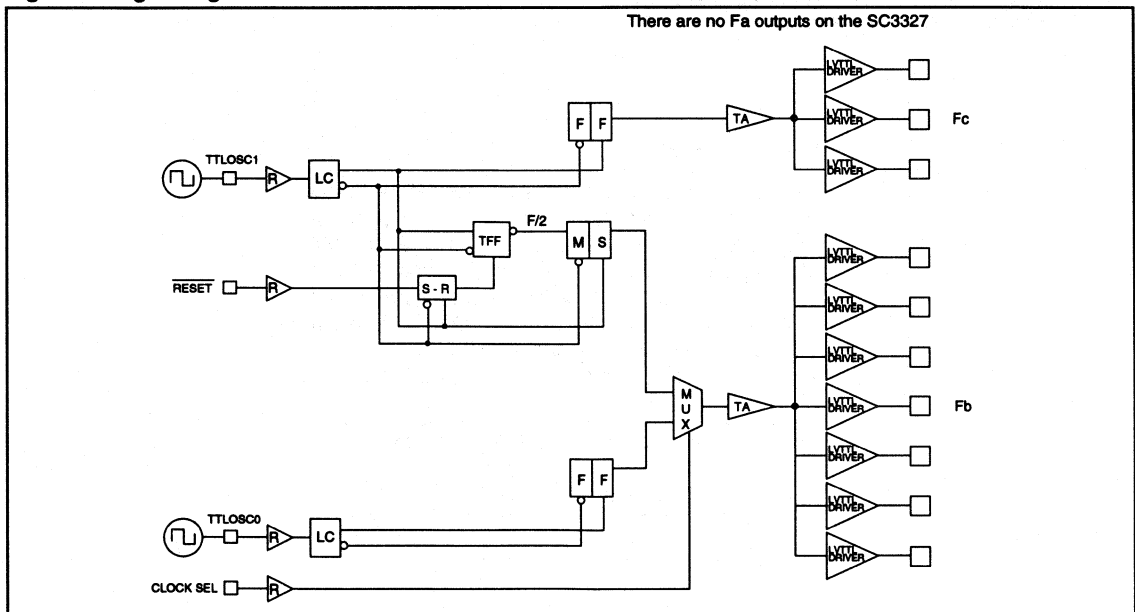
- Datacom and Telecom networks
- Compatible with Intel's Pentium™ and P6 processors
- PCI Bus clock distribution
- Workstation and server systems with high clock fanout

GENERAL DESCRIPTION

The SC3327 is a low skew clock driver with ten outputs. Three outputs operate at the primary reference frequency and seven outputs operate at either half the primary reference frequency or at the secondary reference frequency. A synchronous reset ensures proper phase of the half frequency outputs. It can employ clock input from either one or two single-ended TTL sources. These reference frequency inputs are received and distributed to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of \approx 1.5V/ns to minimize simultaneous output-switching noise, distortion, and EMI.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature -55° to +150°C
 V_{CC} Potential to Ground -0.5V to +7.0V
 Input Voltage -0.5V to +V_{CC}
 Static Discharge Voltage >1750V
 Maximum Junction Temperature +140°C
 Latch-up Current >200 mA
 Operating Ambient Temperature 0° to +70°C

Capacitance (package and die total)

Input Pins 5.0 pF
 TTL Output Pins 5.0 pF

Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTLOSCx	V _{IN} = 2.4V		15	µA
I _{IL}	CLKSEL	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTLOSCx	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 66MHz, C _L = 10pF	2.3V	3.6	V
V _{OL}	Output LOW Voltage	F _{OUT} = 66MHz, C _L = 10pF		0.4V	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-45		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3, Typ pwr=290mW		475	mW

1. Maximum test duration, one second.
2. The SC3327 features source series termination Ohms to assist in matching 50–75 Ohm P.C. board environments.

DC Characteristics

The SC3327 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic “high drive, totem pole outputs” and AMCC’s dynamically adjusting source series terminated outputs. As a result of this, the SC3327 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -2mA	2.1V	
V _{OL}	I _{OL} = 2mA		0.6V

Table 2. AC Specifications — Using Figure 4, AC Test/Evaluation Circuit

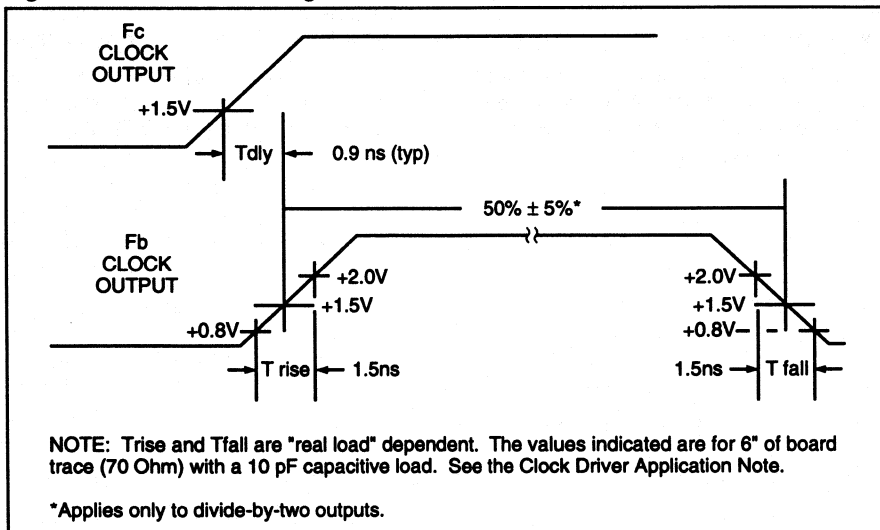
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10pF$
 (reference Figure 2, Threshold Crossing Characteristics)

Parameter	SC3327	Units
Maximum Skew Across Fb outputs	700	ps
Maximum Skew Across Fc outputs	500	ps
Delay of Fb from Fc outputs (CLKSEL = 1) [T _{dly}]	Minimum	50 ps
	Typical	0.9 ns
	Maximum	1.7 ns
Maximum Output Duty Cycle Asymmetry	Minimum	45 %
	Maximum	55 %
Maximum Rising/Falling Edge Rate [T _{rise} /T _{fall}]	1.5	ns
Maximum TTL Input Frequency	80	MHz
Maximum TTL Output Frequency	80	MHz

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The SC3327 output symmetry follows input symmetry for F_C outputs.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads. When $V_{CC} = 4.75V$, the maximum rising edge rate for the range $T_a = 0^\circ C$ to $15^\circ C$ is 1.7 ns. Table 2 is valid for all other conditions.
6. Parameters guaranteed by design and characterization or tested.

Figure 2. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION

(Refer to Logic Diagram)

AMCC has developed a single-chip ten-output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across outputs of the same frequency.

The clock source input for this device can select either one or two single-ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects the dual reference frequency mode, and logic HIGH selects the single reference frequency (TTLOSC1) mode. This input clock will be fanned out to translation amplifiers and output drivers (refer to the preceding logic diagram). The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

When the $\overline{\text{RESET}}$ input is held low (active), the FB0-6 outputs will be driven low. When $\overline{\text{RESET}}$ is de-asserted, the FB0-6 outputs will be active after a fixed three-input clock delay if the single-reference frequency mode is selected. The reset function is only operational when $\text{CLKSEL} = 1$.

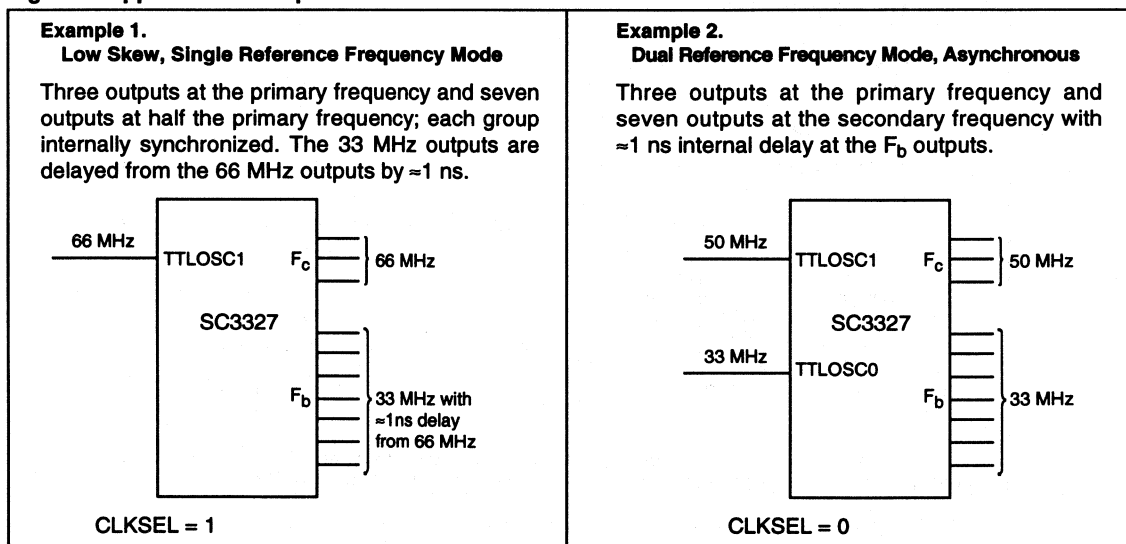
The output drivers are rise and fall slew rate controlled to $\sim 1.5\text{V/ns}$ to minimize noise and distortion resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot

of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance ($>25\text{pF}$ with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for simulation results).

To lower noise and maintain signal fidelity, power and ground pins are carefully interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3327 will exhibit skews less than the specified maximum. A plastic 28 lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

Figure 3. Application Examples



Power Management

The overall goal of managing the power dissipated by the SC3327 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3327 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit for complete load definition).

The individual output power must be added to the static core power (475 mW) of the SC3327 to determine the total power being dissipated by the SC3327. This total power is then multiplied by the SC3327's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3327. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3327 is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3327 with 3 outputs driving 10 pF loads at 66 MHz and 6 outputs driving 15 pF loads at 33 MHz. Total chip power is calculated as follows:

$$\begin{aligned} \text{Core Power} &= 475 \text{ mW} \\ 3 \text{ outputs, } 10 \text{ pF, } 66 \text{ MHz} &= (3 \times 33 \text{ mW}) = 99 \text{ mW} \\ 6 \text{ outputs, } 15 \text{ pF, } 33 \text{ MHz} &= (6 \times 17 \text{ mW}) = 102 \text{ mW} \\ 1 \text{ output, no load, } 33 \text{ MHz} &= (1 \times 8 \text{ mW}) = 8 \text{ mW} \\ \hline \text{Total Power} &= 684 \text{ mW} \end{aligned}$$

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The SC3327's junction temperature would then be:

$$70^\circ\text{C} + (.684 \text{ watts} \times 57.7^\circ\text{C/watt}) = 109^\circ\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

Figure 4. AC Test/Evaluation Circuit

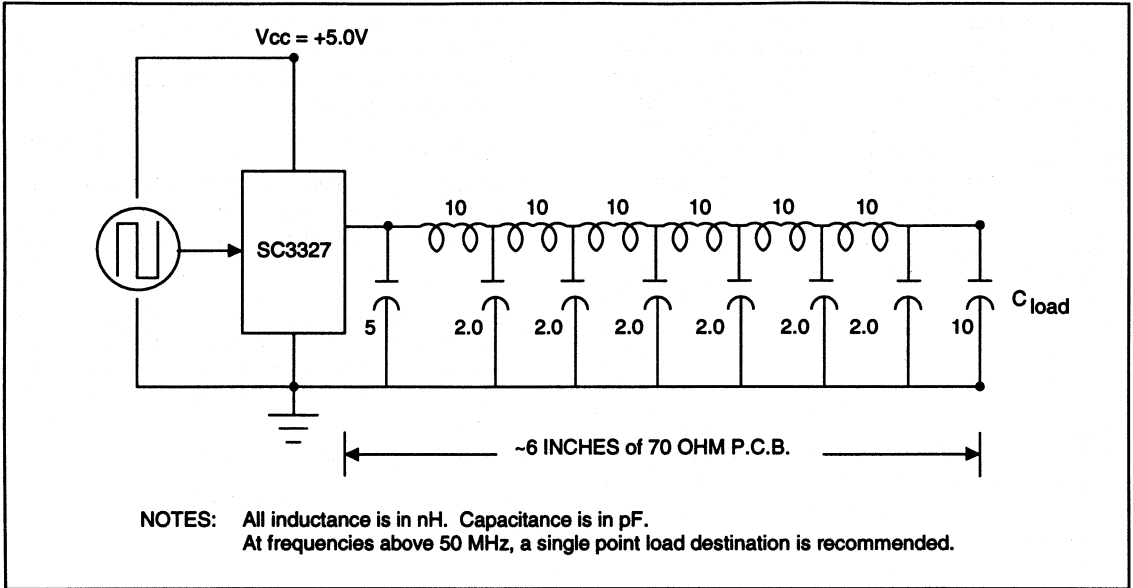
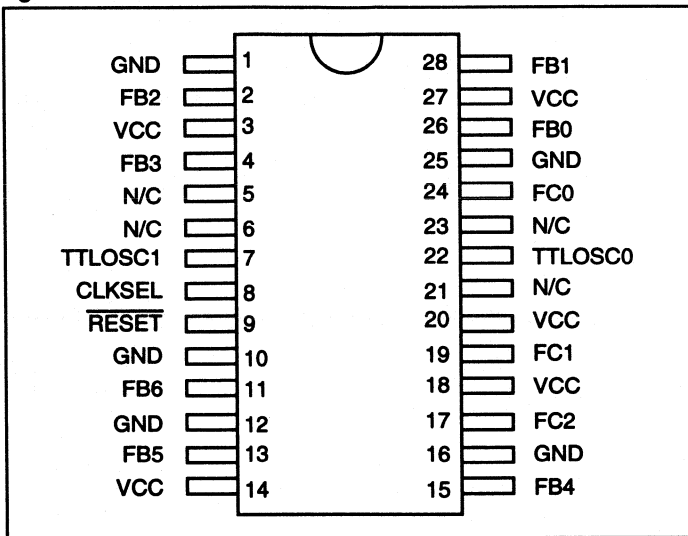


Figure 5. SC3327 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- Device Number
- Package Type
- Optional Shipping Configuration

SC3327

S

/TD

Optional Shipping Configuration

Blank = 25-unit tube

/D = dry pack

/TD = tape, reel and dry pack

Package Option

S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: SC3327S/D

28-pin SOIC package, shipped dry packed in the standard tube.

FEATURES

- Six clock outputs at primary reference frequency up to 80 Mhz
- One "early clock" output at primary reference to support PC chipsets
- Seven clock outputs selectable at half primary reference frequency up to 40 Mhz, or at secondary reference frequency up to 80 Mhz
- Selectable single or dual reference frequencies
- Leading edge skew for all F_D outputs <500 ps
- Leading edge skew for all F_C outputs <250 ps
- Proprietary output drivers with:
 - Complementary 24 mA peak outputs, source and sink
 - 50–75Ω equivalent source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- Output levels compatible with JEDEC LVTTTL standard
- Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers
- F_D output -6ns early

APPLICATIONS

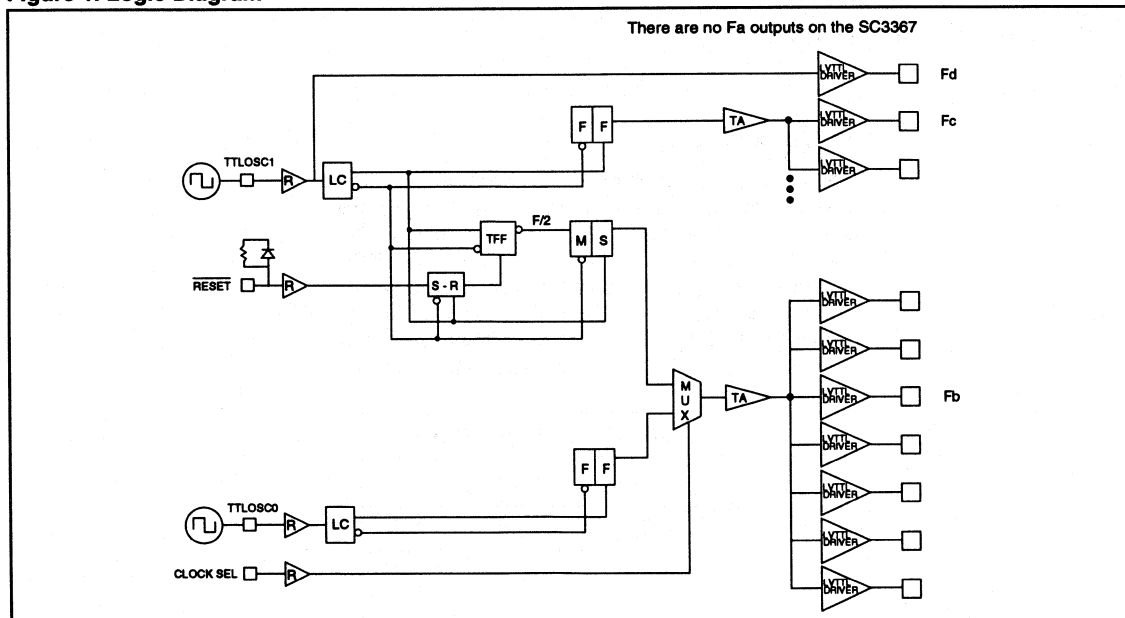
- Datacom and Telecom networks
- Compatible with Intel's Pentium™ and P6 processors
- PCI Bus clock distribution
- Workstation and server systems with high clock fanout

GENERAL DESCRIPTION

The SC3367 is a low skew clock driver with fourteen outputs. Seven outputs operate at the primary reference frequency and seven outputs operate at either half the primary reference frequency or at the secondary reference frequency. A synchronous reset ensures proper phase of the half frequency outputs. It can employ clock input from either one or two single-ended TTL sources. These reference frequency inputs are received and distributed to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise, distortion, and EMI.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTLOSCx	V _{IN} = 2.4V		15	µA
I _{IL}	CLKSEL	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTLOSCx	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 66MHz, C _L = 10pF	2.3V	3.6	V
V _{OL}	Output LOW Voltage	F _{OUT} = 66MHz, C _L = 10pF		0.4V	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-45		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3, Typ Pwr=250mW		400	mW

1. Maximum test duration, one second.
2. The SC3367 features source series termination Ohms to assist in matching 50–75 Ohm P.C. board environments.

DC Characteristics

The SC3367 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3367 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -2mA	2.1V	
V _{OL}	I _{OL} = 2mA		0.6V

Table 2. AC Specifications — Using Figure 4, AC Test/Evaluation Circuit

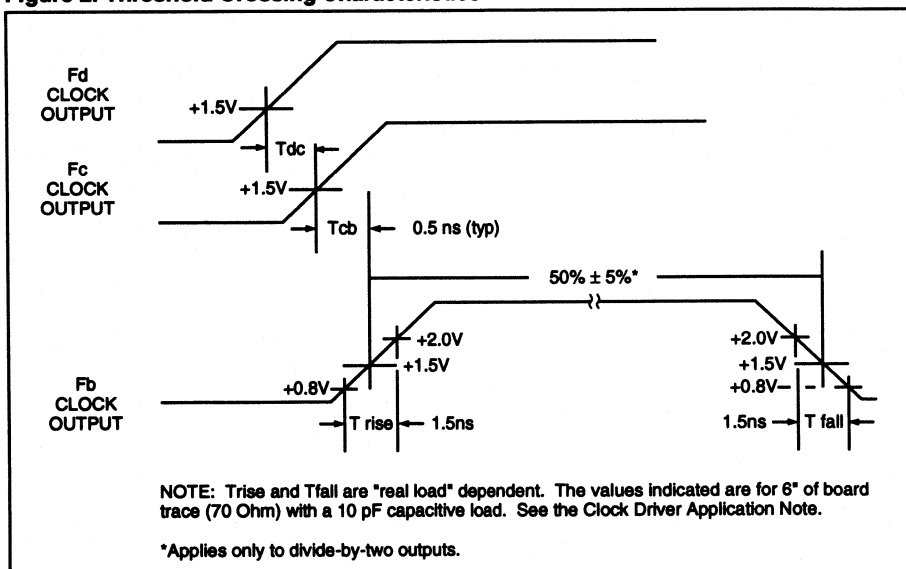
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10pF$
 (reference Figure 2, Threshold Crossing Characteristics)

Parameter 1	SC3367	Units
Maximum Skew Across Fb outputs	500	ps
Maximum Skew Across Fc outputs	250	ps
Maximum Skew Across Fb and Fc outputs, CLKSEL=0	500	ps
Delay of Fb from Fc outputs (CLKSEL = 1) [Tcb]	Minimum	50 ps
	Typical	500 ps
	Maximum	<1.0 ns
Delay of Fc from Fd output [Tdc]	Minimum	5 ps
	Typical	6 ps
	Maximum	7 ns
Maximum Output Duty Cycle Asymmetry (Fb outputs in divide-by-two mode)	Minimum	45 %
	Maximum	55 %
Maximum Rising/Falling Edge Rate (Trise/Tfall)	1.5	ns
Maximum TTL Input Frequency	80	MHz
Maximum TTL Output Frequency	80	MHz

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The SC3367 output symmetry follows input symmetry for all outputs except F_b in divide-by-two mode.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
6. Parameters guaranteed by design and characterization.

Figure 2. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single-chip fourteen-output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across outputs of the same frequency.

The clock source input for this device can select either one or two single-ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects the dual reference frequency mode, and logic HIGH selects the single reference frequency (TTLOSC1) mode. This input clock will be fanned out to translation amplifiers and output drivers (refer to the preceding logic diagram). The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

When the $\overline{\text{RESET}}$ input is held low (active), the FB0-7 outputs will be driven low. When $\overline{\text{RESET}}$ is de-asserted, the FB0-7 outputs will be active after a fixed three-input clock delay if the single-reference frequency mode is selected. The reset function is only operational when CLKSEL = 1.

The output drivers are rise and fall slew rate controlled to $\sim 1.5\text{V/ns}$ to minimize noise and distortion resulting from simultaneous switching of the 14 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot

of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance ($>25\text{pF}$ with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for simulation results).

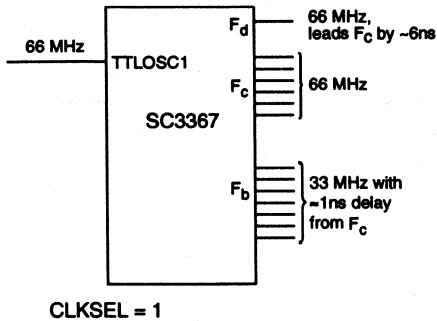
To lower noise and maintain signal fidelity, power and ground pins are carefully interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3367 will exhibit skews less than the specified maximum. A plastic 28 lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

Figure 3. Application Examples

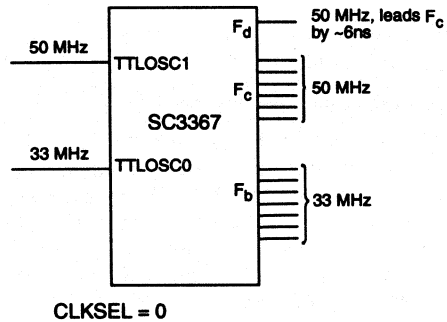
**Example 1.
Low Skew, Single Reference Frequency Mode**

Seven outputs at the primary frequency and seven outputs at half the primary frequency; each group internally synchronized. The 33 MHz outputs are delayed from the 66 MHz outputs by ≈ 1 ns. F_d will lead F_c by ≈ 6 ns.



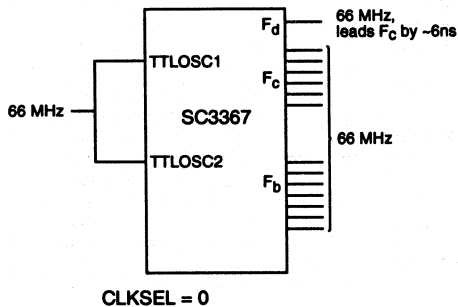
**Example 2.
Dual Reference Frequency Mode, Asynchronous**

Seven outputs at the primary frequency and eight outputs at the secondary frequency. F_d will lead F_c by ≈ 6 ns.



**Example 3.
Single Reference Frequency Mode, Synchronous**

Thirteen outputs will follow the input reference with a maximum skew of 500 ps across all outputs. F_d will lead F_c by ≈ 6 ns.



Power Management

The overall goal of managing the power dissipated by the SC3367 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3367 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit).

The individual output power must be added to the static core power (400 mW) of the SC3367 to determine the total power being dissipated by the SC3367. This total power is then multiplied by the SC3367's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3367. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3367 is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3367 with 5 outputs driving 10 pF loads at 66 MHz and 8 outputs driving 15 pF loads at 33 MHz. Total chip power is calculated as follows:

$$\begin{aligned} \text{Core Power} &= 400 \text{ mW} \\ 5 \text{ outputs, } 10 \text{ pF, } 66 \text{ MHz} &= (5 \times 33 \text{ mW}) = 165 \text{ mW} \\ 1 \text{ output, no load, } 66 \text{ MHz} &= (1 \times 11 \text{ mW}) = 11 \text{ mW} \\ 8 \text{ outputs, } 15 \text{ pF, } 33 \text{ MHz} &= (8 \times 17 \text{ mW}) = 136 \text{ mW} \\ \text{Total Power} &= 712 \text{ mW} \end{aligned}$$

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The SC3367's junction temperature would then be:

$$70^\circ\text{C} + (.712 \text{ watts} \times 57.7^\circ\text{C/watt}) = 111^\circ\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

Figure 4. AC Test/Evaluation Circuit

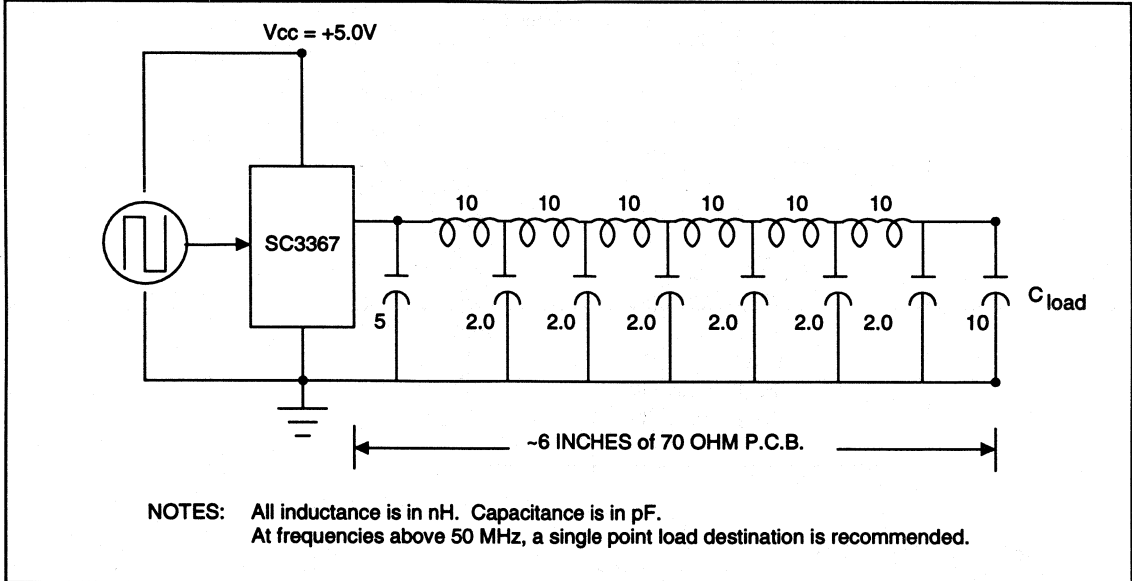
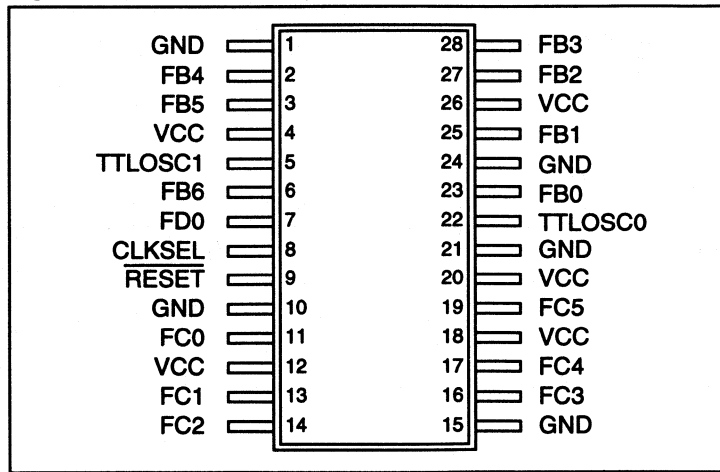


Figure 5. SC3367 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- Device Number
- Package Type
- Optional Shipping Configuration

SC3367

S

/TD

Optional Shipping Configuration

Blank = 25 unit tube

/D = dry pack

/TD = tape, reel and dry pack

Package Option

S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: SC3367S/TD

28-pin SOIC package, shipped tape, reeled and dry packed.

FEATURES

- Six clock outputs at primary reference frequency up to 80 Mhz
- Eight clock outputs selectable at half primary reference frequency up to 40 Mhz, or at secondary reference frequency up to 80 Mhz
- Selectable single or dual reference frequencies
- Leading edge skew for all F_b outputs <500 ps
- Leading edge skew for all F_c outputs <250 ps
- Proprietary output drivers with:
 - Complementary 24 mA peak outputs, source and sink
 - 50–75Ω equivalent source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- Output levels compatible with JEDEC LVTTTL standard
- Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers

APPLICATIONS

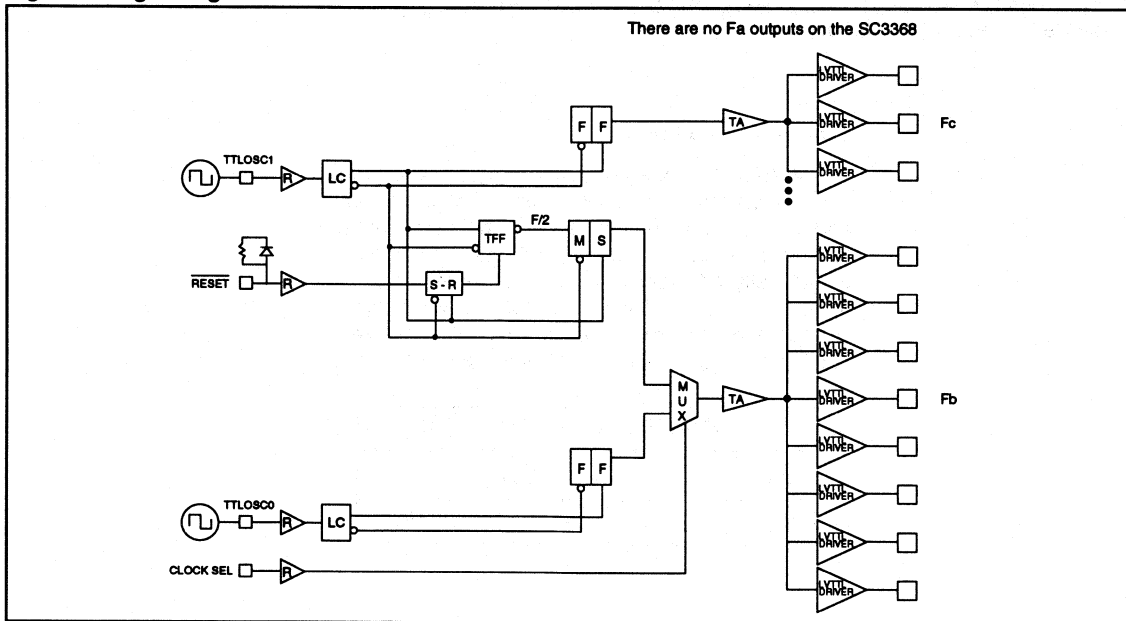
- Datacom and Telecom networks
- Compatible with Intel's Pentium™ and P6 processors
- PCI Bus clock distribution
- Workstation and server systems with high clock fanout

GENERAL DESCRIPTION

The SC3368 is a low skew clock driver with fourteen outputs. Six outputs operate at the primary reference frequency and eight outputs operate at either half the primary reference frequency or at the secondary reference frequency. A synchronous reset ensures proper phase of the half frequency outputs. It can employ clock input from either one or two single-ended TTL sources. These reference frequency inputs are received and distributed to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise, distortion, and EMI.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +7.0V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTLOSCx	V _{IN} = 2.4V		15	µA
I _{IL}	CLKSEL	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTLOSCx	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 66MHz, C _L = 10pF	2.3V	3.6	V
V _{OL}	Output LOW Voltage	F _{OUT} = 66MHz, C _L = 10pF		0.4V	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-45		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3, Typ Pwr=250mW		400	mW

1. Maximum test duration, one second.
2. The SC3368 features source series termination Ohms to assist in matching 50–75 Ohm P.C. board environments.

DC Characteristics

The SC3368 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3368 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -2mA	2.1V	
V _{OL}	I _{OL} = 2mA		0.6V

Table 2. AC Specifications — Using Figure 4, AC Test/Evaluation Circuit

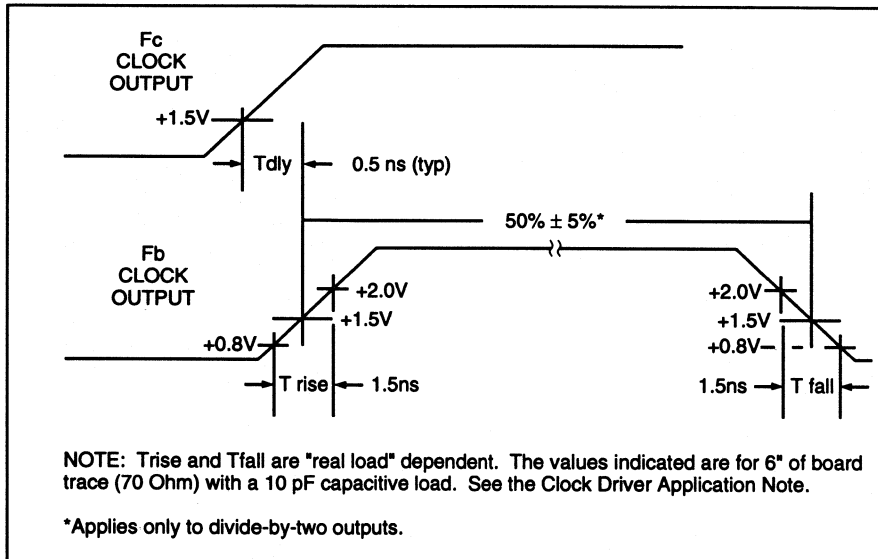
$V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10pF$
 (reference Figure 2, Threshold Crossing Characteristics)

Parameter	1	SC3368	Units
Maximum Skew Across Fb outputs		500	ps
Maximum Skew Across Fc outputs		250	ps
Maximum Skew Across Fb and Fc outputs, CLKSEL=0		500	ps
Delay of Fb from Fc outputs (CLKSEL = 1) [T _{dly}]	Minimum	50	ps
	Typical	500	ps
	Maximum	<1.0	ns
Maximum Output Duty Cycle Asymmetry	Minimum	45	%
	Maximum	55	%
Maximum Rising/Falling Edge Rate [Trise/Tfall]		1.5	ns
Maximum TTL Input Frequency		80	MHz
Maximum TTL Output Frequency		80	MHz

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The SC3368 output symmetry follows input symmetry for F_C outputs.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
6. Parameters guaranteed by design and characterization or tested.

Figure 2. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single-chip fourteen-output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across outputs of the same frequency.

The clock source input for this device can select either one or two single-ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects the dual reference frequency mode, and logic HIGH selects the single reference frequency (TTLOSC1) mode. This input clock will be fanned out to translation amplifiers and output drivers (refer to the preceding logic diagram). The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

When the $\overline{\text{RESET}}$ input is held low (active), the FB0-7 outputs will be driven low. When $\overline{\text{RESET}}$ is de-asserted, the FB0-7 outputs will be active after a fixed three-input clock delay if the single-reference frequency mode is selected. The reset function is only operational when CLKSEL = 1.

The output drivers are rise and fall slew rate controlled to $\sim 1.5\text{V/ns}$ to minimize noise and distortion resulting from simultaneous switching of the 14 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot

of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance ($>25\text{pF}$ with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for simulation results).

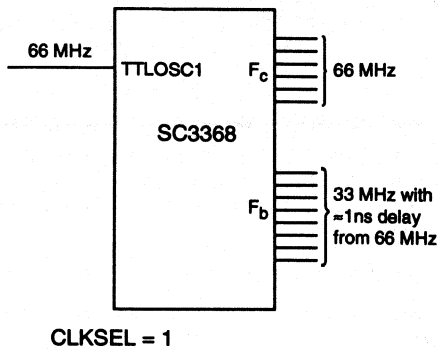
To lower noise and maintain signal fidelity, power and ground pins are carefully interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{\text{CC}}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the SC3368 will exhibit skews less than the specified maximum. A plastic 28 lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

Figure 3. Application Examples

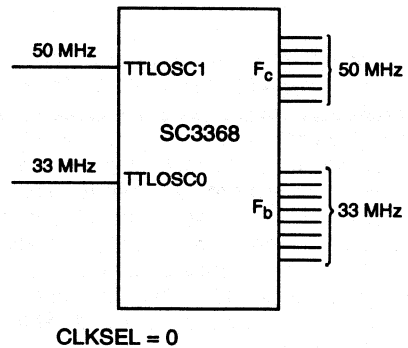
**Example 1.
Low Skew, Single Reference Frequency Mode**

Six outputs at the primary frequency and eight outputs at half the primary frequency; each group internally synchronized. The 33 MHz outputs are delayed from the 66 MHz outputs by ≈ 1 ns.



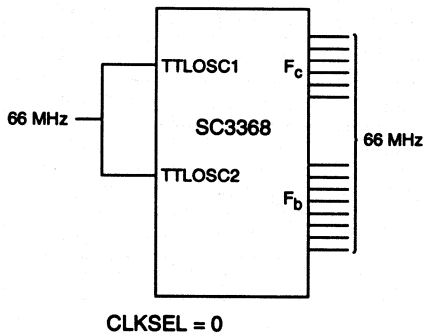
**Example 2.
Dual Reference Frequency Mode, Asynchronous**

Six outputs at the primary frequency and eight outputs at the secondary frequency.



**Example 3.
Single Reference Frequency Mode, Synchronous**

All fourteen outputs will follow the input reference with a maximum skew of 500 ps across all outputs.



Power Management

The overall goal of managing the power dissipated by the SC3368 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3368 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit).

The individual output power must be added to the static core power (400 mW) of the SC3368 to determine the total power being dissipated by the SC3368. This total power is then multiplied by the SC3368's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3368. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3368 is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3368 with 5 outputs driving 10 pF loads at 66 MHz and 8 outputs driving 15 pF loads at 33 MHz. Total chip power is calculated as follows:

$$\begin{aligned} \text{Core Power} &= 400 \text{ mW} \\ 5 \text{ outputs, } 10 \text{ pF, } 66 \text{ MHz} &= (5 \times 33 \text{ mW}) = 165 \text{ mW} \\ 1 \text{ output, no load, } 66 \text{ MHz} &= (1 \times 11 \text{ mW}) = 11 \text{ mW} \\ 8 \text{ outputs, } 15 \text{ pF, } 33 \text{ MHz} &= (8 \times 17 \text{ mW}) = 136 \text{ mW} \\ \text{Total Power} &= 712 \text{ mW} \end{aligned}$$

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The SC3368's junction temperature would then be:

$$70^\circ\text{C} + (.712 \text{ watts} \times 57.7^\circ\text{C/watt}) = 111^\circ\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

Figure 4. AC Test/Evaluation Circuit

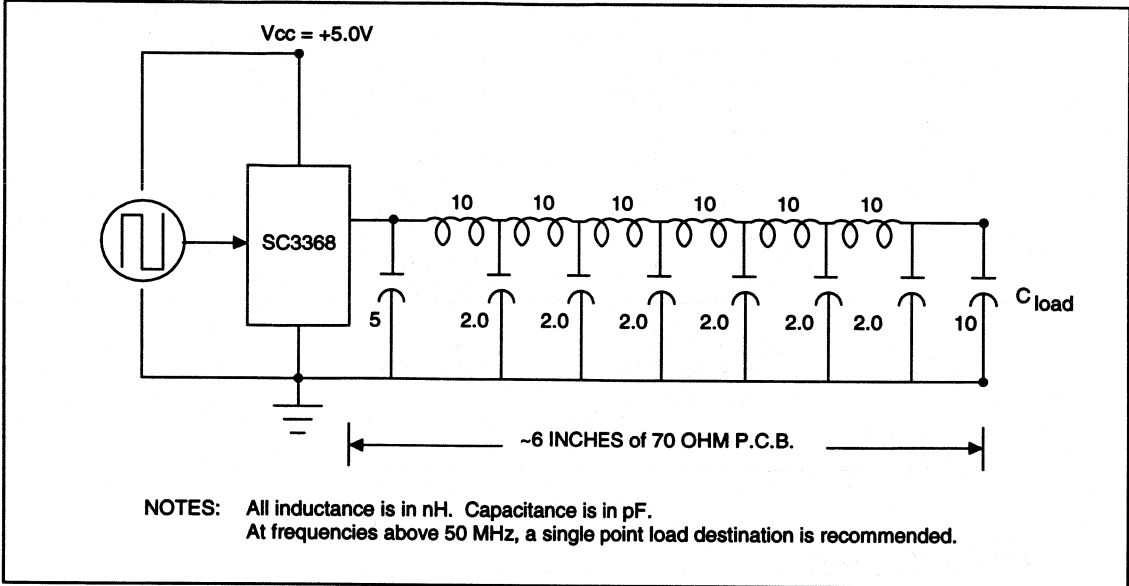
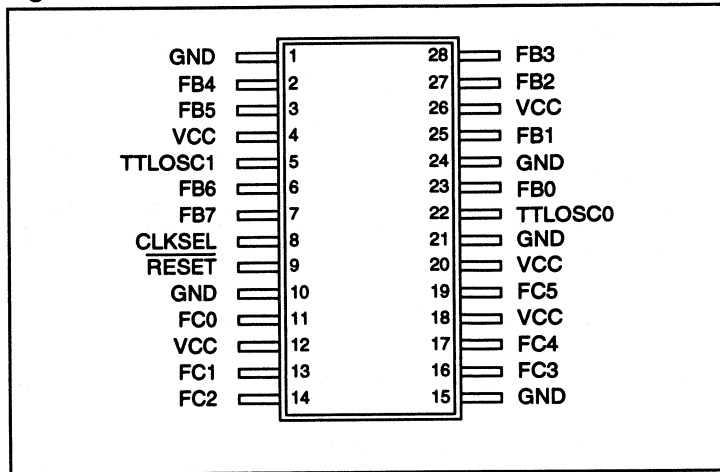


Figure 5. SC3368 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- Device Number
- Package Type
- Optional Shipping Configuration

SC3368

S

/TD

Optional Shipping Configuration
 Blank = 25 unit tube
 /D = dry pack
 /TD = tape, reel and dry pack

Package Option
 S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: SC3368S/D
 28-pin SOIC package, shipped dry packed in the standard tube.

FEATURES

- **20 clock outputs:**
 - Ten outputs at primary frequency, up to 100 MHz
 - Ten outputs at 1/2 primary frequency
- **All outputs are leading edge synchronized to within ≤ 0.5 ns**
- **Proprietary output drivers with:**
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 Ω source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- **Output levels comply with JEDEC LVTTTL standard**
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

- **Datacom and Telecom networks**
- **Compatible with Intel's Pentium™ and P6 processors**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**

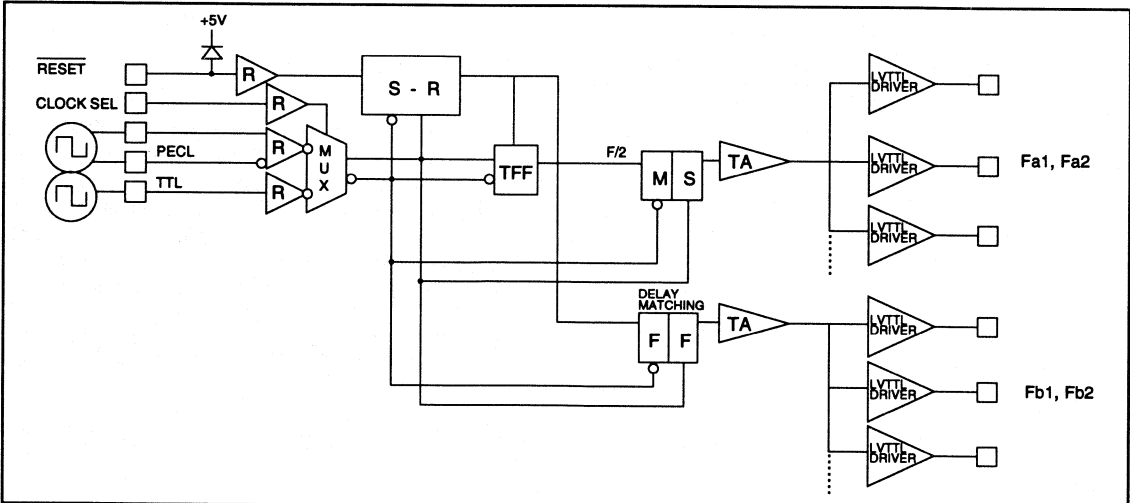
GENERAL DESCRIPTION

The S3LV306 is a precision low skew clock driver with 20 outputs. It employs a clock input from a single-ended TTL or an ECL differential source operating between +3.3V and ground (PECL). This reference frequency input is received and distributed to symmetrical, divide-by-two, master-slave flip-flops. The resultant output is distributed to the clock output drivers. All outputs conform with JEDEC LVTTTL levels.

The 20 outputs are divided into two groups: group Fb is at the primary frequency, equal to the input; group Fa is at one half of the primary input frequency.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise and distortion.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +4.6V
Input Voltage	-0.5V to +V _{CC} +0.5
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

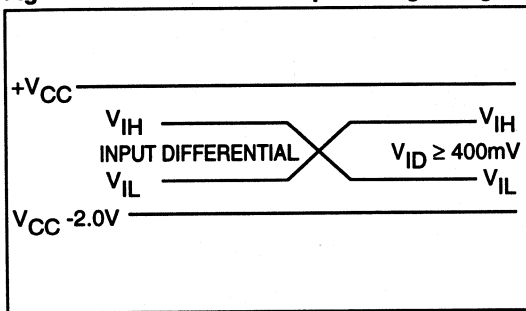
Table 1. Electrical Characteristics

V_{CC} = 3.3V ±0.3V, T_a = 0°C to +70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source-PECL	V _{IL} +0.4	V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source-PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	µA
	CLKSEL	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 100MHz, C _L = 10pF	2.4	V _{CC} +0.3V	V
V _{OL}	Output LOW Voltage	F _{OUT} = 100MHz, C _L = 10pF		0.4V	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3 @ 70°C, Typ Pwr 275 mW		450	mW

1. Maximum test duration, one second.
2. The S3LV306 features source series termination of approximately 40 Ohms to assist in matching 50-75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The S3LV306 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the S3LV306 will dynamically adjust source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -2mA	2.4V	
V _{OL}	I _{OL} = 2mA		0.4V

Table 2. AC Specifications—Using Figure 4, AC Test/Evaluation Circuit

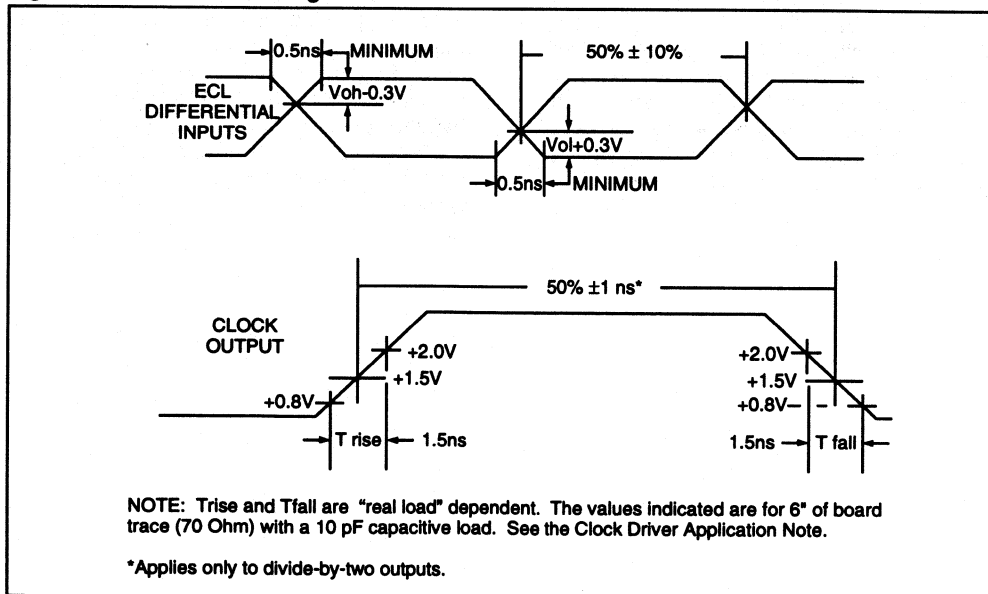
$V_{CC} = 3.3V \pm 0.3V$, $T_a = 0^\circ C$ to $+70^\circ C$, $C_{LOAD} = 10pF$

Parameter	S3LV306-1	Units
Maximum Skew Across All Outputs	0.5	ns
Maximum Skew Across Fa1 Outputs	0.25	ns
Maximum Skew Across Fa2 Outputs	0.25	ns
Maximum Skew Across Fb1 Outputs	0.25	ns
Maximum Skew Across Fb2 Outputs	0.25	ns
Maximum Output Duty Cycle Asymmetry @ 1.5V	± 1.0	ns
Maximum TTL Input Frequency	100	MHz
Maximum Differential PECL Input Frequency	100	MHz
Maximum Rising/Falling Edge Rate	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Output symmetry follows input symmetry for the 1X outputs.
3. Asymmetry is defined as the deviation from a 50% duty cycle measured at 1.5V. Asymmetry will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
6. Parameters guaranteed by design and characterization or tested.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION

(Refer to Logic Diagram)

AMCC has developed a twenty-output fan-out device using an advanced BiCMOS process. This design has been optimized for clock symmetry and absolute minimum skew across all twenty outputs. Two harmonic clock frequency groups are provided.

For highest performance this approach requires a clock source input from a crystal-controlled oscillator (XCO) located adjacent to the clock driver. This oscillator can provide either differential ECL inputs (referenced to +3.3V, PECL) or TTL (CMOS) input levels to the clock driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to a toggle flip-flop and to output flip-flops for synchronization, refer to Figure 1, Logic Diagram. Using this methodology, the output duty cycle for the F/2 or Fa group becomes largely a function of output driver slew rate into the AC load.

The Fb group duty cycle is governed by the input source clock. The output flip-flops are reset keyed for leading edge alignment. These outputs are amplified to fan out to AMCC's complementary source terminated LVTTTL output drivers.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor ($4.7\mu\text{F} = \sim 100\text{ ms}$) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling-edge clock inputs. At the expiration of RESET

(high) outputs will resume, after four falling-edge clock inputs, from a high (leading edge) count origin (see Figure 5, Reset To Output Timing, in the Clock Driver Application Note).

The output drivers are rise and fall slew rate controlled to $\sim 1.5\text{V/ns}$ to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance ($>25\text{pF}$ with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for Spice models).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneously switching outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the S3LV306 will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

Power Management

The overall goal of managing the power dissipated by the S3LV306 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the S3LV306 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The output power must be added to the core power (450 mW) of the S3LV306 to determine the total power being dissipated by the S3LV306. This total power is then multiplied by the S3LV306's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the S3LV306. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the S3LV306 is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an S3LV306 with 8 Fb outputs driving 10 pF loads at 66 MHz, 3 Fa outputs driving 5 pF loads at 33 MHz and 2 Fa outputs driving 15 pF loads at 33 Mhz. Total chip power is calculated as follows:

Core Power	=	450 mW
8 Fb, 10 pF, 66 MHz = (8 x 33 mW)	=	376 mW
2 Fb, no load, 66 MHz = (2 x 11 mW)	=	22 mW
3 Fa1, 5 pF, 33 MHz = (3 x 13 mW)	=	39 mW
2 Fa1, no load, 33 MHz = (2 x 8 mW)	=	16 mW
2 Fa2, 15 pF, 33 MHz = (2 x 17 mW)	=	34 mW
3 Fa2, no load, 33 MHz = (3 x 8 mW)	=	24 mW
Total Power		= 961 mW

The design specifies a 70°C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2°C/watt. The S3LV306's junction temperature would then be:

$$70^{\circ}\text{C} + (.961 \text{ watts} \times 46.2^{\circ}\text{C/watt}) = 114^{\circ}\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
100 MHz	33 mW	39 mW	47 mW	70 mW	15 mW
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

Figure 4. AC Test/Evaluation Circuit

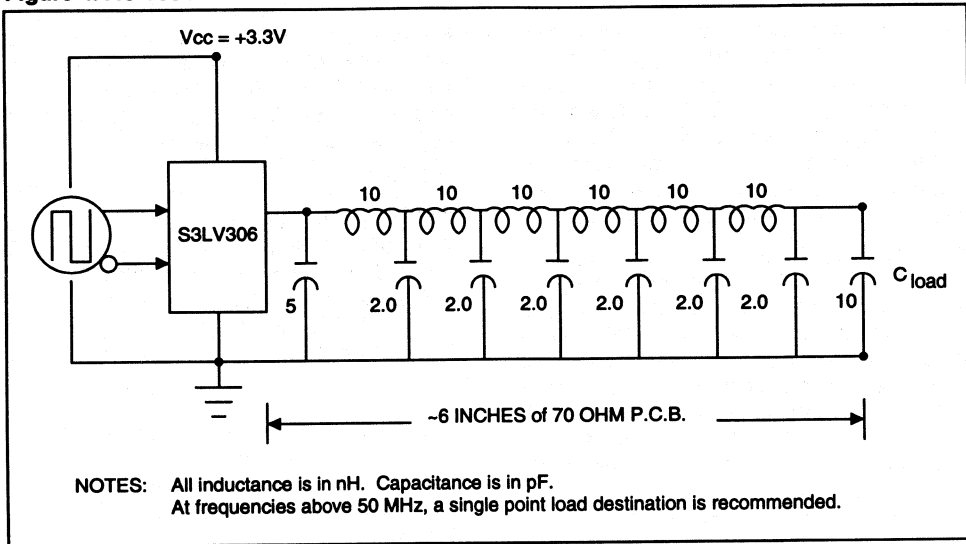


Figure 5. Relative Output Timing

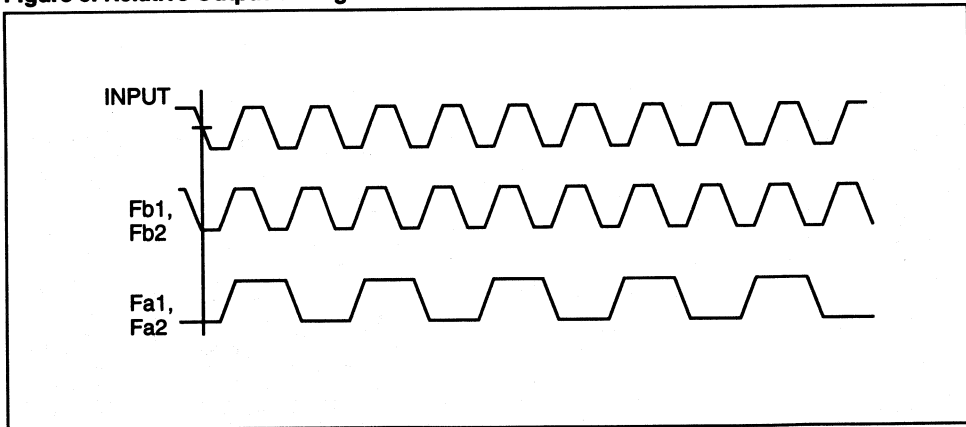
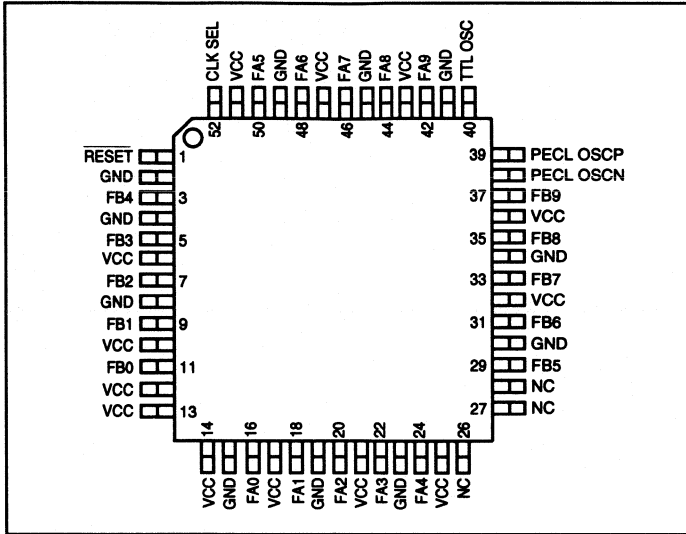


Figure 6. S3LV306 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

S3LV306

Q

-1

/TD

Optional Shipping Configuration

Blank = 84-unit matrix tray

/D = dry pack

/TD = tape, reel and dry pack

Skew Option

Blank = 1.0 ns output-output skew

- 1 = 500 ps output-output skew

Package Option

Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: S3LV306Q-1/D

52-pin PQFP package, 500 ps output-output skew, shipped dry packed in the standard matrix tray.

FEATURES

- 20 clock outputs at primary frequency up to 100 MHz
- All outputs are leading edge synchronized to within ≤ 0.5 ns
- Proprietary output drivers with:
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 Ω source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- Output levels comply with JEDEC LVTTTL standard
- Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers

APPLICATIONS

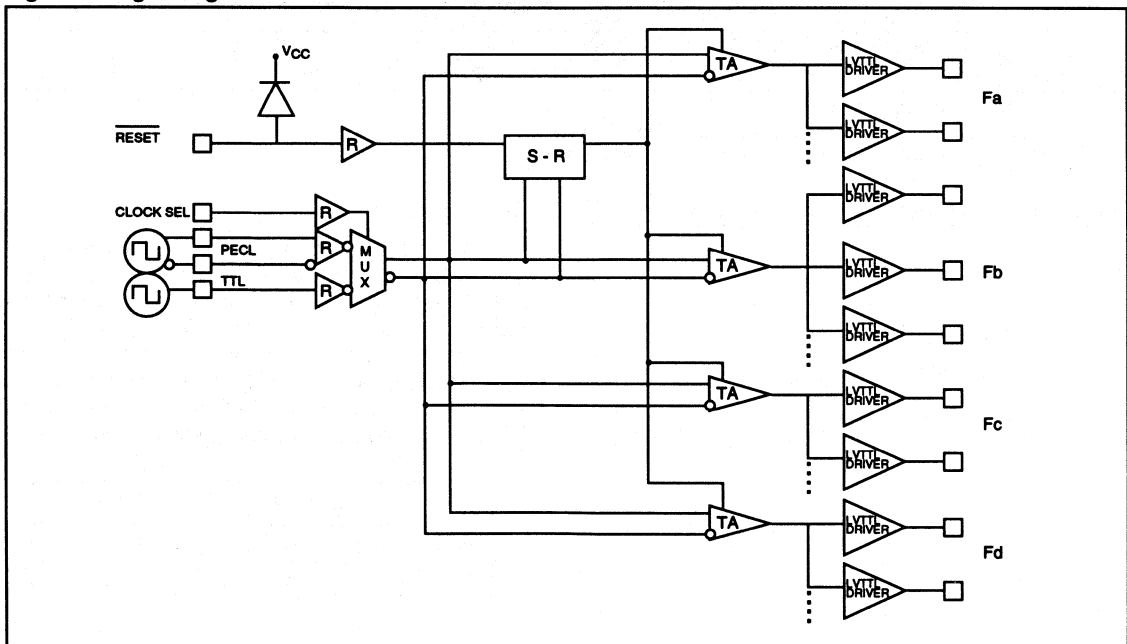
- Datacom and Telecom networks
- Compatible with Intel's Pentium™ and P6 processors
- PCI Bus clock distribution
- Workstation and server systems with high clock fanout

GENERAL DESCRIPTION

The S3LV308 is a minimum skew clock driver with 20 outputs. It can employ a clock input from a single-ended TTL or an ECL differential source operating between +3.3V and ground (PECL). This reference frequency input is received and distributed to the clock output drivers. All outputs conform with JEDEC LVTTTL levels.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise and distortion.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +4.6V
Input Voltage	-0.5V to +V _{CC} +0.5V
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

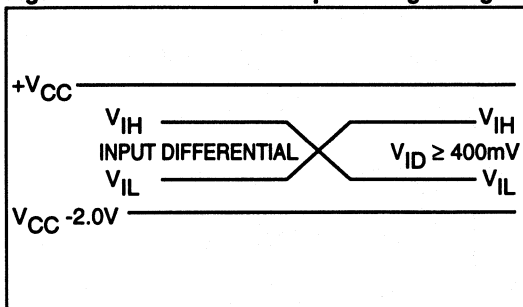
Table 1. Electrical Characteristics

V_{CC} = 3.3V ±0.3V, T_a = 0°C to +70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source-PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source-PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	µA
	CLKSEL	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 100MHz, C _L = 10pF	2.3	V _{CC} +0.3	V
V _{OL}	Output LOW Voltage	F _{OUT} = 100MHz, C _L = 10pF		0.4V	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3 @ 70°C, Typ Pwr=275 mW		450	mW

1. Maximum test duration, one second.
2. The S3LV308 features source series termination of approximately 40 Ohms to assist in matching 50-75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The S3LV308 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the S3LV308 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -2mA	2.4V	
V _{OL}	I _{OL} = 2mA		0.4V

Table 2. AC Specifications—Using Figure 4, AC Test/Evaluation Circuit

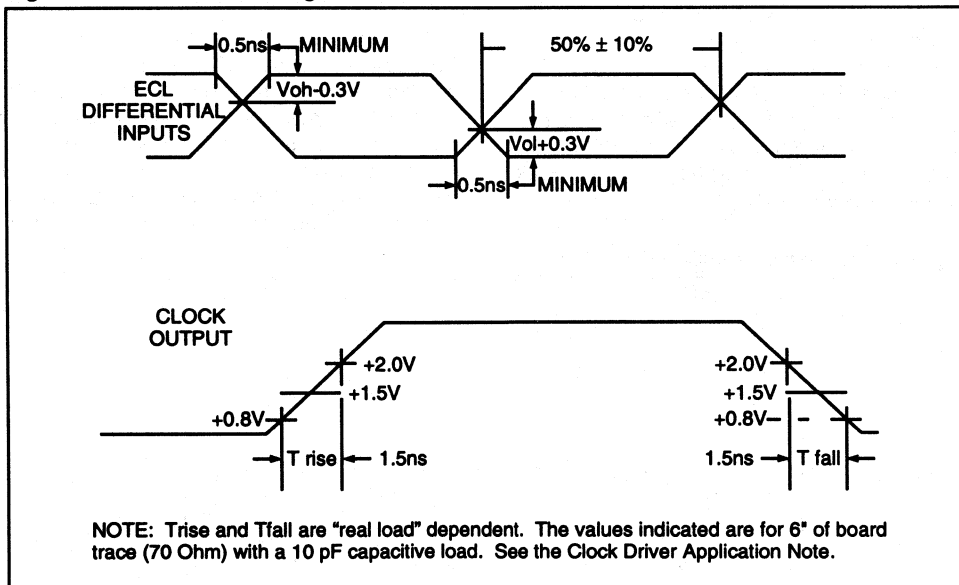
$V_{CC} = 3.3V \pm 0.3V$, $T_a = 0^\circ C$ to $70^\circ C$, $C_{LOAD} = 10pF$

Parameter	S3LV308-1	Units
Maximum Skew Across All Outputs	0.5	ns
Maximum Skew Across Fa, Fb, Fc, or Fd Outputs	0.25	ns
Maximum TTL Input Frequency	100	MHz
Maximum PECL Differential Input Frequency	100	MHz
Maximum Rising/Falling Edge Rate	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. S3LV308 output symmetry follows input symmetry. Output Duty Cycle will also be affected by voltage and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
5. Parameters guaranteed by design and characterization or tested.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single-chip clock buffer and twenty-output fanout driver using AMCC's advanced BiCMOS process. This design has been optimized for absolute minimum skew across all twenty outputs.

For best performance, this approach will require a clock source input from a crystal-controlled oscillator (XCO) located adjacent to this clock driver. This oscillator can provide either differential ECL inputs (referenced to +3.3V, PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to translation amplifiers and output drivers, (refer to Figure 1, Logic Diagram). The output duty factor asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

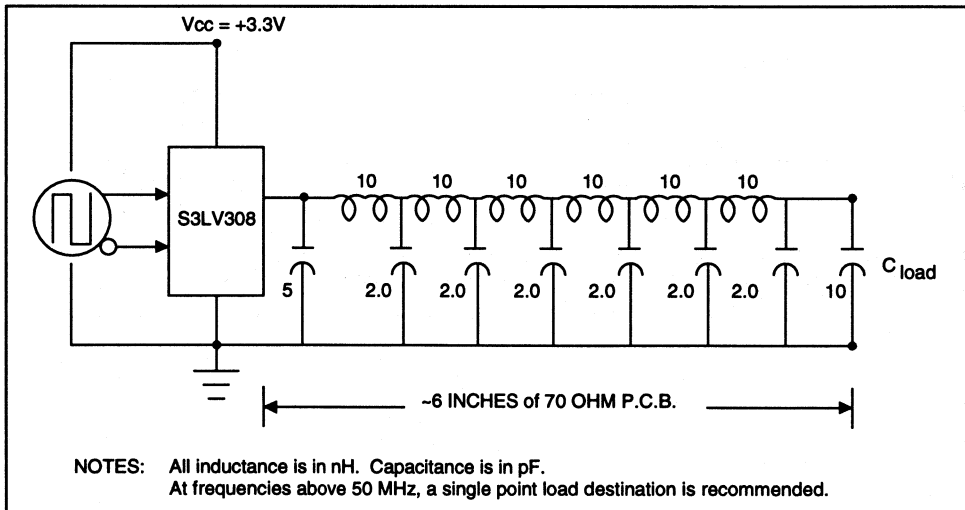
The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high) outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for spice models).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to simultaneously switching outputs, low impedance +V_{CC} and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to ensure that the S3LV308 will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

Figure 4. AC Test/Evaluation Circuit



Power Management

The overall goal of managing the power dissipated by the S3LV308 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the S3LV308 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The output power must be added to the core power (450 mW) of the S3LV308 to determine the total power being dissipated by the S3LV308. This total power is then multiplied by the S3LV308's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the S3LV308. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the S3LV308 is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an S3LV308 with 12 outputs driving 15 pF loads at 50 MHz. Total chip power is calculated as follows:

$$\begin{aligned} \text{Core Power} &= 450 \text{ mW} \\ 12 \text{ outputs, } 15 \text{ pF, } 50 \text{ MHz} &= (12 \times 27 \text{ mW}) = 324 \text{ mW} \\ 8 \text{ outputs, no load, } 50 \text{ MHz} &= (8 \times 10 \text{ mW}) = 80 \text{ mW} \\ \text{Total Power} &= 854 \text{ mW} \end{aligned}$$

The design specifies a 70°C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2°C/watt. The S3LV308's junction temperature would then be:

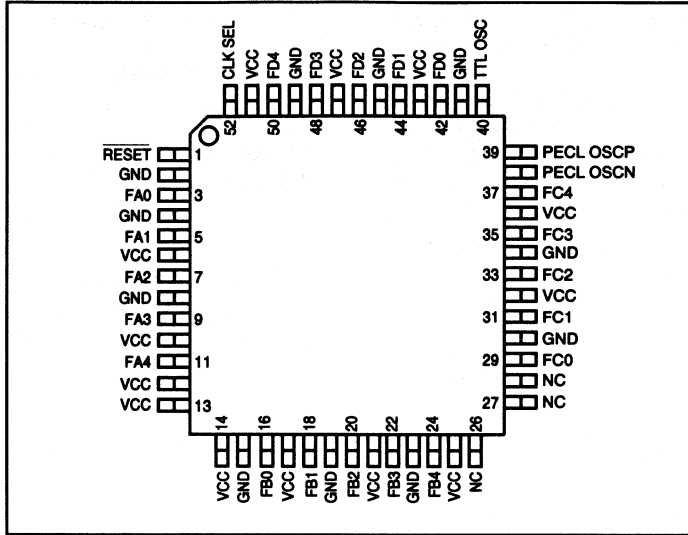
$$70^\circ\text{C} + (.854 \text{ watts} \times 46.2^\circ\text{C/watt}) = 109^\circ\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
100 MHz	33 mW	39 mW	48 mW	70 mW	15 mW
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

Figure 5. S3LV308 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- Device Number
- Package Type
- Skew Option (if applicable)
- Optional Shipping Configuration

S3LV308

Q

-1

/TD

Optional Shipping Configuration

Blank = 84-unit matrix tray
 /D = dry pack
 /TD = tape, reel and dry pack

Skew Option

- 1 = 500 ps output-output skew

Package Option

Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: S3LV308Q-1/D

52-pin PQFP package, 500 ps output-output skew,
 shipped dry packed in the standard matrix tray.

FEATURES

- Ten clock outputs at primary frequency up to 100 MHz
- All outputs are leading-edge synchronized to within ≤ 0.5 ns
- Proprietary output drivers with:
 - Complementary 24 mA peak outputs, source and sink
 - 50–75 Ω source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- Output levels comply with JEDEC LVTTTL standard
- Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers

GENERAL DESCRIPTION

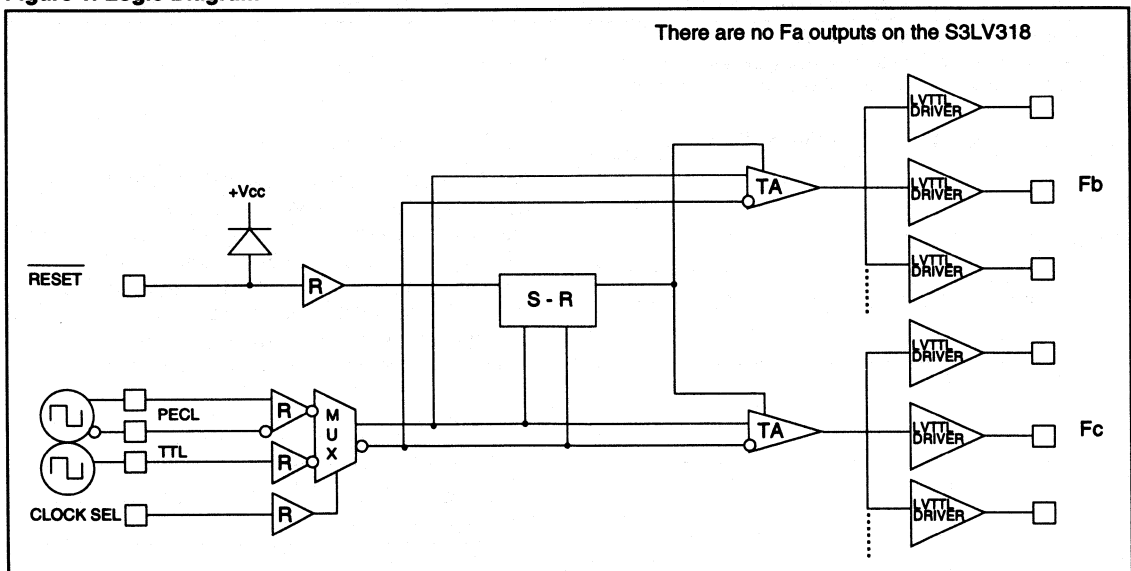
The S3LV318 is a minimum skew clock driver with ten outputs. It can employ a clock input from a single-ended TTL or an ECL differential source operating between +3.3V and ground. This reference frequency input is received and distributed to the clock output drivers. All outputs are "clamped" to conform with JEDEC LVTTTL levels.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈ 1.5 V/ns to minimize simultaneous output-switching noise and distortion.

APPLICATIONS

- Datacom and Telecom networks
- Compatible with Intel's Pentium™ and P6 processors
- PCI Bus clock distribution
- Workstation and server systems with high clock fanout

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +4.6V
Input Voltage	-0.5V to +V _{CC} +0.5V
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

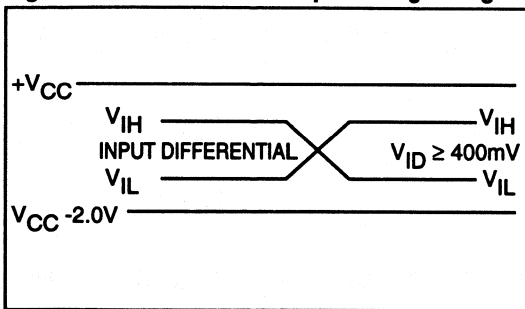
Table 1. Electrical Characteristics

V_{CC} = 3.3V ± 0.3V, T_a = 0°C to +70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (PECL)	Differential Source-PECL	V _{IL} +0.4	+V _{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage (PECL)	Differential Source-PECL	V _{CC} -2.0	V _{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	Input HIGH Current (PECL)	V _{IN} = V _{CC} (max)		200	µA
	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTL	V _{IN} = 2.4V		15	µA
I _{IL}	Input LOW Current (PECL)	V _{IN} = V _{CC} -2.0V		15	µA
	CLKSEL	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTL	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 100MHz, C _L = 10pF	2.3	V _{CC} +3.0	V
V _{OL}	Output LOW Voltage	F _{OUT} = 100MHz, C _L = 10pF		0.4V	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3 @ 70°, Typ Pwr=275mW		450	mW

1. Maximum test duration, one second.
2. The S3LV318 features source series termination of approximately 40 Ohms to assist in matching 50-75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The S3LV318 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the S3LV318 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -2mA	2.4V	
V _{OL}	I _{OL} = 2mA		0.4V

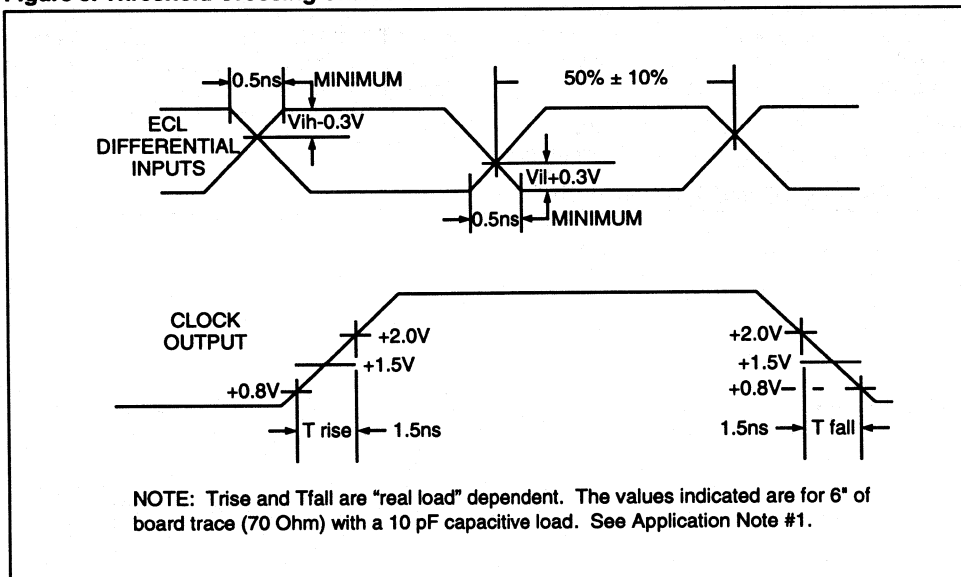
Table 2. AC Specifications—Using Figure 4, AC Test/Evaluation Circuit
 $V_{CC} = 3.3V \pm 0.3V$, $T_a = 0^\circ C$ to $70^\circ C$, $C_{LOAD} = 10pF$

Parameter	S3LV318-1	Units
Maximum Skew Across All Outputs	0.5	ns
Maximum Skew Across Fa or Fb Outputs	0.25	ns
Maximum TTL Input Frequency	100	MHz
Maximum Differential PECL Input Frequency	100	MHz
Maximum Rising/Falling Edge Rate	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The S3LV318 output symmetry follows input symmetry. Output Duty Cycle will also be affected by voltage and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for high loads.
5. Parameters guaranteed by design and characterization or tested.

Figure 3. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION

(Refer to Logic Diagram)

AMCC has developed a single-chip, ten-output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for absolute minimum skew across all ten outputs.

The clock source input for this device may operate between +3.3V and ground and can provide either differential ECL inputs (referenced to +3.3V, PECL) or single-ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL. This input clock will be fanned out to translation amplifiers and output drivers, refer to Figure 1, Logic Diagram. The output duty factor asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low), the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high), the outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin.

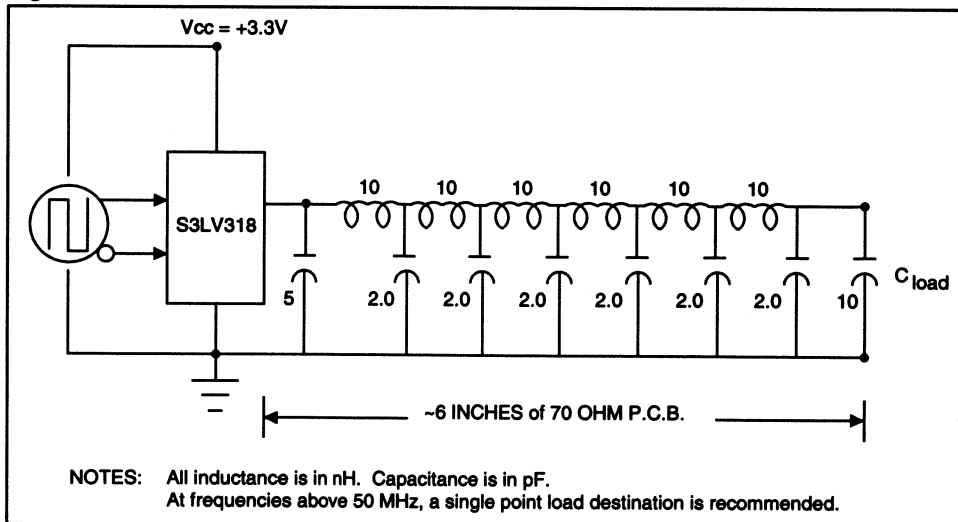
The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion

resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for spice models).

Power and ground are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance +V_{CC} and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the S3LV318 will exhibit skews less than the specified maximum. A plastic 28-lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

Figure 4. AC Test Circuit/Evaluation Circuit



Power Management

The overall goal of managing the power dissipated by the S3LV318 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the S3LV318 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The output power must be added to the core power (450 mW) of the S3LV318 to determine the total power being dissipated by the S3LV318. This total power is then multiplied by the S3LV318's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the S3LV318. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the S3LV318 is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an S3LV318 with 8 outputs driving 10 pF loads at 66 MHz. Total chip power is calculated as follows:

$$\begin{aligned} \text{Core Power} &= 450 \text{ mW} \\ 8 \text{ outputs, } 10 \text{ pF, } 66 \text{ MHz} &= (8 \times 33 \text{ mW}) = 264 \text{ mW} \\ 2 \text{ outputs, no load, } 66 \text{ MHz} &= (2 \times 11 \text{ mW}) = 22 \text{ mW} \\ \hline \text{Total Power} &= 736 \text{ mW} \end{aligned}$$

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The S3LV318's junction temperature would then be:

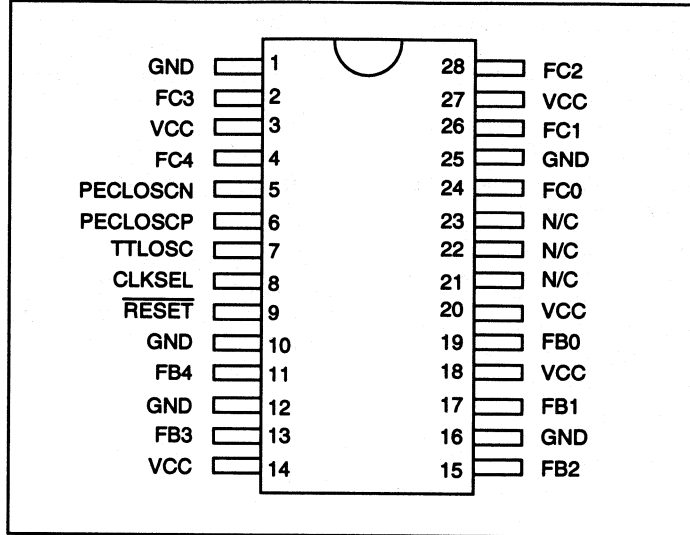
$$70^\circ\text{C} + (0.736 \text{ watts} \times 57.7^\circ\text{C/watt}) = 112^\circ\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
100 MHz	33 mW	39 mW	48 mW	70 mW	15 mW
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

Figure 5. S3LV318 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

S3LV318

S

-1

/TD

Optional Shipping Configuration

Blank = 25-unit tube

/D = dry pack

/TD = tape, reel and dry pack

Skew Option

- 1 = 500 ps output-output skew

Package Option

S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: S3LV318S-1/D

28-pin SOIC package, 500 ps output-output skew, shipped dry packed in the standard tube.

FEATURES

- Six clock outputs at primary reference frequency up to 100 Mhz
- Eight clock outputs selectable at half primary reference frequency up to 50 Mhz, or at secondary reference frequency up to 100 Mhz
- Selectable single or dual reference frequencies
- Leading edge skew for all F_b outputs <500 ps
- Leading edge skew for all F_c outputs <250 ps
- Proprietary output drivers with:
 - Complementary 24 mA peak outputs, source and sink
 - 50–75Ω equivalent source series termination
 - Dynamic drive adjustment to match load conditions
 - Edge rates less than 1.5 ns
- Output levels compatible with JEDEC LVTTTL standard
- Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers

APPLICATIONS

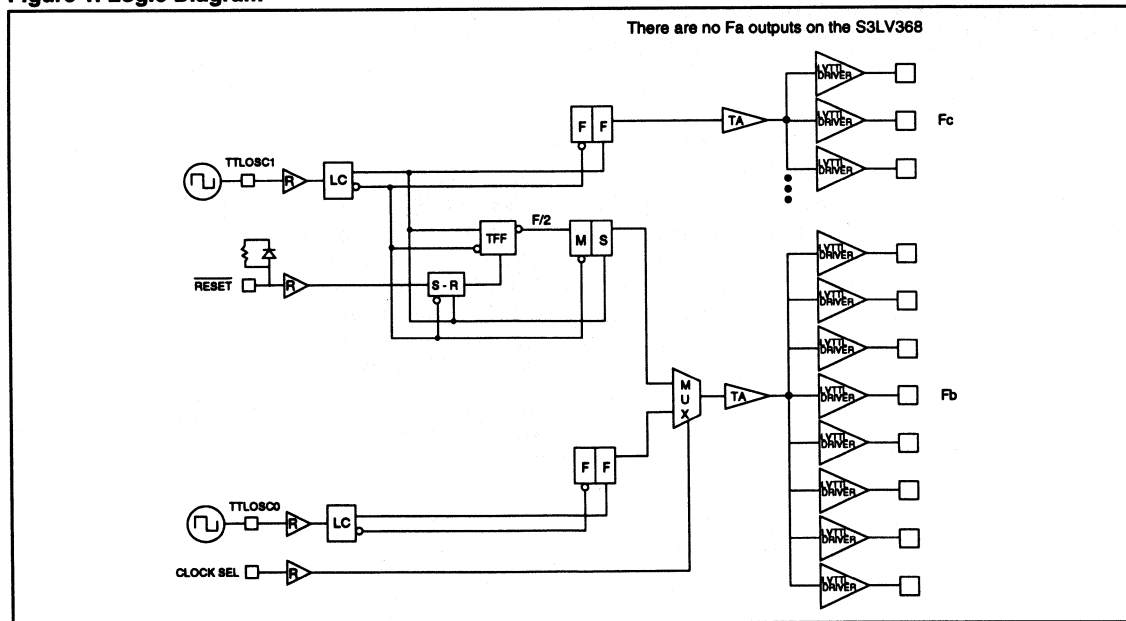
- Datacom and Telecom networks
- Compatible with Intel's Pentium™ and P6 processors
- PCI Bus clock distribution
- Workstation and server systems with high clock fanout

GENERAL DESCRIPTION

The S3LV368 is a low skew clock driver with fourteen outputs. Six outputs operate at the primary reference frequency and eight outputs operate at either half the primary reference frequency or at the secondary reference frequency. A synchronous reset ensures proper phase of the half frequency outputs. It can employ clock input from either one or two single-ended TTL sources. These reference frequency inputs are received and distributed to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of $\approx 1.5V/ns$ to minimize simultaneous output-switching noise, distortion, and EMI.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature	-55° to +150°C
V _{CC} Potential to Ground	-0.5V to +4.6V
Input Voltage	-0.5V to +V _{CC}
Static Discharge Voltage	>1750V
Maximum Junction Temperature	+140°C
Latch-up Current	>200 mA
Operating Ambient Temperature	0° to +70°C

Capacitance (package and die total)

Input Pins	5.0 pF
TTL Output Pins	5.0 pF

Table 1. Electrical Characteristics

V_{CC} = +3.3V ± .3V, T_a = 0°C to +70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V _{CC}	V
V _{IL}	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I _{IH}	CLKSEL	V _{IN} = V _{CC} (max)		350	µA
	RESET	V _{IN} = 2.4V		-200	µA
	TTLOSCx	V _{IN} = 2.4V		15	µA
I _{IL}	CLKSEL	V _{IN} = 0.4V		25	µA
	RESET	V _{IN} = 0.5V		-325	µA
	TTLOSCx	V _{IN} = 0.4V		15	µA
V _{OH}	Output HIGH Voltage	F _{OUT} = 100MHz, C _L = 10pF	2.3V	V _{CC} +0.3	V
V _{OL}	Output LOW Voltage	F _{OUT} = 100MHz, C _L = 10pF		0.4V	V
I _{OHS} ¹	Output HIGH Short Ckt Current	Output High, V _{OUT} = 0V Typ	-55		mA
I _{OLS} ¹	Output LOW Short Ckt Current	Output Low, V _{OUT} = V _{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3, Typ Pwr=250mW		400	mW

1. Maximum test duration, one second.
2. The S3LV368 features source series termination Ohms to assist in matching 50–75 Ohm P.C. board environments.

DC Characteristics

The S3LV368 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic “high drive, totem pole outputs” and AMCC’s dynamically adjusting source series terminated outputs. As a result of this, the S3LV368 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V _{OH}	I _{OH} = -2mA	2.4V	
V _{OL}	I _{OL} = 2mA		0.4V

Table 2. AC Specifications — Using Figure 4, AC Test/Evaluation Circuit

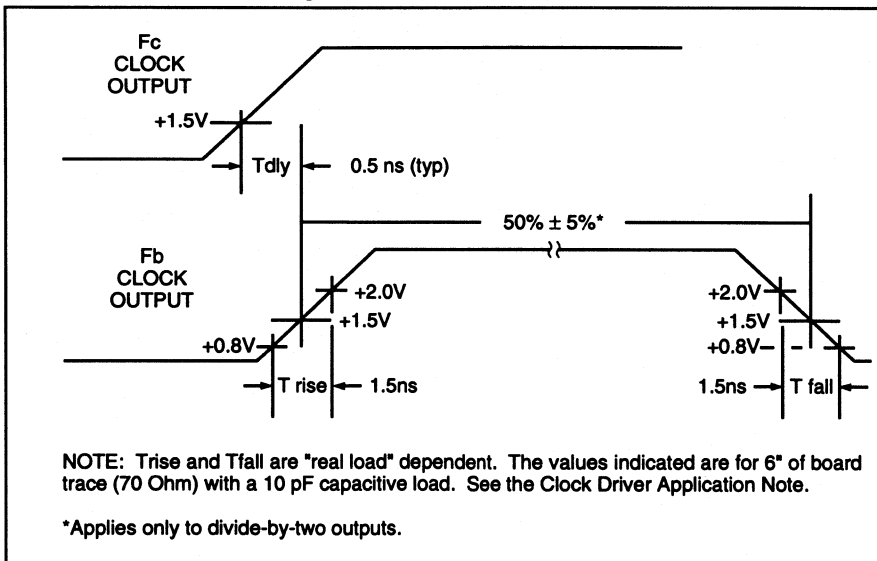
$V_{CC} = +3.3V \pm .3V$, $T_a = 0^{\circ}C$ to $+70^{\circ}C$, $C_{LOAD} = 10pF$
 (reference Figure 2, Threshold Crossing Characteristics)

Parameter	S3LV368	Units
Maximum Skew Across Fb outputs	500	ps
Maximum Skew Across Fc outputs	250	ps
Maximum Skew Across Fb and Fc outputs, CLKSEL=0	500	ps
Delay of Fb from Fc outputs (CLKSEL = 1) [T _{dly}]	Minimum	50 ps
	Typical	500 ps
	Maximum	<1.0 ns
Maximum Output Duty Cycle Asymmetry	Minimum	45 %
	Maximum	55 %
Maximum Rising/Falling Edge Rate [T _{rise} /T _{fall}]	1.5	ns
Maximum TTL Input Frequency	100	MHz
Maximum TTL Output Frequency	100	MHz

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The S3LV368 output symmetry follows input symmetry for F_C outputs.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
6. Parameters guaranteed by design and characterization or tested.

Figure 2. Threshold Crossing Characteristics



DESCRIPTION OF OPERATION **(Refer to Logic Diagram)**

AMCC has developed a single-chip fourteen-output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across outputs of the same frequency.

The clock source input for this device can select either one or two single-ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects the dual reference frequency mode, and logic HIGH selects the single reference frequency (TTLOSC1) mode. This input clock will be fanned out to translation amplifiers and output drivers (refer to the preceding logic diagram). The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

When the $\overline{\text{RESET}}$ input is held low (active), the FB0-7 outputs will be driven low. When $\overline{\text{RESET}}$ is de-asserted, the FB0-7 outputs will be active after a fixed three-input clock delay if the single-reference frequency mode is selected. The reset function is only operational when CLKSEL = 1.

The output drivers are rise and fall slew rate controlled to $\sim 1.5\text{V/ns}$ to minimize noise and distortion resulting from simultaneous switching of the 14 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot

of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance ($>25\text{pF}$ with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for simulation results).

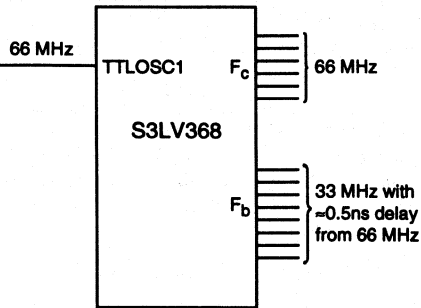
To lower noise and maintain signal fidelity, power and ground pins are carefully interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{\text{CC}}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the S3LV368 will exhibit skews less than the specified maximum. A plastic 28 lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

Figure 3. Application Examples

**Example 1.
Low Skew, Single Reference Frequency Mode**

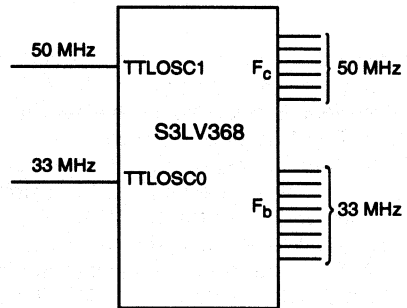
Six outputs at the primary frequency and eight outputs at half the primary frequency; each group internally synchronized. The 33 MHz outputs are delayed from the 66 MHz outputs by $\approx 0.5\text{ns}$.



CLKSEL = 1

**Example 2.
Dual Reference Frequency Mode, Asynchronous**

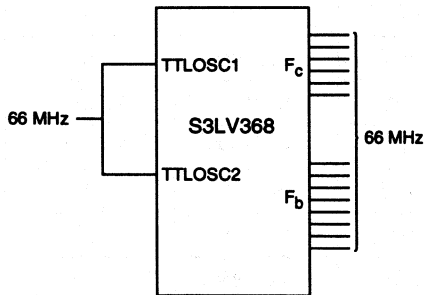
Six outputs at the primary frequency and eight outputs at the secondary frequency.



CLKSEL = 0

**Example 3.
Single Reference Frequency Mode, Synchronous**

All fourteen outputs will follow the input reference with a maximum skew of 500 ps across all outputs.



CLKSEL = 0

Power Management

The overall goal of managing the power dissipated by the S3LV368 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the S3LV368 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit).

The individual output power must be added to the static core power (400 mW) of the S3LV368 to determine the total power being dissipated by the S3LV368. This total power is then multiplied by the S3LV368's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the S3LV368. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the S3LV368 is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an S3LV368 with 5 outputs driving 10 pF loads at 66 MHz and 8 outputs driving 15 pF loads at 33 MHz. Total chip power is calculated as follows:

$$\begin{aligned} \text{Core Power} &= 400 \text{ mW} \\ 5 \text{ outputs, } 10 \text{ pF, } 66 \text{ MHz} &= (5 \times 33 \text{ mW}) = 165 \text{ mW} \\ 1 \text{ output, no load, } 66 \text{ MHz} &= (1 \times 11 \text{ mW}) = 11 \text{ mW} \\ 8 \text{ outputs, } 15 \text{ pF, } 33 \text{ MHz} &= (8 \times 17 \text{ mW}) = 136 \text{ mW} \\ \hline \text{Total Power} &= 712 \text{ mW} \end{aligned}$$

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The S3LV368's junction temperature would then be:

$$70^\circ\text{C} + (.712 \text{ watts} \times 57.7^\circ\text{C/watt}) = 111^\circ\text{C}$$

Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	NO LOAD
100 MHz	33 mW	39 mW	48 mW	70 mW	15 mW
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

Figure 4. AC Test/Evaluation Circuit

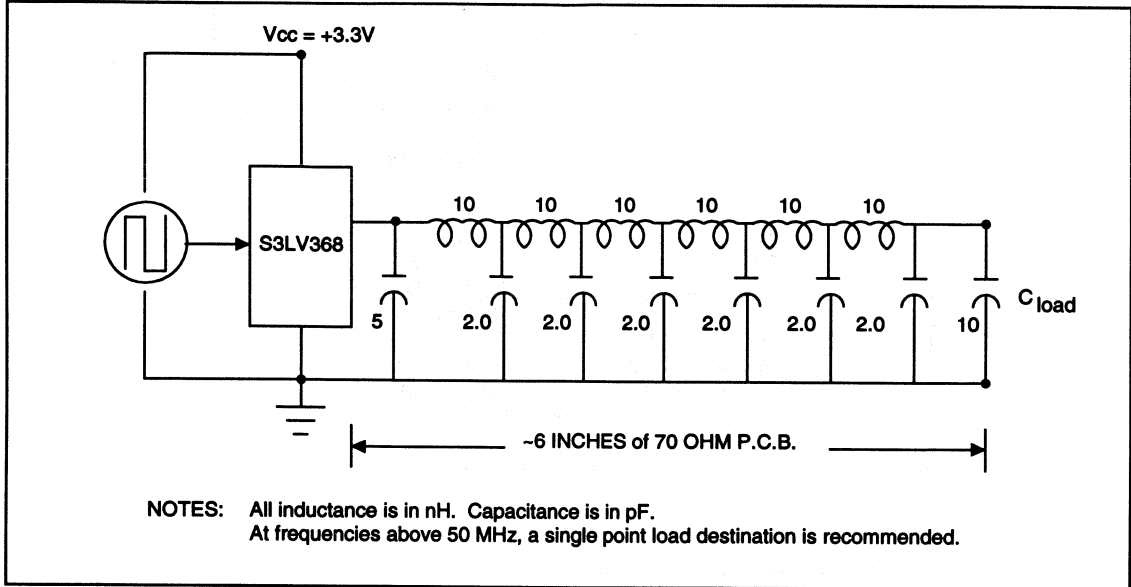
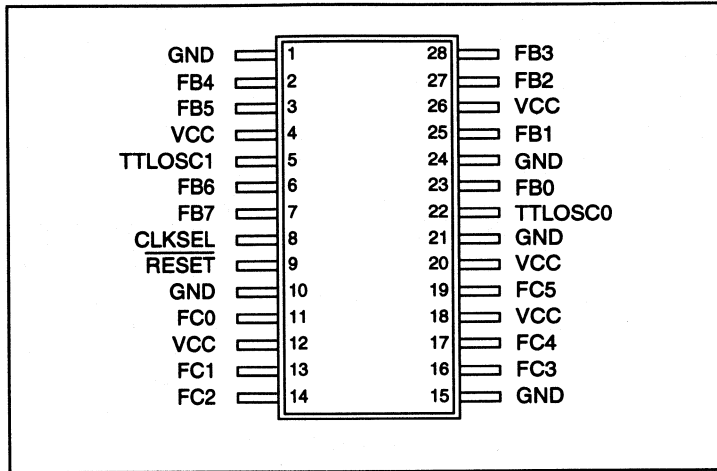


Figure 5. S3LV368 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Optional Shipping Configuration**

S3LV368

S

/TD

Optional Shipping Configuration

Blank = 25 unit tube

/D = dry pack

/TD = tape, reel and dry pack

Package Option

S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: S3LV368S/D

28-pin SOIC package, shipped dry packed in the standard tube.

The SC35XX Family of Clock Drivers have been designed to provide single chip solutions which ease clock distribution for TTL/CMOS I/O compatible microprocessor based systems.

All products have a generous supply (10 or 20) of the various derived frequency outputs to avoid overloading any one output. The outputs may also be used in parallel for driving particularly heavy loads. The availability of numerous clock outputs reduces the need to "daisy chain" or "branch" loads. The end benefit to the user is reduced clock skew with a high quality received wave form. By virtue of this single chip providing clock shape, clock edge alignment and clock fanout, the system designer's task is reduced to providing load balance and careful PC board layout.

The "Appnote" describes and discusses:

- Frequency Sources
- Skew Management
- Clock Waveform Signal Integrity
- Chip Power Estimations
- High Capacitance Loads
- Output Symmetry Compensation
- Reset Control and Timing
- Use of Multiple Clock Chips in a System-
Primary and Secondary Distribution

FREQUENCY SOURCE

It is suggested that the basic Frequency Source be a low cost crystal-controlled oscillator (XCO). Frequency tolerance and stability are offered from 0.05% (500PPM) to 0.001% (10PPM), with 0.01% (100PPM) being readily available at competitive prices. These crystal oscillators should be acceptable over most operating temperature ranges. Only with large temperature fluctuations during operation would the higher priced temperature compensated crystal oscillator (TCXO) be suggested. TTL output devices are available up to 100 MHz with ECL output devices spanning the entire range of interest, from 30 to 200 MHz.

An appended list of domestic sources for these oscillators, including phone numbers is provided. While this list is not all inclusive, it will provide an initial reference (See Appendix A).

NOTE: The SC35XX PECL (Positive 5 -Volt ECL) inputs are designed to interface with an ECL output oscillator operating at ground to +5.0 Volts. The oscillator's complementary emitter follower outputs may be "self-terminated" within the package by 200 to 500 Ohm pull down resistors to ground (-Vee) or they may be terminated discretely via resistors on the PC board. The oscillator should be placed close (<3") to the SC35XX driver.

CLOCK SKEW MANAGEMENT

The SC35XX has been designed to reduce the system level Clock Skew Management task to two basic design issues.

1) Balancing clock trace delays

Balancing clock trace delays requires the use of equal lengths of microstrip and stripline traces on each clock line

"Microstrip," which is a single surface conductor over a distributed ground or power plane, has a nominal propagation delay of approximately 150 pS per inch (see Figure 1).

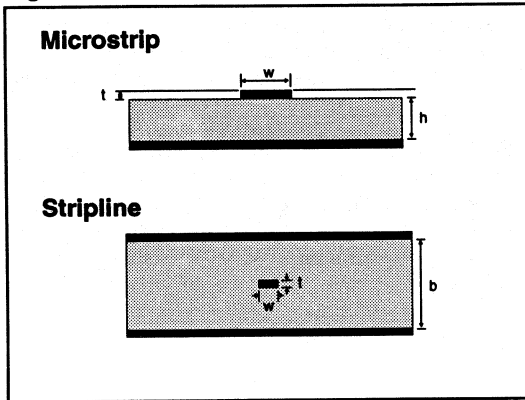
"Stripline," which is a buried conductor sandwiched between two ground or power planes, has a nominal propagation delay of approximately 200 pS per inch.

To match clock trace lengths, when the receiving devices are differing "Manhattan" distances from the SC35XX drive, the PC trace must be lengthened to the closer loads. This can be accomplished by forming a "serpentine" path (Figure 2).

2) Matching the end-of-line load capacitance

Variations in the end-of-line lumped-load capacitance will increase or decrease the clock signal's rise and fall time. These changes will be approximately 0.5 ns per 10 pF over the range of 10 to 40 pF. Be sure to verify the receiving input package capacitance of all clock receptors. Typically, plastic flat packs have the lowest input pin capacitance and ceramic pin grid arrays (PGAs) have the highest. PGAs also have the disadvantage that their plated thru holes can add significant capacitance (up to 10 pF or more). This should be checked with a capacitance meter.

Figure 1



CLOCK WAVEFORM SIGNAL INTEGRITY

Clock waveform signal integrity refers to the control of noise margin and receiver threshold crossing distortions. DC margins for TTL I/O levels are often secondary when operating frequencies exceed 25 MHz. This is due to the overriding effects of "overshoot/undershoot" (i.e., ringing) or poorly terminated transmission lines causing reflections on the clock traces.

The effect of these reflections can be the presence of half or partial amplitude steps in the clock waveform appearing at intermediate "branched" or "daisy chained" load points. These partial amplitude steps can cause spurious triggering at these intermediate load points.

The TTL/CMOS clock output driver must provide a reasonably square voltage waveform from +0.5 to +3.5 Volts, as a minimum. Unfortunately, you must distribute this clock over a printed copper trace with variable inductance, capacitance and length, which may exhibit characteristic line impedance (Z_0) anywhere from 50 to 200 Ohms. Add to this the variable of receiver(s) load capacitance and notice that the 50% duty cycle square wave that you started with has become distorted with ringing and undershoot. You should be aware that undershoot below about -1.0 Volt can draw substrate bias current at the receivers causing transient errors.

This leads to a need for controlled impedance clock traces with good termination. This is especially true when device clock frequencies are greater than 30 MHz while the high and low times of critical minimum widths and voltage levels are specified.

Figure 2

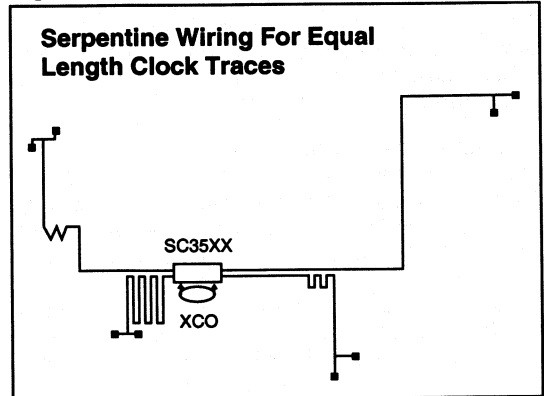
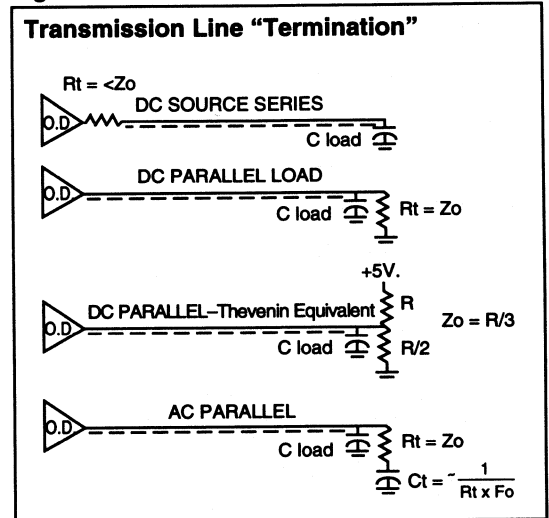


Figure 3



Termination is needed on lines that exhibit ringing and signal distortion. The ringing and distortion are caused by mismatched clock driver output impedance, line impedance, and load input impedance. The termination is used to match the line impedance to the driver or load impedance.

Several methods of line termination are available (refer to Transmission Line "Termination," Figure 3):

A. DC parallel load termination is generally a Thevenin equivalent resistor pair across the +5 Volts and ground buses with the mid point tied to the end of each clock line. While the signal integrity results are good, the large power consumption, due to the large voltage applied to the low end of line resistance make this scheme a poor choice.

B. AC parallel load termination can be effective to "tune" each load network with a selected parallel resistor-capacitor pair at the end of each clock line to ground. If the load capacitance or line length varies appreciably, so must the R-C termination pair. As with any of the parallel termination schemes, you must provide external trace and component mounting locations at the end of every clock line. AC power dissipation is quite high using this method.

C. DC source series termination can be incorporated within the clock driver output, thereby eliminating the need for external components. Clock loads may only be placed at the end of the line. This series termination reduces the power dissipation.

NOTE: Use of any of the parallel or termination methods precludes the use of branch or "Y" wiring within the clock fanouts due to impedance splitting.

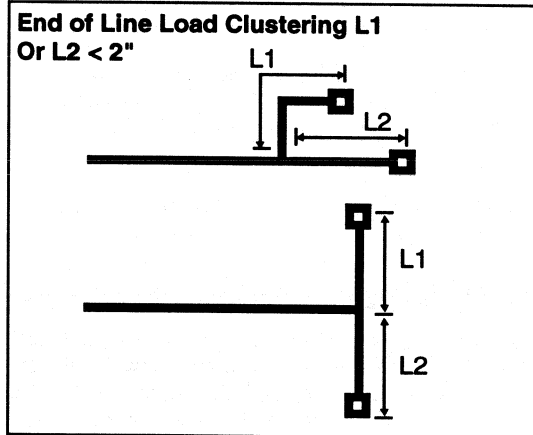
The following table compares these three described termination schemes.

	DC PARALLEL	AC PARALLEL	SERIES
EXTERNAL MOUNTING	YES	YES	NO
TUNING AT LOADS	NO	POSSIBLE	NO
DAISEY CHAIN	PENALTY	PENALTY	NO
LOAD CLUSTER AT END	DESIRED	DESIRED	REQ'D

The SC35XX helps the designer manage these clock termination in two ways. First, with a generous number of clock outputs (10 or 20) available, "daisy chained" or "branched" connected receivers can be avoided. Secondly, the source termination within the SC35XX output drivers is provided to terminate a lumped-load capacitance at the end of a 60–100 Ohm transmission line, without the addition of any discrete termination circuits.

While 100 Ohm traces are preferred, characteristic line impedances of 50 or 75 Ohms, may be necessary at an increase of power in the SC35XX's output drivers. These lower impedance PC board traces are generally dictated by manufacturing issues accompanying multiple signal, power, and ground layers in the PC board fabrication.

Figure 4



Remember that TTL type signal amplitudes, in the 2.5 to 4.0 Volt peak range, dissipate considerable AC (CV^2F) power. This AC power, coupled with the fact that the transmission line capacitance is at least twice as great at $Z_0=50$ Ohms compared to $Z_0=100$ Ohms, strongly suggests that the characteristic trace impedance of high frequency clock lines should be selected at 70 Ohms or above to reduce the clock distribution power. See Appendix B for equations.

NOTE: For series terminated lines, a maximum of two loads may be driven if the stub lengths are less than two inches in length. The capacitance of each pin is additive. See Figure 4.

SC35XX POWER DISSIPATION

With output frequencies above 50 MHz, the SC35XX's loading must be "managed" to limit its power dissipation to less than 1 Watt. This can be accomplished by minimizing the loading on each clock output or by connecting fewer of the clock outputs. In this case unused outputs still dissipate a minimum of power, which must be added into the total.

The SC35XX product data sheets detail all necessary power dissipation calculations.

NOTE: The capacitance of 70 Ohm transmission line is approximately 1.5 times that of 100 Ohm line for effective lengths up to one rise time or ~10 inches and, as mentioned above, with $Z_0=50$ Ohms the capacitance is twice that of $Z_0=100$ Ohms. The additional effective output load capacitance is approximately 8 pF for 70 Ohms at 10 inches as compared to 100 Ohms. See Appendix B for equations.

CAPACITIVE LOADS

Capacitive loads consist of four contributors:

- The "load" package itself, where a plastic flat pack may exhibit 4–8 pF loads, while a ceramic pin grid array may represent 8–15 pF loads.
- Plug in sockets can add 5–10 pF.
- Plated-through-holes and vias, in a dense multiplayer PC board may add as much as 5–15 pF.
- PC board trace impedance (as reviewed above)

AMCC strongly recommends that the user "balance" his loads. This will help to minimize skew at the various loads (the larger a load is, the slower the rise time of the clock). Where the user is not able to balance his loads, the skew will typically be derated at 50 ps/pF at the 1.5V threshold. (Example – one load is 5 pF heavier than all other loads – that load's clock will cross the 1.5V threshold 250 ps later than the others). A compensatory shortening of the higher capacitance load traces may be considered.

In addition to presenting capacitive loads, some microprocessors and co-processors require minimum peak clock amplitudes of 3.5 Volts or greater along with a minimum dwell time at a specified voltage level.

While each output driver of the SC35XX has been designed to handle a wide frequency-voltage-load range, they have also been designed to allow the parallel application of two (or more) adjacent drivers to a common load. By connecting two adjacent drivers to a common load, such as a microprocessor or co-processor, the user reduces the effective output series termination by half, while doubling the AC and static output current that can be supplied to that load.

RESET CONTROL

The reset control input is clocked into a 3 stage shift register in each driver to ensure that the asynchronous RESET input is synchronized to the input clock.

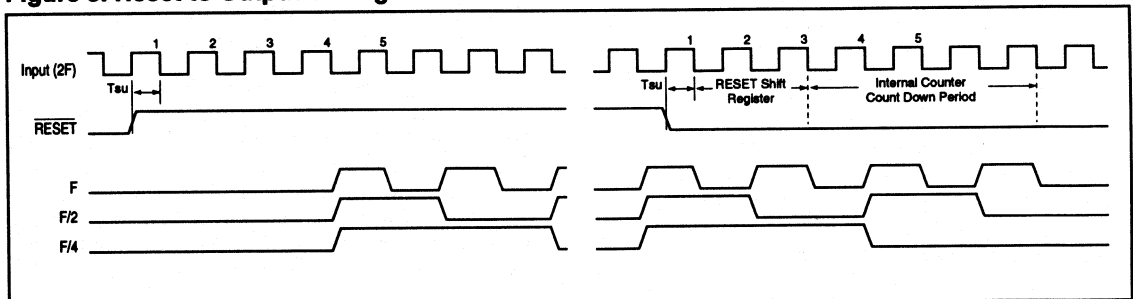
The outputs resume toggling when $\overline{\text{RESET}}$ is deasserted. On the fourth or fifth falling clock edge after the deassertion of RESET, the outputs begin operating in a synchronous fashion.

When $\overline{\text{RESET}}$ is asserted, the internal counter is allowed to continue counting until each of its outputs is in the low state. At that point all the driver outputs will be in the low state, and they will be held low until RESET is deasserted. Since RESET may be asserted when the internal counter is in any state, there will be a delay of 0 to 7 clocks plus the 3 clock shift register before all the outputs will be disabled.

The designer may choose to use a simple "power on" reset function by using an external capacitor connected between the RESET pin and ground. When power is applied, the clock driver will be held in the disabled state until the capacitor is charged through the pull-up resistor on the RESET input.

NOTE: The above reset timing control applies to SC3500, SC3506, SC3507, SC3508, SC3517, SC3518, SC3528 and SC3529. If multiple outputs of SC35XX are to be reset resynchronized by a common RESET input to all, set up and hold time of RESET with respect to the input clock of 3 ns must be accommodated.

Figure 5. Reset to Output Timing



USE OF MULTIPLE CLOCK CHIPS IN A SYSTEM

Many applications require greater than 20 clock outputs, and the use of multiple SC35XXs would be advantageous. The loads that receive these clocks may all reside on a large PC Board, or they may be distributed across a number of PC Boards interconnected via a backplane.

To effectively distribute these clocks requires the user to give some consideration to the strategy for distributing the SC35XX primary input clock. The objective is to get a low skew primary clock distributed to each SC35XX.

Remember that the SC35XX provides the option of two different types of primary clock inputs. For primary inputs over short distances and at frequencies of 50 MHz or less the single rail TTL input may be used. For "longer" distances and backplanes or where the primary frequencies exceed 50 MHz AMCC recommends that the user consider utilizing the "PECL" (Positive referenced 100K ECL input). In either case a single +5V power supply is the only power supply required.

The diagrams on the following pages summarize these recommendations.

The High Speed PECL distribution scheme utilizes the Motorola MC100E111 (Differential, 1:9, 50 ps Skew, ECL Driver) fed from the Crystal Oscillator (XCO). This primary fanout driver requires a pair of 240 Ohm pull down resistors to ground at its input pins. All of the output pairs should be source terminated by a 40 Ohm resistor in series and a 240 Ohm pull down (to ground) resistor at both legs of the differential PECL output. The differential primary fanout branches should be of equal length when routed to the receiving SC35XX.

Alternatively, the PECL backplane signal pairs can be parallel terminated at each SC35XX input by a thevenin equivalent 50–70 Ohm resistor to +3V. As an example, a 100 Ohm resistor to +5V and a complement 150 Ohm resistor to ground is equivalent to 60 Ohms to +3V.

There are two main advantages to these schemes.

1. Minimal Noise Generation

The high speed PECL Signals are limited to 0.8V in amplitude. This limits the potential crosstalk effects that they might have on surrounding signals, and limits their radiated energy (EMI).

2. High Noise Immunity

Since the PECL signals are differentially received at the SC35XX, any noise will appear in equal phase and amplitude on each of the differential signals. The SC35XX will reject this common mode noise at its receiver, providing excellent noise immunity.

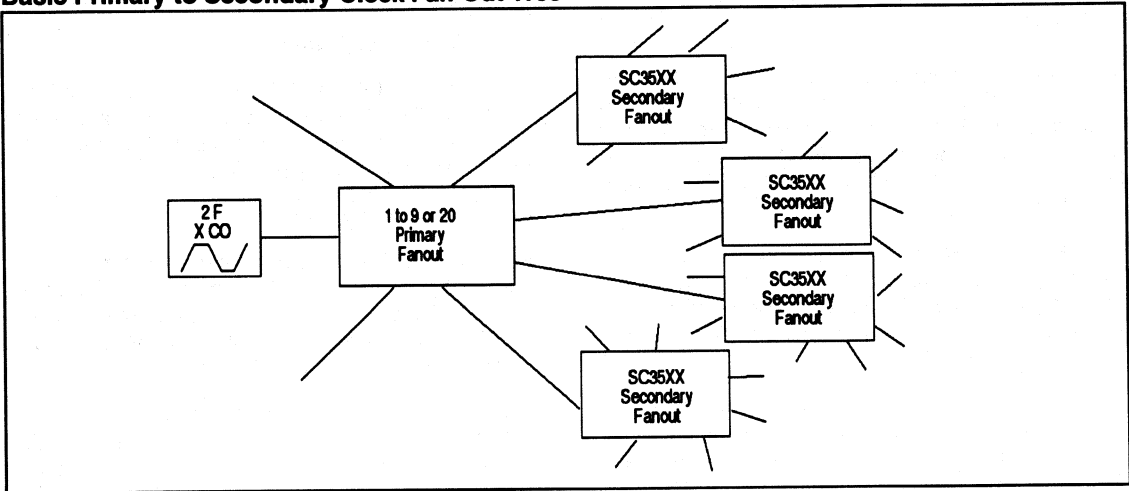
The Low Speed TTL distribution scheme utilizes the SC3508 (TTL 1:20 Driver) fed from a crystal oscillator. Good clock distribution techniques should be followed. This includes avoiding "daisy chaining" or "branching" of the clock fanouts (greater than 2" stubs).

SUMMARY

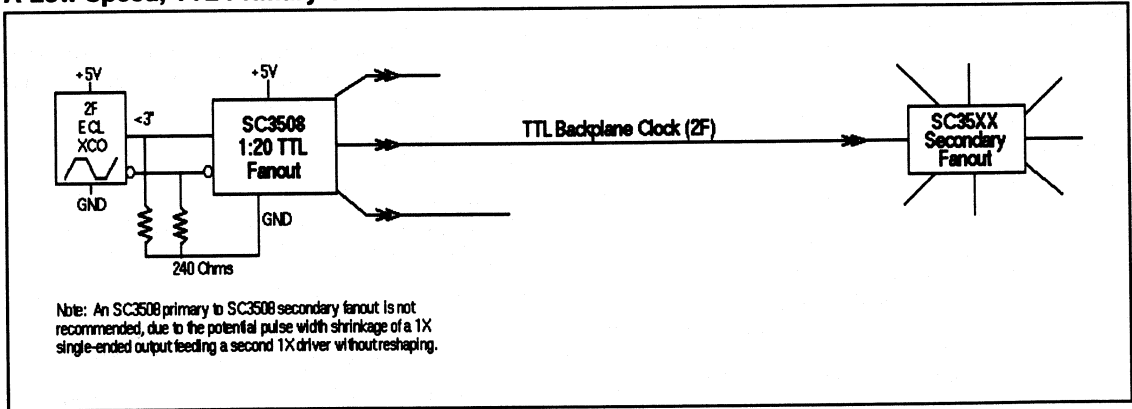
The SC35XX greatly simplifies the task associated with distributing high performance clocks within today's systems. It accomplishes this by reducing the variables that the designer must contend with to these basic issues:

- 1) Keep each clock driver's loading light (SC35XX's large output count allows the clock loads to be distributed one load per clock output typically);
- 2) Balance the total load equally among all drivers;
- 3) Keep clock trace lengths equal (Use serpentine traces to make all clock traces of equal length);
- 4) Be aware of and manage AC power dissipation in the SC35XX. Where possible make clock traces $Z_0=70$ to 100 Ohms for minimal power dissipation;
- 5) High capacitive loads at high frequencies can be supported by paralleling two adjacent SC35XX outputs;
- 6) Be generous with switching noise decoupling capacitors at the four sides of the SC35XX drivers, between the +V_{CC} and ground planes. AMCC recommends a pair of 0.1 μ F and 0.01 μ F ceramic capacitors at each side of the SC35XX package. These decoupling capacitors should be placed on the same side of the board as the SC35XX, and very close to the power and ground package pins.

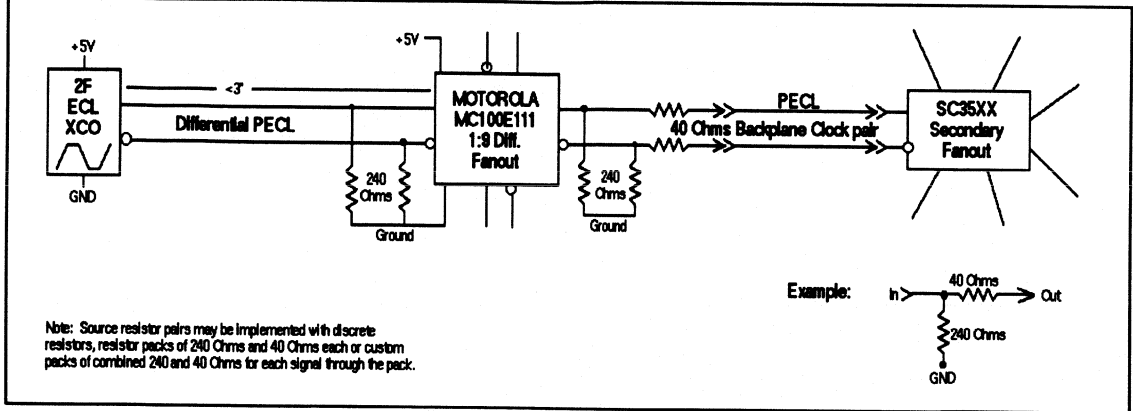
Basic Primary to Secondary Clock Fan-Out Tree



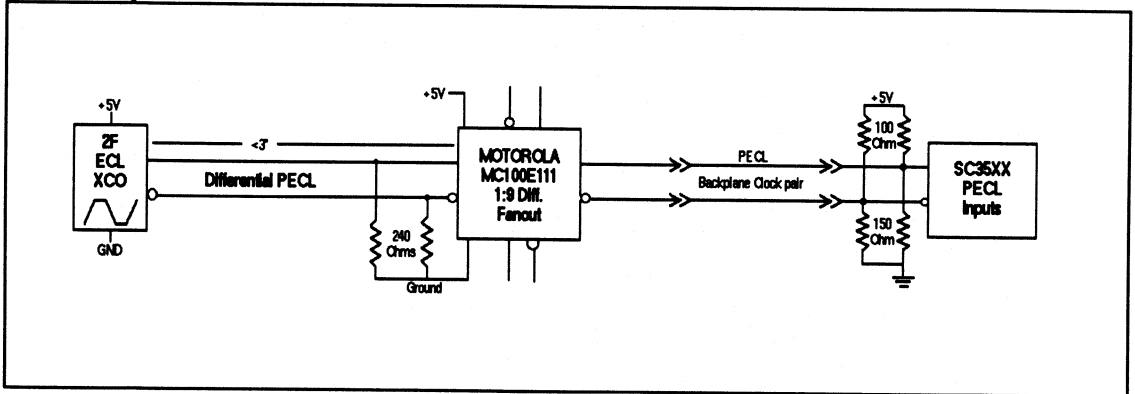
A Low Speed, TTL Primary Clock Fan-Out Path to the SC35XX



A High Speed Series Terminated PECL Primary Clock Fan-Out Path to the SC35XX



Alternate PECL Primary Fanout Path to SC35XX With Parallel Termination at each SC35XX Input Pair



APPENDIX-A**Crystal Controlled Oscillator Suppliers**

MONITOR PRODUCTS, Oceanside, CA	619-433-4510
CTS, KNIGHTS DIVISION, Sandwich, IL	815-786-8411
ECLIPTEK, Fountain Valley, CA	714-963-4009
SARONIX, Palo Alto, CA	800-227-8974
STANDARD CRYSTAL, El Monte, CA	800-423-4578
CONNOR-WINFIELD, Aurora, IL	708-851-4722
ANDERSON ELECTRIC, Holidaysburg, PA	814-695-4428
CHAMPION TECHNOLOGIES, Franklin Park, IL	708-451-1000

APPENDIX-B**PC Board Transmission Line Equations**

The characteristic impedance and propagation delay for printed circuit board traces are functions of the board material, physical board layout and board topology. Please refer to Figure 1 for referenced dimensions.

The following calculations assume G-10 glass-epoxy board material with an $\epsilon_r=4.7$:

CHARACTERISTIC IMPEDANCE

$$Z_0 = (L_0/C_0)^{1/2}$$

PROPAGATION DELAY

$$T_{pd} = (L_0 \cdot C_0)^{1/2} \text{ pS/inch, if units are in inches}$$

MICROSTRIP TECHNOLOGY

$$Z_0 = 35.2 \text{Ln}[(6 \cdot h)/(0.8 \cdot w + t)]$$

STRIPLINE TECHNOLOGY

$$Z_0 = 27.7 \cdot \text{Ln}[(1.9 \cdot b)/(0.8 \cdot w + t)]$$

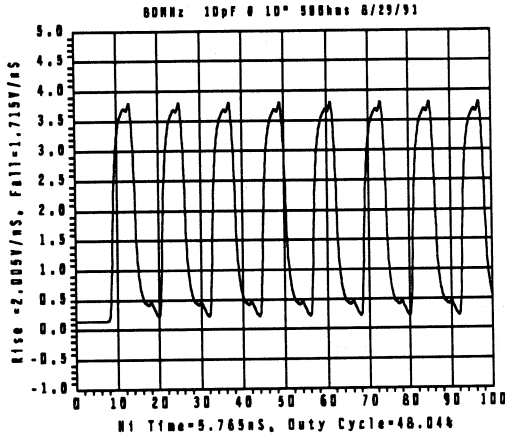
APPENDIX-C

Spice Simulation of Output Waveforms

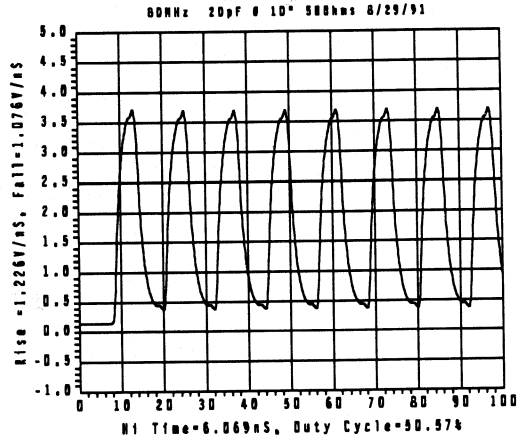
Modeled Frequency – 80MHz

(X-Axis is in ns)

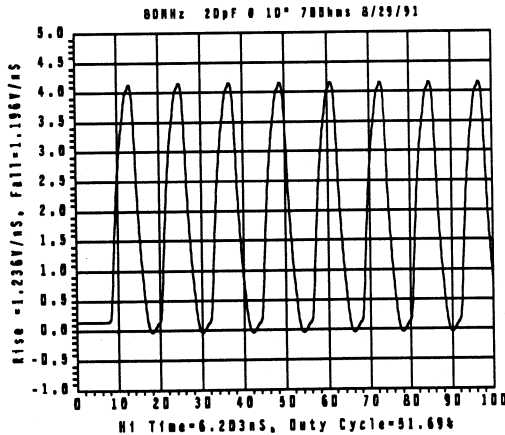
10 pF Load with 10" of Trace ($Z_0=50\Omega$)
Single Driver



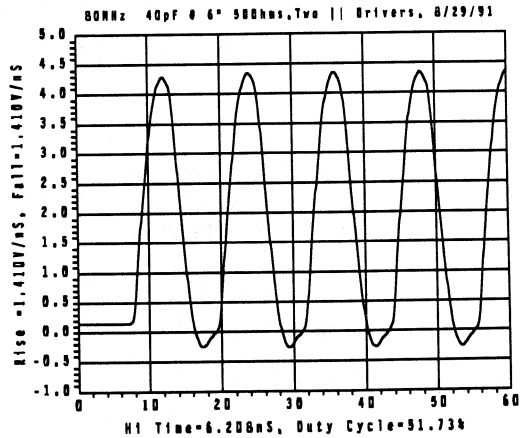
20 pF Load with 10" of Trace ($Z_0=50\Omega$)
Single Driver



20 pF Load with 10" of Trace ($Z_0=70\Omega$)
Single Driver



40 pF Load with 6" of Trace ($Z_0=50\Omega$)
Two Drivers in Parallel



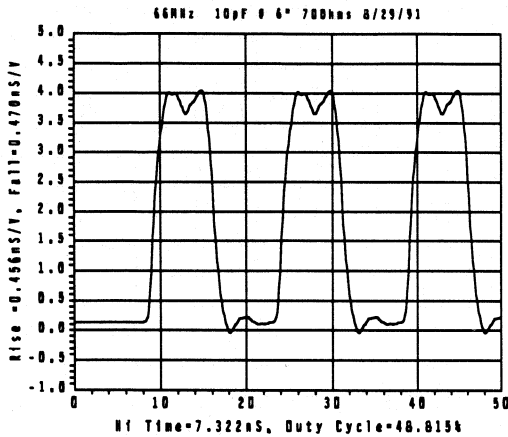
APPENDIX-C

Spice Simulation of Output Waveforms

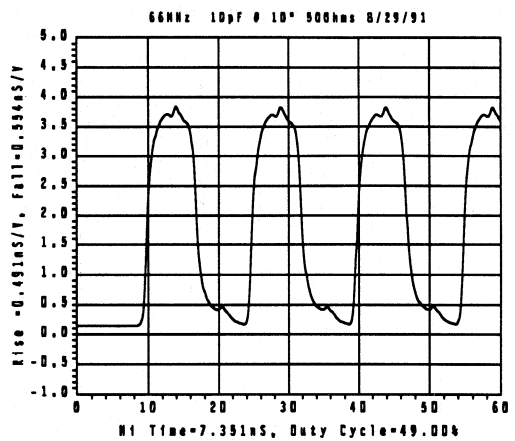
Modeled Frequency – 66MHz

(X-Axis is in ns)

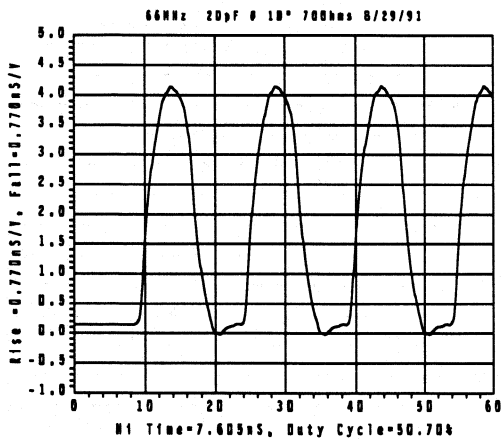
**10 pF Load with 6" of Trace (Zo=70Ω)
Single Driver**



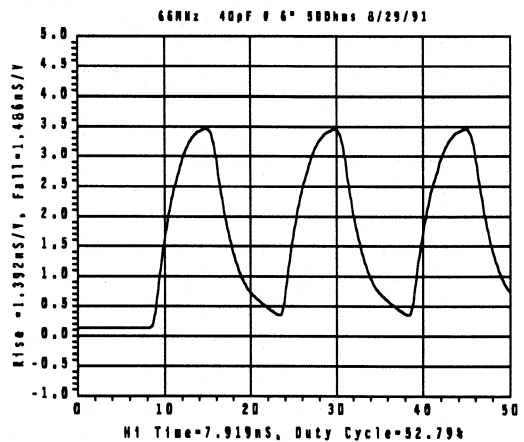
**10 pF Load with 10" of Trace (Zo=50Ω)
Single Driver**



**20 pF Load with 10" of Trace (Zo=70Ω)
Single Driver**



**40 pF Load with 6" of Trace (Zo=50Ω)
Two Drivers in Parallel**



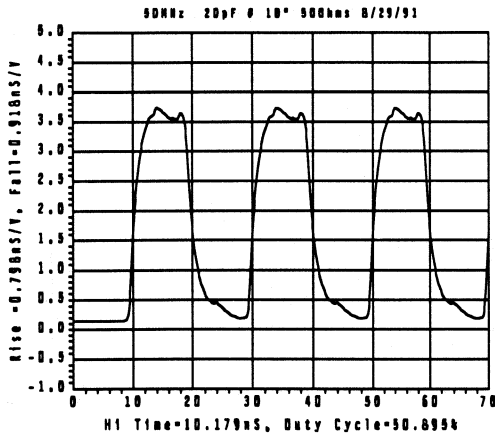
APPENDIX-C

Spice Simulation of Output Waveforms

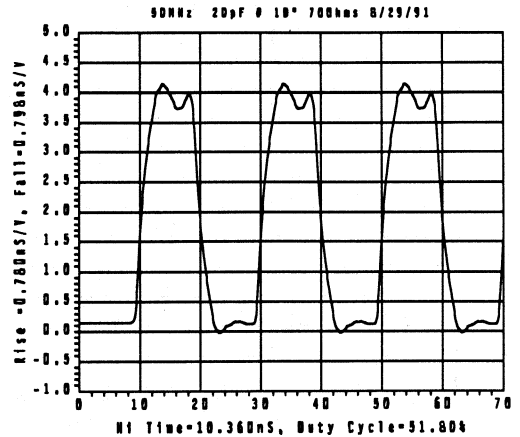
Modeled Frequency – 50MHz

(X-Axis is in ns)

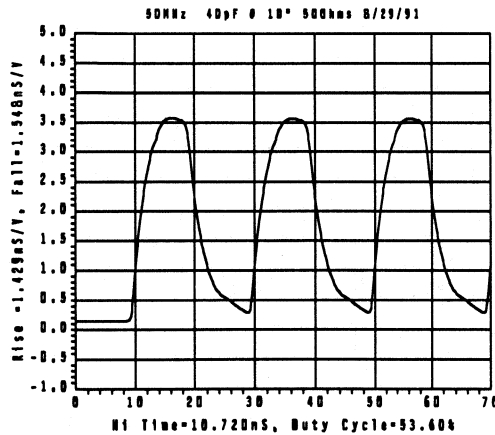
20 pF Load with 10" of Trace ($Z_0=50\Omega$)
Single Driver



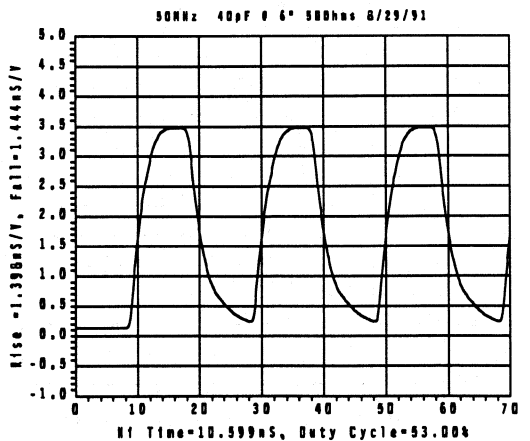
20 pF Load with 10" of Trace ($Z_0=70\Omega$)
Single Driver



40 pF Load with 10" of Trace ($Z_0=50\Omega$)
Single Driver



40 pF Load with 6" of Trace ($Z_0=50\Omega$)
Two Drivers in Parallel



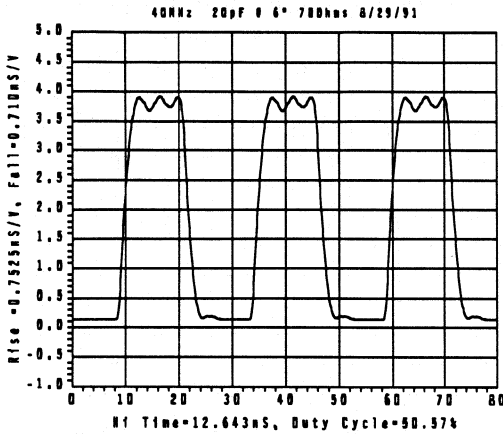
APPENDIX-C

Spice Simulation of Output Waveforms

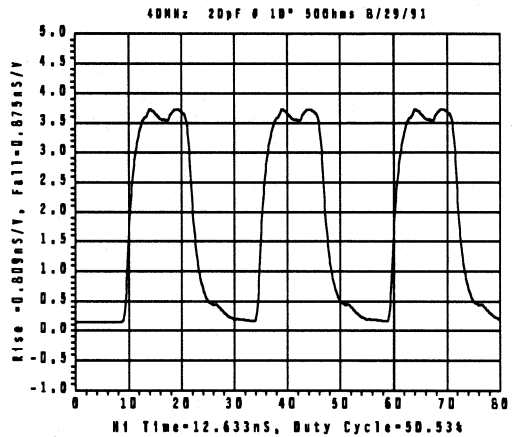
Modeled Frequency – 40MHz

(X-Axis is in ns)

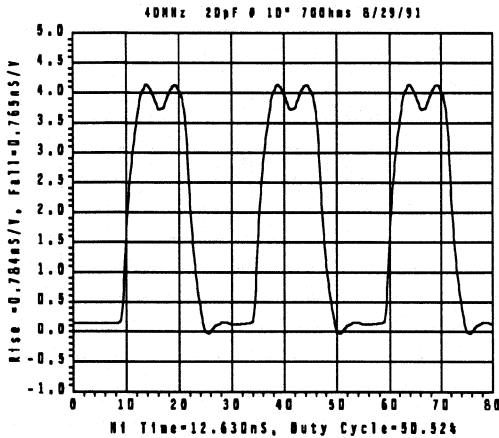
**20 pF Load with 6" of Trace (Zo=70Ω)
Single Driver**



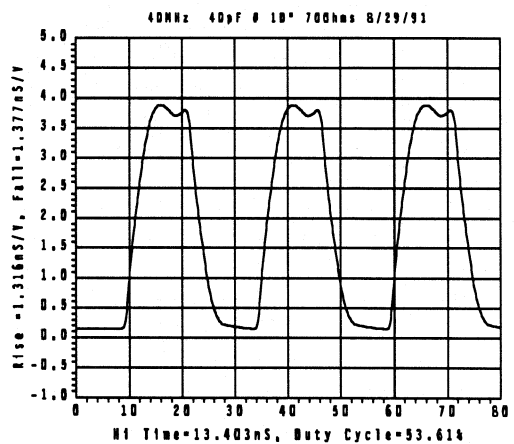
**20 pF Load with 10" of Trace (Zo=50Ω)
Single Driver**



**20pF Load with 10" of Trace (Zo=70Ω)
Single Driver**



**40 pF Load with 10" of Trace (Zo=70Ω)
Single Driver**



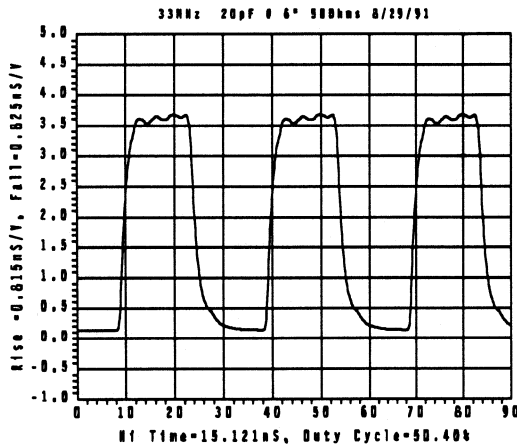
APPENDIX-C

Spice Simulation of Output Waveforms

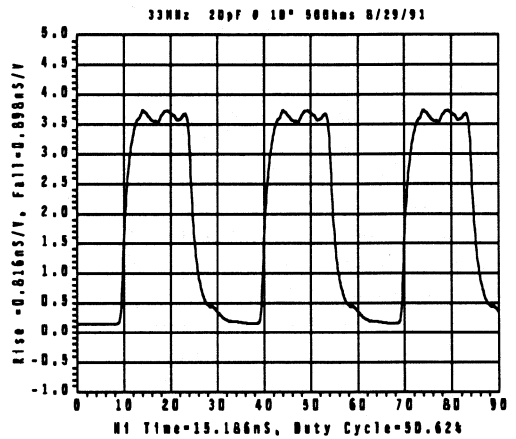
Modeled Frequency – 33MHz

(X-Axis is in ns)

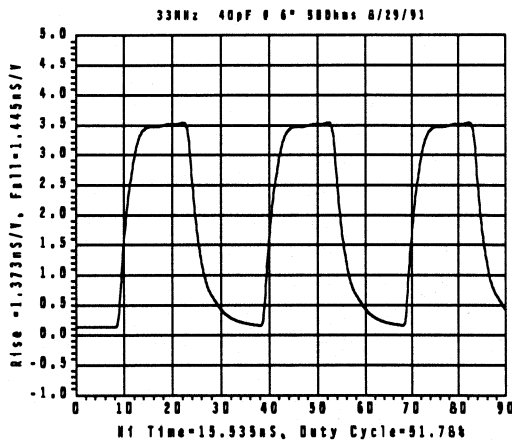
20 pF Load with 6" of Trace ($Z_0=50\Omega$)
Single Driver



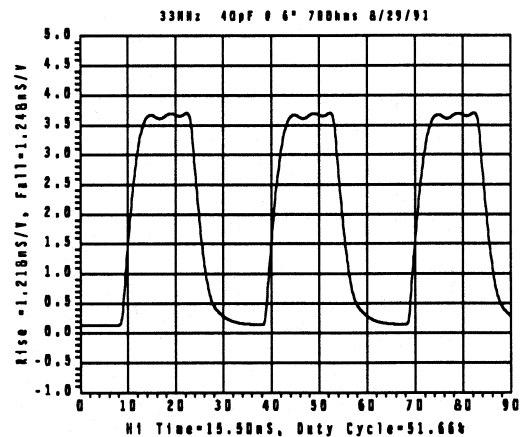
20 pF Load with 10" of Trace ($Z_0=50\Omega$)
Single Driver



40pF Load with 6" of Trace ($Z_0=50\Omega$)
Single Driver



40 pF Load with 6" of Trace ($Z_0=70\Omega$)
Single Driver



Clock Design In Intel Pentium™ Processor Systems using the SC3508

M.K. Williams
Owner/Principal Consultant
Amherst Systems Associates

1. INTRODUCTION

The Pentium processor is the latest, high-performance entry in the X86 microprocessor family from Intel. There are 60- and 66-MHz versions. It operates on 64-bit data in two instruction pipelines with instruction prefetching and branch prediction. There is also on-board floating-point processing, as well as sophisticated data and instruction caching. These are all structural elements that, until very recently, were found exclusively in main-frame and supercomputer designs.

At the hardware level, Pentium designs also have a good deal in common with larger computer system designs. For example, the tighter timing margins and the higher clock and edge speeds of Pentium designs dictate the careful application of high-speed digital design methods. This includes employing design methods which preserve the fidelity of the clock pulse and effectively manage the tolerances present in the circuitry which distributes or receives the system clock.

The purpose of this application note is to clearly illustrate an approach to the design of the system clock for the Pentium using the AMCC SC3508. We will methodically work through a simple but representative example. In doing so, we will identify the important design decisions encountered in the design of a correctly timed system, and show methods for resolving them.

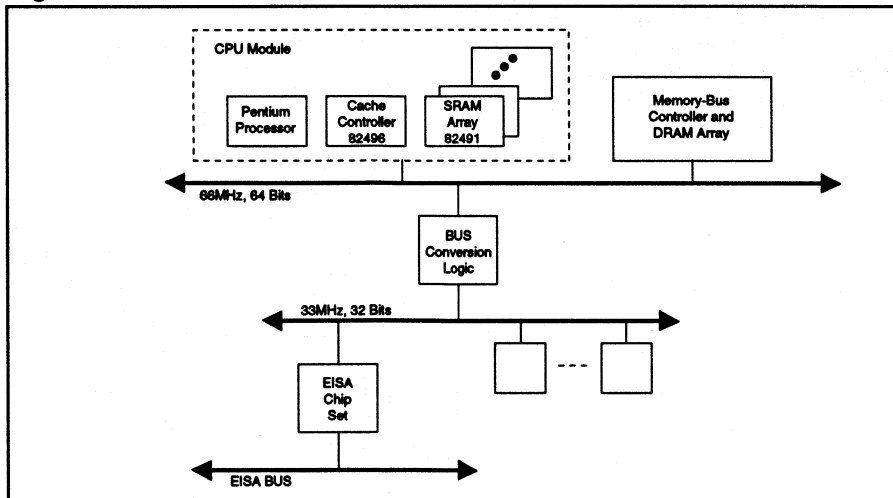
A Word About Specifications

In this document, we make use of a number of Pentium specifications. The reader is cautioned to verify any specifications with Intel prior to applying them, since they are all subject to change. It is also the responsibility of the designer to exercise sound engineering judgment to determine the suitability of how any particular specification or method is to be employed in his design.

2. DETERMINING YOUR DESIGN REQUIREMENTS

The first step in specifying the design of the clock for a Pentium, or any other system, is to clearly define what the design requirements are. Some of these will come from Intel specifications while others will be determined by aspects of the design, such as critical delay paths. In this section, we present some background on the

Figure 1.



mechanisms we are trying to manage and how to quantify the impact of those mechanisms on the design.

2.1. Timing-Environment Design: Fundamentals

The fundamental goal for any timing environment design is the specification of a *statistically stable* design. That is, it is assumed that the elements from which each system will be assembled will have some statistical distribution on their characteristic parameters (in our case, delay). Since many copies of the design will be fabricated, we must employ design methods which recognize this tolerancing and which ensure that every clock signal in each machine built arrives within the time interval predicted at design-time.

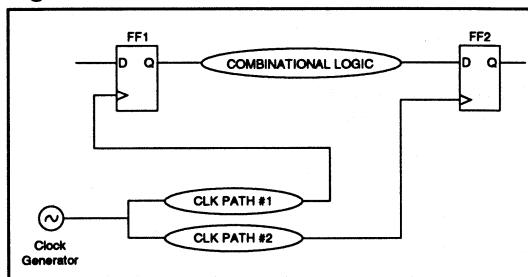
2.1.1. Basic Requirement on Clock-Arrival Time

We will use Figure 2, which shows a critical path, to illustrate the tolerancing effects we are concerned with controlling. Given that the two clock paths are built from components which have some statistical delay distribution, we can describe two pathological situations:

1. Clock-path 1 is slower than anticipated
2. Clock-path 2 is faster than anticipated

For the first case, FF1 is clocked late causing the data to arrive at FF2 after FF2 samples its input. The result is that the data is missed or the flip-flop enters a metastable state. The second case results in an equivalent situation by again clocking FF2 early relative to the arriving data. We can see from this simple example that any mechanism which causes the delay of a clock

Figure 2.



path to vary by more than the designer anticipated can result in a failure. Notice that it is *delay variation*, rather than the magnitude of the delay that results in timing failures.

2.1.2. Basic Clock-Tolerancing Mechanisms

As we just saw, we must manage anything which can result in unequal or inconsistent arrival times of the clock at the load. This equates to two important design tasks:

1. Precisely balance the mean delay along every path from the clock generator to the clock loads.
2. Anticipate and manage those mechanisms which tend to alter the delay along these paths.

The merit of balanced mean delays for all clock paths is illustrated by Figure 3. Since the worst-case tolerance is computed from the earliest and latest arrivals, balancing the mean delays moderates the impact of any statistical delay variations.

We will use Figure 4 to illustrate the various tolerancing mechanisms we are attempting to manage. The figure shows a clock-buffer driving a transmission-line which terminates at some clock-input. This circuit is representative of a complete clock path for many Pentium systems (i.e. one-level buffering). Given Pentium speeds (66-MHz clock rates and fast clock edge rates),

Figure 3.

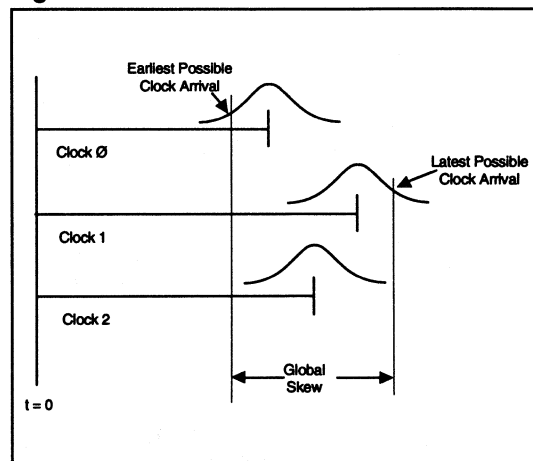


Figure 4.

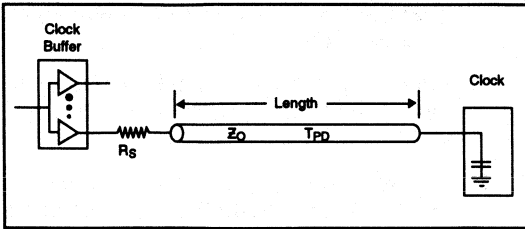
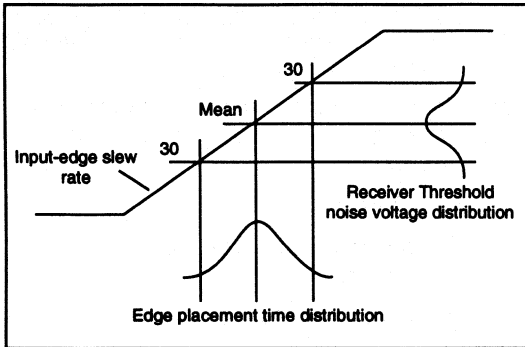


Figure 5.



a controlled-impedance interconnect is required. For this clock net, the expression for the variation in delay along the net is:

$$\text{Tolerance} = \text{Intrinsic skew} + \text{Extrinsic skew} + \text{Jitter} \quad (1)$$

Where ,

Intrinsic Skew is the delay variation in the clock buffer. This is usually specified separately for part-to-part and pin-to-pin skew. Some clock buffers also specify skew within a group of clock-buffer outputs. Assuming a single-chip solution, we will use pin-to-pin.

Extrinsic Skew is delay variation attributable to effects in the interconnect.

Jitter is the cycle-to-cycle variation in the arrival-time of the clock. It is due primarily to noise in the power environment which, in turn, causes time-varying shifts in the input threshold of a device. The relationship between noise and edge-placement (jitter) is shown in Figure 5. For more information on jitter, see References 1 and 2.

Extrinsic skew is not a single mechanism. It is convenient to break it into three major components:

$$\text{Extrinsic skew} = \Delta\text{TOF} + \Delta\text{Dist_Del} + \text{MT} \quad (2)$$

Where,

ΔTOF is the **variation in the time of flight** of an undistorted signal. This is due primarily to variation in line lengths, and does not include additional delay variation attributable to edge degradation. This effect is addressed by equalizing all clock net lengths to that of the longest clock net.

$\Delta\text{Dist_Del}$ is the **distortion-delay variation**. As a signal propagates, some of the high-end spectral content is attenuated. One prominent cause of this is the capacitance of the clock load. This results in a slower or degraded edge, and ultimately additional delay in reaching threshold voltage. Any variation in edge degradation (e.g. ΔC_L) results in a variation in delay. This is $\Delta\text{Dist_Del}$.

MT is the **manufacturing tolerance** on the delay. It ranges from one's of psec/in to mid-10's of psec/in.

The expression can be rewritten as:

$$\text{Tolerance} = \text{Int skew} + \Delta\text{TOF} + \Delta\text{Dist_Del} + \text{MT} + \text{Jitter} \quad (3)$$

From transmission-line theory, we know that the propagation rate of a loaded transmission-line is:

$$T_{PD}' = T_{PD} \sqrt{1 + C_L / (L * C_0)} \quad (4)$$

Where,

T_{PD} is the propagation rate of the unloaded transmission-line.

C_L is the load capacitance (may be distributed)

L is the length of the line

C_0 is the intrinsic capacitance of the line

And the delay (time of flight plus distortion-delay) of a loaded transmission-line is simply:

$$LT_{PD}' = L * T_{PD} \sqrt{1 + C_L / (L * C_0)} \quad (5)$$

If we know the minimum and maximum values for C_L , we can compute the min and max delays for a given lossless transmission line (exclusive of manufacturing tolerances).

$$\Delta LT_{PD}' = L * T_{PD} \left(\sqrt{1 + C_{Lmax} / (L * C_0)} - \sqrt{1 + C_{Lmin} / (L * C_0)} \right) \quad (6)$$

And we can use the difference in these values to replace the second and third terms in expression (3):

$$\text{Tolerance} = \text{Int skew} + \Delta LT_{PD}' + \text{MT} + \text{Jitter} \quad (7)$$

We will use this expression to compute the tolerancing of various "tolerance groups" later in the example. One very important effect to note is that the preceding expression implies that clustering loads which have non-trivial load-capacitance variation on a single clock net will drive the $\Delta LT_{PD}'$ factor up and thus the overall tolerance.

2.1.3. Design Flow/Approach

There are a variety of approaches one can take:

Clocks first - Specify in detail the clock distribution and use resultant tolerances to compute delay margins on critical paths ($T_{cyc} - T_{tol} = \max T_{path}$).

Critical paths first - Design critical paths and use the resultant maximum delays to compute timing margins ($T_{cyc} - T_{path} = T_{tol}$).

Most designers will take an approach that iterates between both styles, ensuring that both the timing and path delays are equally prioritized. In our example design, we are starting with critical-path information to determine timing margins, and then using the margin information to establish constraints on critical-path parameters (e.g. allowable load-capacitance variation on external loads). In detail, our decision-flow is as follows:

1. Determine allowable tolerances in CPU module.

2. Use critical path information to determine allowable clock tolerance (i.e. margin) on external loads.
3. From an inventory of clock loads, determine your slowest clock path in the system.
4. Starting with your tightest tolerance group (Pentium-82496), begin designing clock nets. Make each net approximately as long as that of the slowest path (previous step). As you progress through other tolerance groups, ensure you balance the mean delays.
5. From the unused margin for each group, develop constraints for each of the following:
 - Jitter
 - Manufacturing tolerances on net delays
 - Load-capacitance variation

Three-Level Tolerance Specifications

The Pentium specification dictates tolerances within the CPU module at three voltage levels (0.8, 1.5, and 2.0V). This was most likely done to combine tolerance management and pulse-fidelity into a common specification. However, designing for minimum tolerancing at multiple voltage levels can be very difficult. For clarity, we will design for minimum tolerancing at 1.5V and employ methods which ensure good pulse fidelity. This will ensure that the tolerances are satisfied at all three levels.

2.2. Specific Pentium System Design Requirements

The degree of difficulty for any timing-environment design is derivable from two aspects of the design — the number of board-level clock loads and the fraction of the cycle time allocated to clock tolerancing. Broadly speaking, a design becomes challenging when the number of loads exceeds 10 and the total tolerancing is restricted to 10 to 15% of the cycle time.

For Pentium systems, the number of board-level clock loads varies according to the complexity of the design. For the most basic designs, the number of loads will be four to eight, primarily the Pentium processor and memory-bus controller. For very sophisticated designs (e.g. large server systems), with a second-level cache, as well as controllers for large interleaved memories and other synchronous devices, the number of board-level clock loads can exceed forty or more.

A typical 66-MHz design with a second-level cache will have 12 clock loads in the CPU module plus more loads for the memory bus controller (MBC) and other logic such as bus conversion. Therefore, depending upon how the MBC, etc. are implemented, a typical 66-MHz design will have 15 to 20 clock consumers.

The small fraction of the period allotted for tolerancing qualifies Pentium designs as quite challenging. At 66-MHz, the cycle time is 15 nsec. Clock tolerances within the CPU module are either 200 or 700 psec, and those external to it vary depending upon critical path delays to/from devices external to the CPU module. Stated another way, the tolerances within the CPU module are 1.3% and 4.7% of the cycle time.

For the rest of this section, we determine the various tolerances in a 66-MHz Pentium system with a second-level cache. The design requirements are configuration-specific and best considered in tolerance groups.

There are very few explicit clock requirements in the basic Pentium specification. Only clock stability (jitter) and pulse fidelity are specified.

Clock Stability (Jitter) - The Pentium clock must have a stability of better than +/- 250 psec. There are many metrics of frequency stability. While it does not explicitly state so, this specification refers to period-jitter. In a footnote to the specification, the distribution of the jitter in the jitter frequency spectrum excludes any peaking between 500kHz and 1/3 of the clock frequency (repetition rate).

Pulse Fidelity - The Pentium clock signal operates at TTL levels. The clock waveform must remain at the high and low levels for a minimum of 4 nsec, and the transition times must be less than 1.5 nsec. The Pentium specification dictates other clock waveform parameters beyond these. The reader is referred to the specification for complete information.

2.2.2. CPU Module

There are four possible configurations for the "CPU module". They are summarized in the following table.

Clock Speed (MHz)	Cache Size	Tolerance (psec)	Number of Loads
60 or 66	None	N/A	1 (CPU only)
66	256K	700	12 CPU, cache control, 10 SRAM
60	512K	800	20 CPU, cache control, 18 SRAM
60	256K	800	12 CPU, cache control, 10 SRAM

Layout Considerations Within CPU Module

There are flight-time specifications for various signal groups within the CPU module. For example:

Pentium - 82496: Only max flight times are specified (1.6 nsec is smallest value).

Pentium - 82491: Min and max flight times are specified (1 - 2.2 nsec range for 66-MHz).

These flight-times are critical, and it is likely that they will drive the placement of devices within the CPU module. That placement, in turn, will interact with clock tolerancing within the CPU module, since the distances from the clock driver to the clock loads determine certain tolerancing components. Specifically, interconnect tolerancing increases with the length of the

clock nets. For our example, we will use the configuration for the layout of the CPU module found in the Intel Pentium clock application note (Reference 8). There may be another approach (e.g. locating the clock driver in the center) that results in additional timing margin.

**Pentium-82496 Tolerance Group:
Two Loads at 200 psec Tolerance**

This requirement is very tight and essentially unheard of in microprocessor systems. To meet

this specification, both loads must be driven by the same pin of clock buffer. This eliminates the intrinsic skew component of the tolerance. By locating the Pentium and 82496 clock pins close to each other, and moving the branching point to the end of the transmission line (versus stubbing into two lines near the clock buffer), it is possible to minimize the manufacturing tolerance. The 200 psec tolerance thus splits between jitter and arrival time variation due to load capacitance variation.

Are there two different jitter specifications for the Pentium?

There can be some confusion in systems with second-level caches, since there appear to be two conflicting jitter specifications. This, however, is not the case:

The Pentium clock specification states that the maximum allowable instability (jitter) on the clock to the Pentium processor is +/- 250 psec. Further restrictions as to how this energy can distribute across the jitter spectrum are also specified in a footnote.

When the Intel CPU-Cache chip set is employed, the maximum tolerance between the clock signals driving the Pentium and the 82496 is limited to 200 psec. That is, for systems with second level-caches, the sum of the skew and the jitter between the clock signals driving the cache controller and the Pentium must be less than 200 psec.

Actually, there is no conflict in these specifications once you determine what they represent. The former jitter specification (+/- 250 psec) is established by the timing requirements of segments 100% internal to the Pentium. Any displacements larger than 250 psec run the risk of an internal Pentium timing failure. Furthermore,

the requirements on the jitter spectrum are in place to prevent stimulating the resonant frequency of the loop filter in the internal PLL clock receiver. When jitter causes the PLL loop-filter to resonate, the signal out of the PLL (i.e. the internal clock) has more jitter on it than the signal driving into the PLL (i.e. the Pentium clock input), and is possibly larger than acceptable.

The latter specification (200 psec) governs the timing of segments between the Pentium and the 82496. When that specification is violated, timing failure on one of the paths which span both chips is likely.

How do you use this information?

In systems without second-level caching, the latter specification(200 psec) does not apply. Assuming there is sufficient margin on all paths external to the Pentium, system jitter must be less than +/- 250 psec and distributed in the jitter spectrum as specified in the footnote.

In systems with second-level caching, the 200 psec specification sets the upper limit on the jitter amplitude (jitter < 200 psec - Pentium/82496 skew). Furthermore, the jitter must distribute through the jitter spectrum as specified in the Pentium clock specification.

Pentium-82491 & 82496-82491 Tolerance Groups: 10 SRAM (+2) Loads at 700 psec Tolerance

This group has many more clock loads, which necessitates driving the group by more than one pin of the clock buffer. Much of the margin obtained by increasing the tolerance specification to 700 psec is absorbed by the increased intrinsic skew. There will also be a more significant manufacturing tolerance contribution, since the SRAMs are more widely dispersed on the board and there will be more inches of interconnect in the clock nets that drive them.

Since we are forced to increase the intrinsic skew term of the total tolerance in this group, we want to use a point-to-point scheme (1 load/net). This reduces the range of load-capacitance variation and minimizes the ΔLT_{PD} .

2.2.3. External Tolerance Groups

There will also be clock consumers external to the CPU module. In more complex Pentium designs, the number of loads in the external tolerance group can be several times the number of loads within the CPU module. The primary external clock loading will be in the memory bus controller (MBC). The tolerance requirements of this group will be dictated by the critical paths in this part of the design. Shortly, we will provide a simple example of computing that tolerance.

The majority of logic external to the CPU module is treated as memory. From a timing perspective, there are three distinct ways in which system memory can be configured:

1. Fully Synchronous
2. Divided Synchronous
3. Asynchronous

This impacts the clock as follows:

Fully synchronous systems: All clock inputs driven at 66-MHz

Divided-synchronous systems: All clock inputs in CPU module driven at 66-MHz, the memory-bus controller driven by both 66- and 33-MHz clocks, and all external devices driven by a 33-MHz clock.

Asynchronous systems: The CPU module and part of the MBC driven by 66-MHz clocks. A second, relatively-asynchronous clock (generated elsewhere in the system) drives part of the MBC and all external devices.

3. DESIGN EXAMPLE

3.1. Configuration

Our example system will be a fully synchronous 66-MHz system with a 256k second-level cache. It will use the Intel 82496 Cache Controller and 82491 Cache SRAMs. This configuration embodies many of the most challenging aspects of a Pentium clock design — the extremely tight tolerancing of the clocks within the CPU module, non-trivial load-capacitance variation, and determination of critical paths external to the CPU module. Furthermore, it will be extended to address other important design decisions — dual-frequency clocking and larger numbers of clock loads.

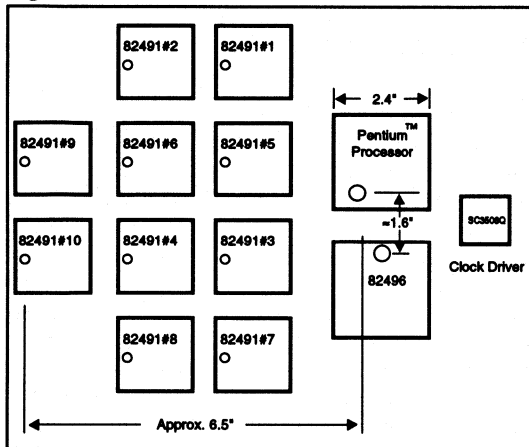
3.2. Preliminary Design Decisions

Before beginning to work through our example design, we will first describe some preliminary design decisions, and the impact they have on the system clock.

Clock-Buffer Selection - We are using an AMCC SC3508Q-1 clock buffer to drive the clock in this example. Our selection criteria for this part is based upon two factors. Specifically, that the SC3508Q-1 has twenty outputs and that the pin-to-pin skew for this part is less than 500 psec. In second-level cache systems, we have to drive 12 loads which have a non-trivial (relative to the tolerance requirement) amount of capacitive load variation. With 20 pins available from the SC3508Q-1, a single-IC point-to-point (i.e. one driver pin for each clock load) clock-distribution solution can be employed. If these loads had to be driven such that two or more SRAM inputs were clustered on a net, the arrival-time variation due to extrinsic skew and C_L effects (c.f. expressions 6 and 7) would exceed the allowed tolerance, even without factoring-in jitter.

Device Placement Within the CPU Module - We will use the placement suggested by Intel in Reference 8. Figure 6 shows that placement.

Figure 6.



Interconnect Environment - For our speeds and spectral content, we obviously need a controlled-impedance interconnect. The reader is referred to References 3 and 10 for detailed background information on this topic.

Microstrip vs stripline - We are routing all clock signals in microstrip, since the propagation rate is higher than that of stripline (146 psec/in for microstrip versus 182 psec/in for stripline). While the twenty or so clock nets may increase the level of radiated noise, the faster rates reduce the impact of interconnect manufacturing tolerances (5% of 146 is less than 5% of 182).

Parameters - Our example assumes a 70-ohm characteristic impedance. Higher values of Z_0 reduce the dynamic current available to charge the load capacitance. This, in turn, results in higher sensitivity to load capacitance variation. However, lower dynamic current also means less noise and therefore less jitter. The other parameters for our assumed interconnection environment follow.

Structure: Microstrip

Dielectric: 4.7 .012" thick

Conductor: .011" W x .0015" T copper

Properties:

C_0 2.08 pF/in

L_0 10.3 nH/in

Z_0 70.4 ohms

T_{pd} 146.4 psec/in

Definition of External Loading and Tolerance - For any design, it is necessary determine the allowable clock tolerance on external critical paths. To do that, you have to identify the critical paths in the external circuitry. This may be quite difficult, given the large number of bus-transaction types, and that not all segments are 1-cycle long.

To simply illustrate what is required, we will assume we have identified the external critical path as shown in Figures 7 and 8. That is, the critical path runs from the fictitious Pentium output P5_OUT through two PLDs and into the fictitious inputs P5_IN and CC_IN. The delays through the PLDs have been arbitrarily assumed to be 3.5 and 3.2 nsec. For simplicity, we as-

Figure 7.

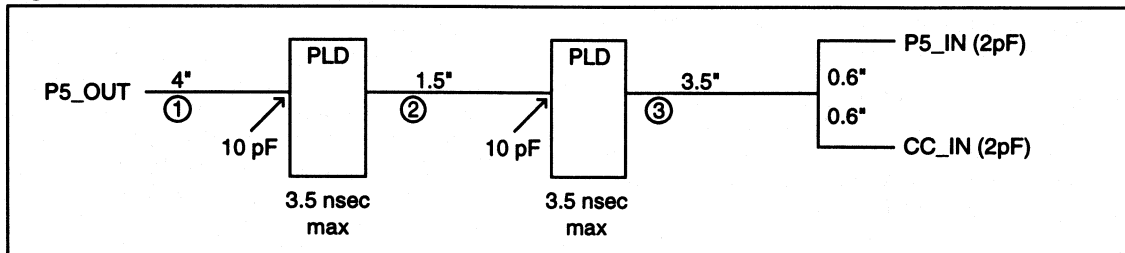
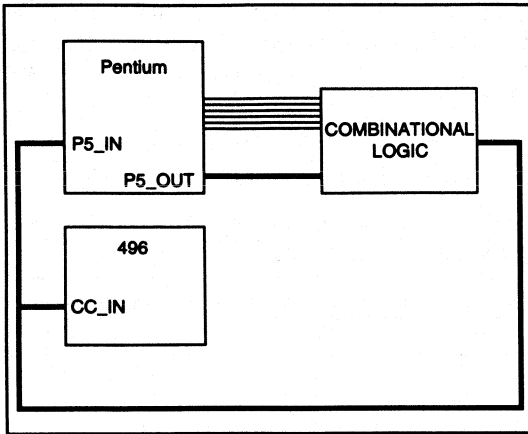


Figure 8.



sume P5_OUT is valid on the rising edge of the clock (add appropriate delay if this not the case for your system). Furthermore, we will assume the setup-time for both inputs is 5 nsec. Computing the path delay:

Segment 1

From our previous discussion, we can compute the delay of a loaded transmission line from expression (5). Using $C_L = 10$ pF (hopefully a maximum value), $L = 4"$, and our previous values for the remaining variables, we have:

$$\begin{aligned} \text{Delay}(\text{segment 1}) &= (4")(146.4\text{ps/in}) \\ &\frac{\sqrt{1 + (10\text{pF})/(4" * 2.08\text{pF/in})}}{} \\ &= 868 \text{ psec} \end{aligned}$$

Segment 2

Using the same method, we compute:

$$\text{Delay}(\text{segment 2}) = 450 \text{ psec}$$

Segment 3

For this segment, we analyze the capacitive effects of the two 0.6" segments as a single 1.2" segment with twice the load capacitance:

$$\begin{aligned} \text{LT}_{PD}' &= (3.5+.6) * (146.4)" \\ &\frac{\sqrt{1 + (2+2)/((3.5+1.2) * (2.08))}}{} \\ \text{Delay}(\text{segment 3}) &= 713 \text{ psec} \end{aligned}$$

Computing the critical path delay, T_{CPD} :

$$\begin{aligned} T_{CPD} &= \text{Max gate delays} + \\ &\text{Max net delays} + MT^* \quad (8) \end{aligned}$$

where, MT^* is an estimate of the maximum positive manufacturing tolerance.

$$\begin{aligned} T_{CPD} &= (3.5 + 3.2) + (.868 + .450 + .713) + \\ &9.6 * (20 \text{ psec/in}) \\ &= 8.923 \text{ nsec} \end{aligned}$$

Computing the available clock tolerance, TOL_{EXT} :

$$\begin{aligned} TOL_{EXT} &= T_{CYC} - T_{CPD} - \text{Setup-time} \quad (9) \\ &= 15 - 8.923 - 5 \\ &= 1.077 \text{ nsec} \end{aligned}$$

We will make use of this figure later in the example.

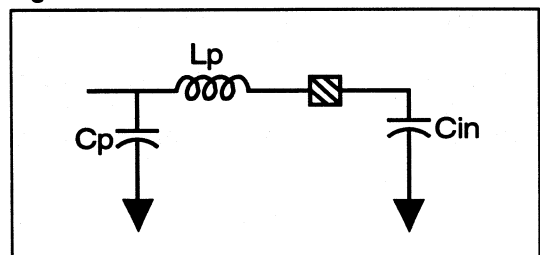
3.4. Inventory of Loading and Placement of Clock Loads

As the expressions illustrated earlier, variation in load-capacitance can be a principal contributor to clock tolerancing. We will see that in Pentium systems with second-level caching, this effect will dominate in the CPU module.

Loading in CPU Module

Intel has characterized the high-frequency behavior of the pins of the devices in the CPU module. Reference 7 provides models for all input pins in the CPU module (it also has output models). The model is shown in Figure 9. The values for the components are shown in Table 1. When analyzing various design approaches with a good simulation tool, these models will contribute to a more accurate answer. They are especially useful since minimum and maximum

Figure 9.



values are provided instead of typical values. However, since the model is a third-order low-pass filter which is driven by a transmission-line with its own distributed reactive components, we need to simplify it for our manual calculations here. Our transmission-line delay expressions employ a single, lumped load capacitance. So we need to estimate minimum and maximum values for input capacitance from the data in the table.

Table 1 - Component Values for Input Pin Models

Device	Buffer Type	C _p (pF) Min/Max	L _p (nH) Min/Max	C _{in} (pF) Min/Max
Pentium*	ER3	1.6/2.2	6.2/8.4	1.7/2.3
82496	ER8	1.4/1.9	5.8/7.9	2.4/3.3
82491	ER11	0.5/1.5	6.9/9.3	2.9/3.9

* Ignore 7pF maximum input capacitance rating from DC specification when using these models.

We are concerned about the time at which V_{IN}, the voltage across C_{IN}, charges up to threshold. An edge arriving at the pin on the transmission line can be considered as the sum of several sine-waves - the fundamental (66-MHz) and the harmonics (up to about 250-MHz). The elements of the filter attenuate or resist the high-end spectral components more than the lower ones, degrading the edge and delaying the time V_{IN} charges up to threshold. The fastest time will be when the high-end spectra is attenuated the least, the slowest time when it is attenuated the most. We can assume that the least attenuation will occur when both capacitors and the inductor are at minimum values. If we let the inductance go to zero, the capacitors are in parallel and we can simply add them. This assumption will result in a slightly faster estimate of the arrival time, since the inductor would limit some of the current which charges C_{IN}. The slowest time will occur when both capacitors and the inductor are at their maximum values. In this case, we can simplify, and still account for the effect of the inductor (resisting the passage of the current which charges C_{IN}), by letting the inductance go to zero

but scaling C_{IN} up to increase the charging time. Our assumption is that scaling C_{IN} up by 50% will account for the elimination of the inductor. So our maximum value for the pin capacitance will be computed as:

$$\max C_{PIN} = \max C_p + 1.5(\max C_{IN}) \quad (10)$$

The values we will use are shown in Table 2.

Table 2 - Simplified Pin-Capacitance Values

Device	C _{MIN} (pF)	Typical C _L
Pentium	1.6 + 1.7 = 3.3	2.2 + 1.5(2.3) = 5.7
82496	1.4 + 2.4 = 3.8	1.9 + 1.5(3.3) = 6.9
82491	.5 + 2.9 = 3.4	1.5 + 1.5(3.9) = 7.4

Placement of Loads in CPU Module

Since we are assuming the placement suggested in Reference 8, we can derive the distance to loads from that. The shortest path from the clock driver to either the Pentium or 82496 clock pins is approximately 2 inches. The nearest and farthest 82491s to the clock buffer are approximately 5 and 7.5 inches, respectively.

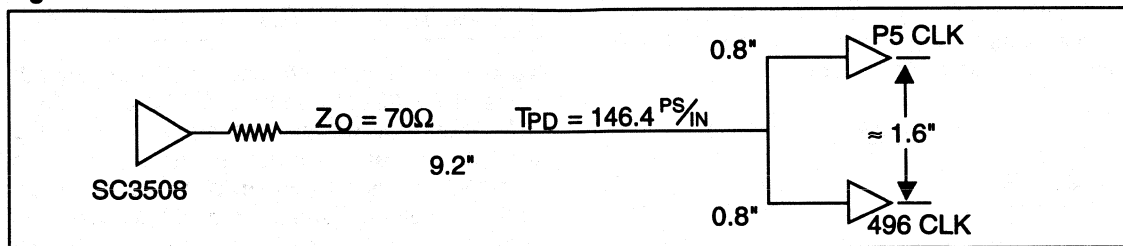
Loading Outside CPU Module

Assumed placement and loading for the external clock loads is shown in Table 3. It is obvious from the table that either load 1 (largest capacitance value) or load 3 (most remote load) will be our worst case load. Note that we have assumed only typical values for C_L. We would obviously like to have min/max values, but this is usually not available.

Table 3 - External Clock Loads

Load	Estimated Min Distance Clk buffer to load	Typical C _L
1	4"	10pF
2	5"	2pF
3	10"	5pF
4	5.5"	5pF
5	4"	2pF

Figure 10.



3.5. Pentium/496 Tolerance Group

Requirement: 200 psec

Structure of Clock Net: This tolerance is sufficiently tight that both loads must be driven off the same pin of the clock buffer to eliminate extrinsic skew (500 psec for the SC3508Q-1). Examining the clock-load inventory from the previous section, we see that the longest clock net will probably be about 10". This will be our starting point for this and all subsequent nets. Nets can be serpentine to use up extra length. The layout of the CPU module tells us the two loads are about 1.6" apart. From this, we will assume the structure for our clock net as shown in Figure 10. The branching point for the stubs has been moved as far out on the transmission line as possible to reduce manufacturing tolerance effects between these two loads.

Analysis: For approximately 1.5 nsec transition times, the 9.2" segment of the line can be treated as a transmission line (i.e. an edge doesn't "know" about a load until it gets there). We can expect the edge to propagate down the 9.2" segment at the unloaded propagation rate, which is 146.4 psec/in. Therefore, we can analyze it and the stubs separately. The stubs are short enough to treat as equipotential nodes. We will treat the two loads as a single capacitive load equal to the sum of the two input capacitance ranges.

$$\begin{aligned} \text{Net Delay} &= \text{Delay of long segment} + \text{Stub delay} \\ &= 9.2" \cdot \text{Unloaded } T_{PD} + \text{Loaded stub delay} \\ &= 1347 \text{ psec} + L \cdot T_{PD} \sqrt{1 + C_L / (L \cdot C_0)} \end{aligned}$$

where,

$$L = 0.8" \text{ for either stub}$$

$$T_{PD} = \text{Unloaded propagation rate} = 146.4 \text{ psec/in}$$

$$C_0 = 2.08 \text{ pF/in (computed earlier)}$$

$$3.3 \leq C_L \leq 5.7 \quad \text{For Pentium input}$$

$$3.8 \leq C_L \leq 6.9 \quad \text{For 82496 input}$$

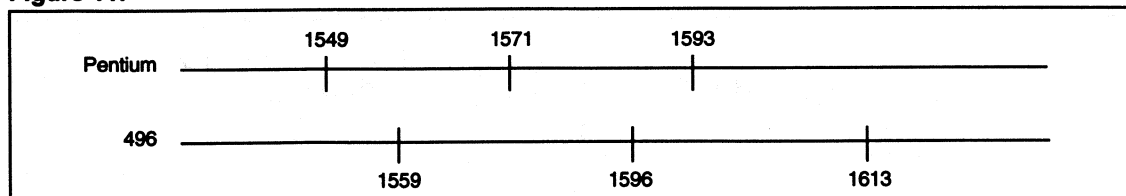
Computing the min and max delays for both paths (SC3508-Pentium and SC3508-82496), we have:

	Min	Max	Mean
Delay SC3508-Pentium	1549 1347+202	1593 1347+246	1571 1347+224
Delay SC3508-82496	1559 1347+212	1613 1347+266	1586 1347+239

Representing this graphically:

The difference between the earliest and latest arrivals is 1613-1549=64 psec. This leaves 200-64=136 psec margin for jitter and manufacturing tolerance on the stubs. We can improve this by aligning the mean delays. In this case, that means increasing the mean delay of the Pentium stub from 224 psec to 239 psec. And

Figure 11.



this is accomplished by lengthening the stub to the Pentium. Solving expression (5) for L, we find that a new Pentium stub length of 882 mils gives us the appropriate alignment.

	Min	Max	Mean
Delay SC3508-Pentium	1563	1609	1586
Delay SC3508-82496	1559	1613	1586

Tolerance: This is determined by the difference in arrival times. There are two cases (early Pentium/late 82496 and late Pentium/early 82496). Since we balanced the mean delays, both cases are identical.

Skew = 1613-1563 = 50 psec.

This should be guard-banded to accommodate manufacturing tolerances on the stubs. These tolerances will probably not be that large due to substantial tracking effects (i.e. these nets are all in the same area of the same layer of the same board). So we'll assume

Guarded skew = 65 psec.

This leaves 200-65 = 135 psec for jitter so far. Remember that these figures are just for clocks in this tolerance group.

3.6. Pentium/82491 and 82496/82491 Tolerance Group

Requirement: 700 psec.

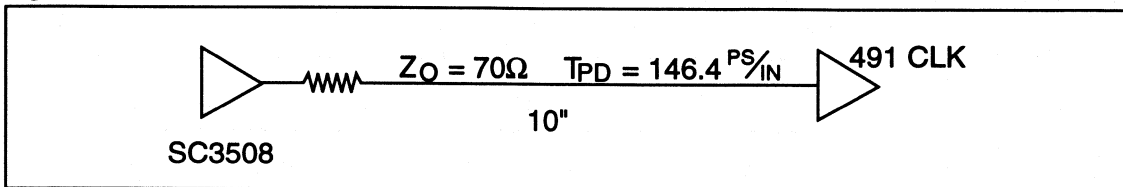
Structure of Clock Net: We will assume point-to-point for all SRAM nets to minimize C_L effects. The net will be as shown in Figure 12, with an approximate length of 10".

Analysis: Using

$$3.4 \leq C_L \leq 7.4 \quad \text{for 491s}$$

and forcing the mean delay to 1586 psec, we solve for a length of 9.621". The full set of delays is:

Figure 12.



	Min	Max	Mean
Delay SC3508-82491	1523	1649	1586

Tolerance: If the difference between arrival-times at the 82491s and the 82496 are acceptable, then they will also be acceptable for the difference between the Pentium and the 82491's. This is, of course, because the mean delays are aligned and the arrival time spread is wider at the 82496 than at the Pentium. So we will analyze with respect to the 82496. Using expression (7):

$$\text{Tolerance} = \text{Int skew} + \Delta LT_{PD}' + MT + \text{Jitter} \quad (7)$$

Substituting our 700 psec limit in for the tolerance

$$700 \text{ psec} \leq 500 + \Delta LT_{PD}' + MT + \text{Jitter}$$

$$200 \text{ psec} \leq \Delta LT_{PD}' + MT + \text{Jitter}$$

where,

$\Delta LT_{PD}'$ in this case is the worst case arrival time difference (due to C_L effects) between the 82496 and the 82491s. Again, we only have to compute one of the two possible cases due to symmetry.

$$\Delta LT_{PD}' = 1649 - 1559 = 90 \text{ psec}$$

Guard-banding this figure to accommodate manufacturing tolerances, we can assume

$$\text{Guarded skew} = 115 \text{ psec}$$

$$\text{Leaving } 200 - 115 = 85 \text{ psec for jitter.}$$

3.7. External Tolerance Group

Requirement: 1.077 nsec (computed earlier)

Structure of Clock Net: We will assume point-to-point for the external loads as well. This net will be identical to that shown in Figure 12.

Analysis: For this group, analysis will not yield the same quality result as it did for the preceding tolerance groups. The reason is that for this

group, it is highly likely that you can only get typical values for each load-type. Unfortunately, you require min/max information about load capacitance to compute arrival time variation. There are, however, some approaches that maximize the ability of the design to cope with uncharacterized tolerancing mechanisms. These include:

1. Point-to-point clock nets to minimize the C_L variation on any one net. Given that we have 20 outputs to work with on the clock buffer, this is not a problem for most Pentium designs.
2. Use the lowest possible Z_0 which produces the maximum dynamic current, and thus charges the load capacitance as fast as possible. Reference 2 elaborates on the sensitivity of tolerancing to transmission-line characteristic impedance and variation in load-capacitance.
3. Extending the "charge current" logic applied in the previous point to termination, it is generally advisable to select a termination scheme other than series. The SC3508Q-1 employed in our example design has integral series termination. However, the benefit of point-to-point distribution afforded by the SC3508Q-1's twenty output pins outweighs the impact of series termination.
4. Design each external clock net such that its delay, as computed with typical C_L values, is aligned with the mean delay value of the CPU module.
5. Bypass heavily and use other noise reduction methods to minimize clock jitter at that load, *and* devices it communicates with.

From our earlier computations, we know the maximum allowable tolerance for the external tolerance group is 1.077 nsec. This is the maximum arrival-time difference between either the

Pentium and any external load, or the 82496 and any external load. Note that instead of treating all external clock loads identically, we could separately analyze for each load, if necessary.

Computing the mean delay for external load #3 first:

$$LT_{PD}' = L * T_{PD} \sqrt{1 + C_L / (L * C_0)} \quad (5)$$

Where we will substitute:

$$L = 10''$$

$$C_L = 5\text{pF typical}$$

We get a typical delay of 1631 psec. We need to adjust something so that this typical delay aligns with the mean in the CPU module of 1586 psec. We can add delay to all the other nets or possibly reduce the delay of this net. Let us assume we can take the latter approach by slightly repositioning the SC3508 relative to this load. To align the delays, the length of this net must be 9.698" (computed by forcing the loaded delay in (5) to be 1586 psec).

At this point, we may also want to consider reducing Z_0 . Repeating the preceding for all the other external loads:

Load	Estimated Min Clock-Net Length	Typical C_L	Actual Length
1	4"	10pF	8.693"
2	5"	2pF	10.363"
3	10"	5pF	9.698"
4	5.5"	5pF	9.698"
5	4"	2pF	10.363"

3.8. Final Design Decisions and Summary

At this point we have "finished" the design of the clock nets. We still have some constraints to compute, which we will do in this section. However, in the event that an unachievable constraint results, it would be necessary to rework the layout of the loads and the lengths of the clock nets.

Jitter, Noise, and External C_L Constraints

The following summarizes the tolerancing for the nets we have just designed:

Tolerance Group	Intrinsic Skew (pin-pin) (psec)	Extrinsic Skew w/ mfg. tol (psec)	Tolerance Constraint (psec)	Jitter Constraint (psec)
Pentium-82496	0	65	200	135 200-65
Pentium-82491	500	< 115*	700	> 85 700-500-<115
82496-82491	500	115	700	85 700-500-115
82496-EX1	500	???	1077	???
82496-EX2	500	???	1077	???
82496-EX3	500	???	1077	???
82496-EX4	500	???	1077	???
82496-EX5	500	???	1077	???
82496-EX6	500	???	1077	???

* - By examination.

System Jitter Constraint - Given the complete information we have about the loads in the first two tolerance groups, we were able to compute jitter constraints. This was done using expression (7). While jitter can be considered to vary from location to location in a system, it is a much more manageable problem to assume it is uniform throughout the system. So, for our example, we will assume a jitter constraint of

$$\text{System Jitter Constraint} = \text{Min}(135, <85, 85) = 85\text{psec}$$

Therefore, we will limit jitter to 85 psec on a system-wide basis. Given the $1077 - 500 = 577$ psec of room we have for combined jitter and extrinsic tolerancing in the external tolerance group, it is not likely we will need to control jitter to a lower level. We will now use our jitter constraint to compute the extrinsic skew constraint on the external loads and an approximation on the noise level.

External Extrinsic Skew Constraint- Our limit on tolerancing in the external group due to load-capacitance variation and manufacturing tolerances on the net is:

$$1077 - 500 - 85 = 492\text{psec}$$

In the following table, we have computed the allowable variation on C_L . The analysis allocates 20 psec/in for manufacturing tolerances on each external net, computes an extrinsic skew constraint from that, and then a constraint on C_L .

Load	C_{TYP} (pF)	Length (in)	Mfg Tol @ 20 psec/in (psec)	Extrinsic Skew Limit (psec)	ΔC_L^2 (pF)
1	10	8.693	174	318	± 5.6
2	2	10.363	207	285	± 4.2
3	5	9.698	194	298	± 4.7
4	5	9.698	194	298	± 4.7
5	2	10.363	207	285	± 4.2

1. 492psec - MT

2. Computed from expression (6) by setting ΔLT_{PD} equal to the extrinsic skew limit, and forcing symmetric variation of the C_L value around the typical value. That is, letting

$$C_{Lmax} = C_{TYP} + C_L/2 \quad \text{and,}$$

$$C_{Lmin} = C_{TYP} - C_L/2$$

The values from the right-most column are a constraint that we place on the clock inputs of the devices that receive the external clocks. In most cases, it is clear we have more than adequate margin on the low side.

System Noise Constraint - From Figure 5, we know that noise in the power environment and clock-signal transition-times interact directly with jitter. Budgeting jitter in a clock-distribution and reception network is complicated and a detailed treatment of that is beyond the scope of this note. In our example, we have a single device performing clock-distribution, and can assume all jitter is added at that point. An approximation of the maximum noise-voltage that the SC3508Q-1 can see at its power pins can be derived from:

$$\text{Max Jitter} \approx \text{Slew}_{max} * V_{noise(p-p)} \quad (11)$$

where,

Slew_{max} is the slowest (largest) slew rate in nsec/volt.

$V_{noise(p-p)}$ is the peak to peak noise voltage.

This was "derived" by examination of Figure 5. Assuming the signal into the SC3508-1 climbs 4V in 5 nsec (typical for many crystal oscillators),

$$0.085 \text{ nsec} = (5\text{nsec}/4V) * V_{noise(p-p)}$$

$$V_{noise(p-p)} = 68\text{mV}$$

This is an aggressive but achievable noise-voltage level at the pin of the SC3508Q-1. To achieve this, noise reduction methods must be used, such as including suitable bypass capacitors. A detailed discussion of noise-voltage reduction is beyond the scope of this note. Notice, however, that employing a crystal oscillator with faster edges increases the allowable noise voltage.

Configuring the SC3508Q-1

The data sheet provides detailed information on configuring the various inputs of the SC3508Q-1. The CLOCK SEL pin must be tied either low for a TTL source or high for an ECL source. Since the clock must toggle during power up (c.f. Section 2.2), the RESET input of the SC3508Q-1 can be tied high (inactive). Finally, source series termination is provided within the SC3508Q-1 to match the output drivers to lines with characteristic impedances in the range of 50 to 75 ohms. The patented output drivers also prevent undershoot and thereby reduce noise at the receiving chip input. The result is that the SC3508 provides 20 outputs with excellent signal integrity.

A Word About Serpentine Delays

Through out this design example we have assumed that the clock net lengths are matched. A typical method of accomplishing this to serpentine clock nets which need additional length.

The reader is cautioned that serpentine can have an effect on the propagation rate of a net. In Reference 2, this effect is described and illustrated with measurement.

4. EXTENSIONS TO THE DESIGN EXAMPLE

Our example was for a "typical" Pentium system. There are two significant extensions that can be made to this example:

1. Divided synchronous systems
2. Larger systems

4.1. Divided Synchronous Systems

In a divided synchronous system, the CPU module (12 loads) runs at 66-MHz and all of the circuitry external to the CPU module runs at 33-MHz. The memory bus controller will need one or two copies of both clocks to coordinate communication between the two timing environments. If our example design were converted to a divided synchronous system, we would need to select a clock buffer capable of providing an appropriate number of copies both clock frequencies. The AMCC SC3500Q-1 can fill this role. The SC3500's outputs are arranged in three groups (10, 5, & 5 pins), each of which can be operated at various relationships to the input as follows:

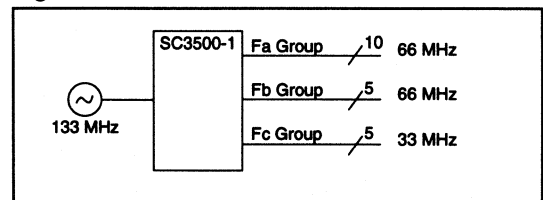
Output Group	Relationship to Output
Fa	10 outputs at $F_{input}/2$ (max = 80 MHz)
Fb	5 outputs at $F_{input}/2$ or $F_{input}/4$
Fc	5 outputs at $F_{input}/4$ or $F_{input}/8$

Therefore, we can convert our example to a divided synchronous system using an SC3500 as follows:

1. Drive the buffer with a 133MHz source.
2. Configure Fa and Fb groups for 66MHz (15 clock signals)
11 loads in CPU module (as previous)
4 clock signals available for MBC
3. Configure Fc group for 33-MHz (5 clock signals)

Figure 13 shows this configuration. The analysis of tolerancing for this new arrangement would be similar to what was shown in our original example.

Figure 13.



4.2. Larger Systems

When the number of loads in a system exceeds the number of pins on the clock buffer employed, it is necessary to move to a tree-structured clock-distribution network to fan out the signals. When this is the case, the tradeoffs and the analysis are more complicated. The most notable effect is that part-to-part buffer tolerances come into play. In even larger systems, cascaded part-to-part tolerances come into play. A complete discussion of these issues goes beyond the scope of this note. References 1 and 2 cover this subject in more depth. We will, however, provide some guidelines:

1. Exploit locality (i.e. the commonality of clock paths) in signal groups where tolerancing requirements are tight. For example, drive all of the loads in the CPU module from a single SC3508Q-1 to keep the part-to-part tolerances out of tolerances expressions.
2. Align the mean delays of all clock paths.

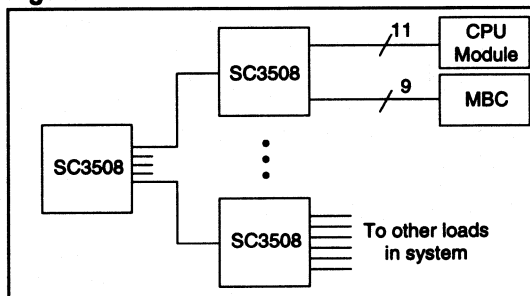
Figure 14 shows a mid-sized Pentium clock distribution network. It takes advantage of the reduced tolerancing among the outputs of the Fa group (250 psec).

5. SUMMARY

This note has presented a detailed example of clock-distribution in a typical Pentium design using AMCC's SC3508Q-1 clock driver. This example discussed the most important design decisions, and extended the example to other common design cases. As we saw, many of the timing-environment design methods previously necessary only in larger and faster computers are now necessary in Pentium systems.

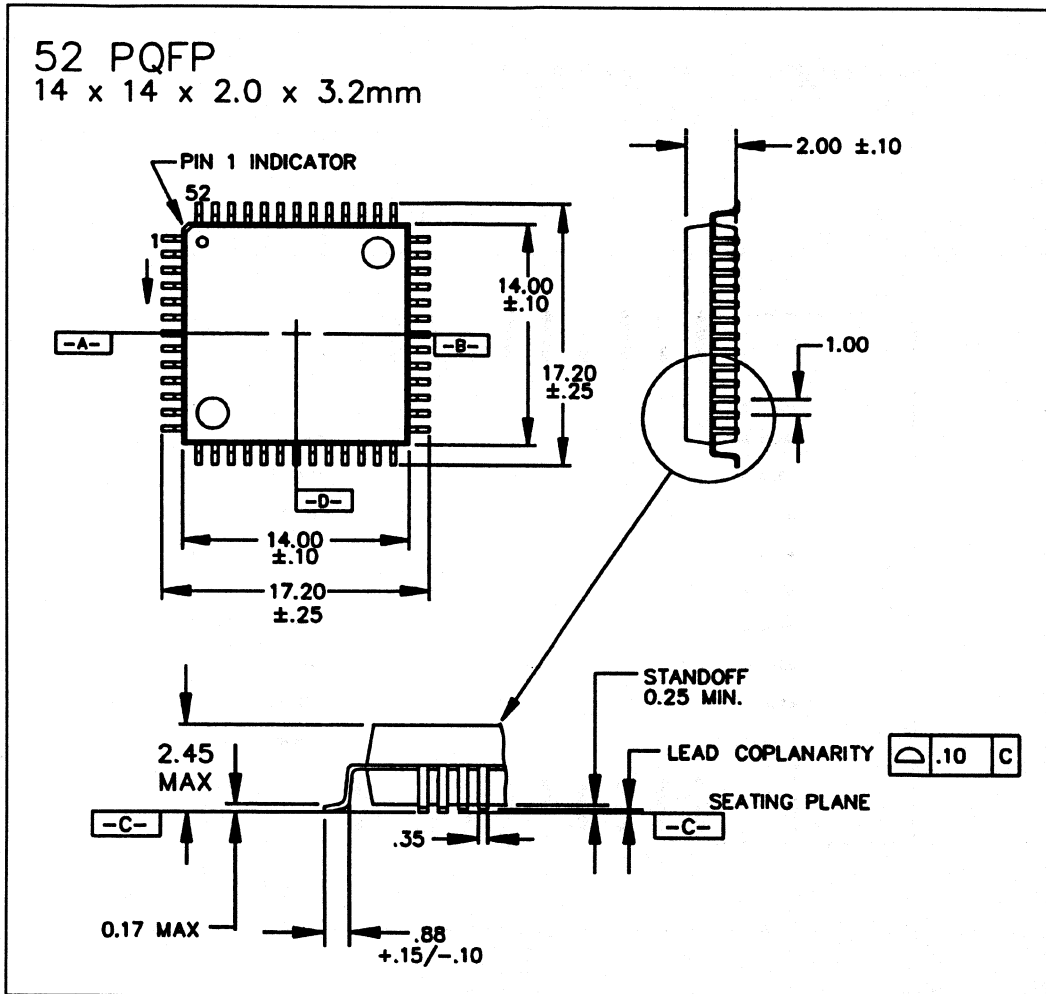
Even with these constraints, this application note shows that the SC3508Q-1 can be used in Pentium systems to create a statistically stable design. With twenty outputs, a low-skew design, and its no-undershoot drivers, the SC3508Q-1 allows the engineer to design a clock distribution scheme that will satisfy the rigorous requirements of the Pentium chips.

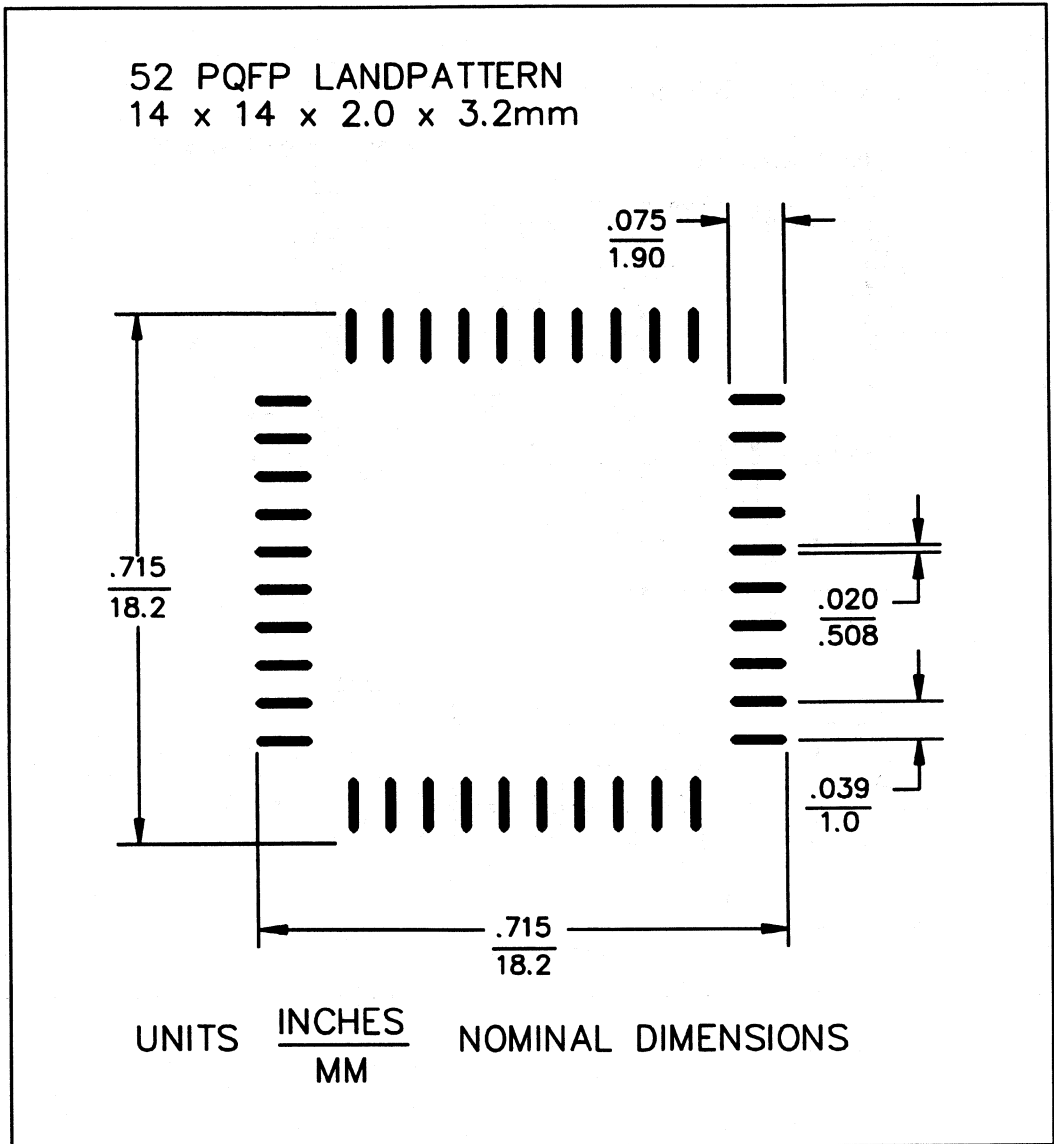
Figure 14.

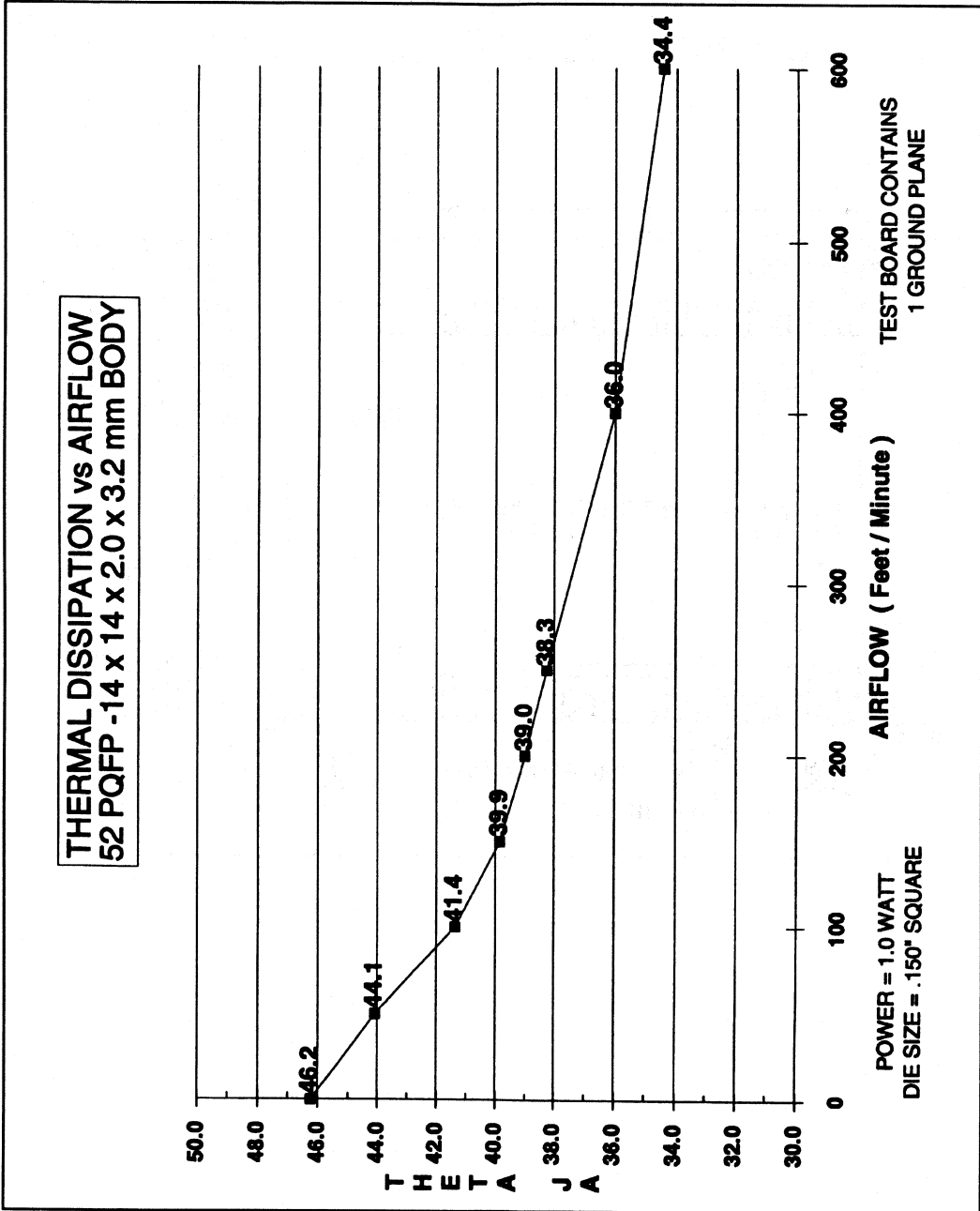


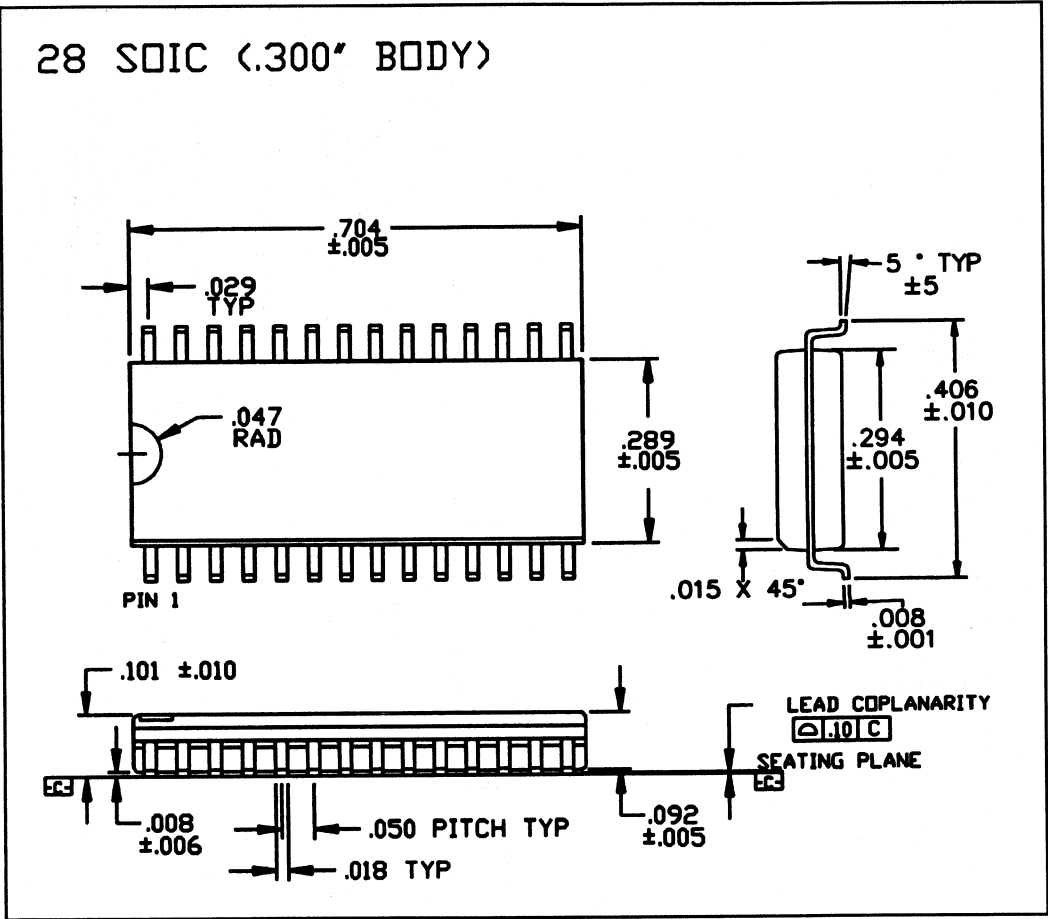
6. REFERENCES

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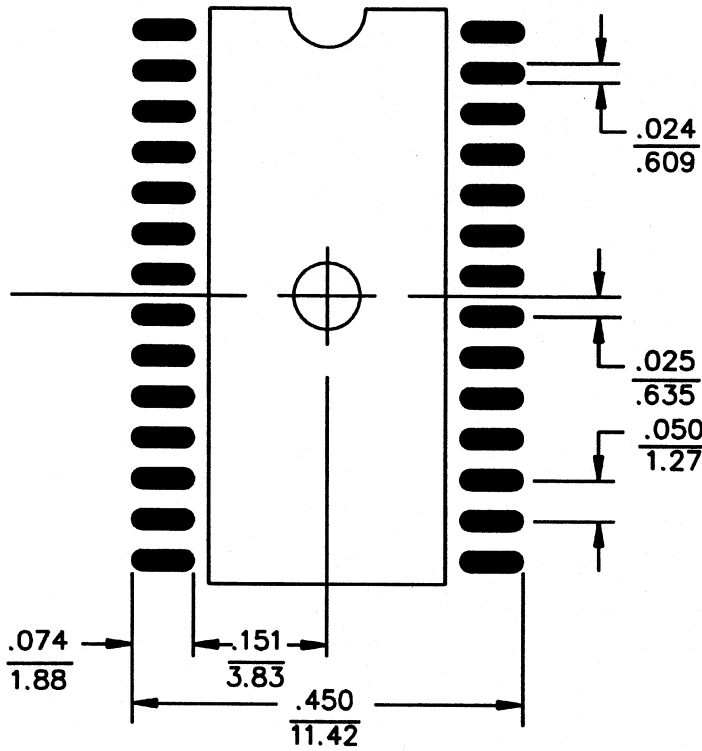




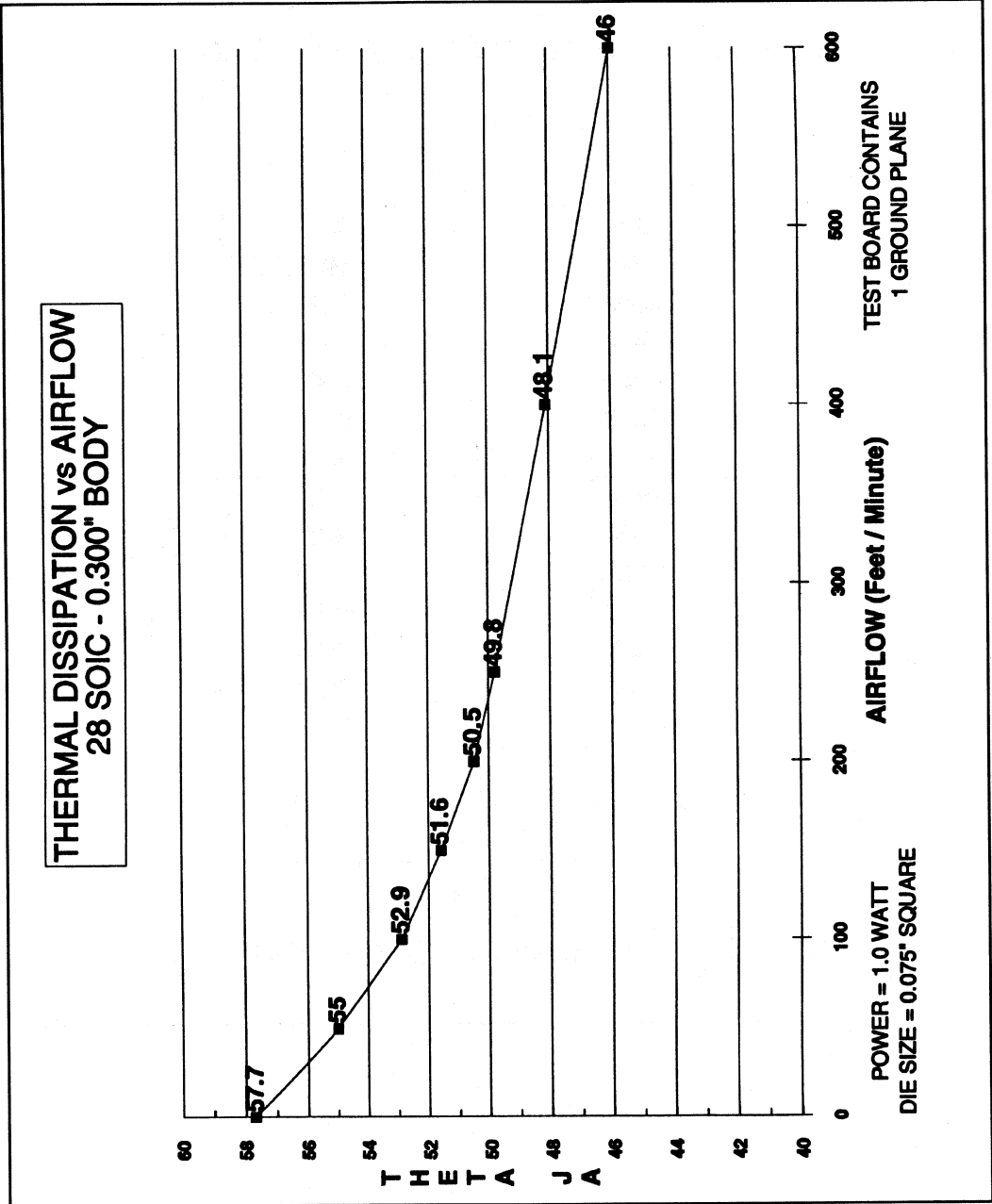




28 SOIC (.300" BODY) LANDPATTERN



UNITS $\frac{\text{INCHES}}{\text{MM}}$ NOMINAL DIMENSIONS



FEATURES

- Generates six clock outputs from 20 MHz to 80 MHz (the S4403 generates ten outputs and HFOUT generates 10MHz to 40MHz)
- 21 selectable phase/frequency relationships for the clock outputs
- Compensates for clock skew by allowing output delay adjustment down to 3.125 ns increments
- TTL outputs have less than 400 ps maximum skew
- Lock Detect output indicates loop status
- Internal PLL with VCO operating at 160 to 320 MHz
- Test Enable input allows VCO bypass for open-loop operation in board test
- Maximum 1.0 ns of phase error (750 ps from part to part)
- Proven 1.0 micron BiCMOS technology
- Single +5V power supply operation
- 28/44 PLCC packages

APPLICATIONS

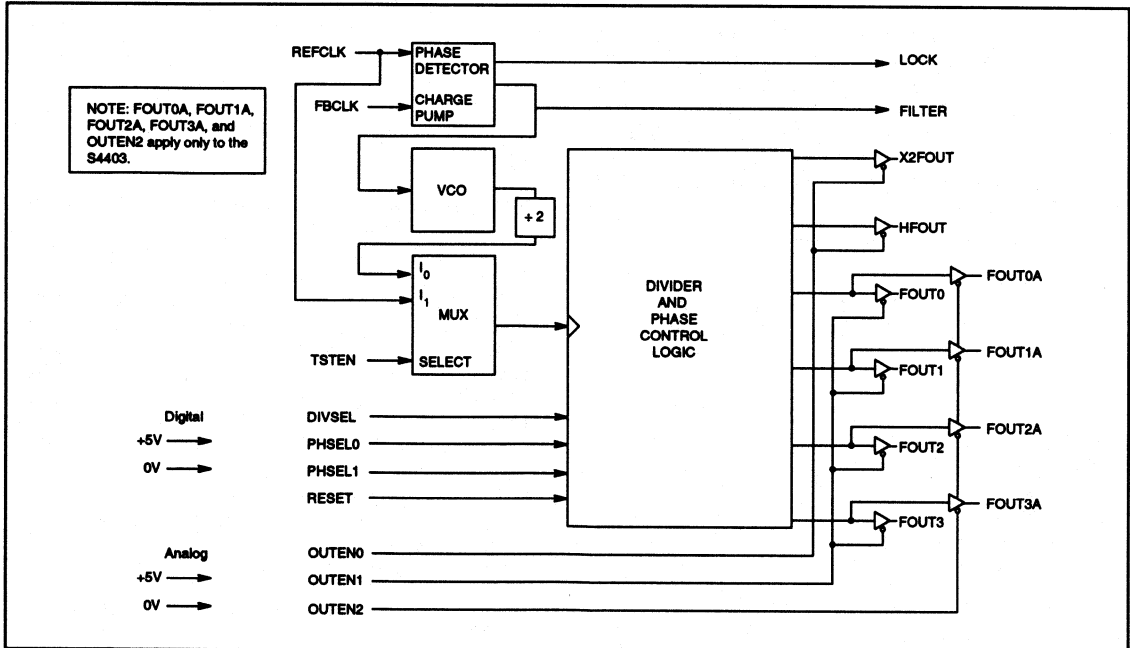
- CMOS ASIC Systems
- High-speed Microprocessor Systems
- Backplane Clock Deskew and Distribution

GENERAL DESCRIPTION

The S4402/S4403 BiCMOS clock generators allow the user to generate multiphase TTL clocks in the 10–80 MHz range with less than 400 ps of skew. Use of a single off-chip filter allows an entire 160–320 MHz phase-locked loop (PLL) to be implemented on-chip. Divide-by-two and times-two outputs allow the ability to generate output clocks at half, equal to, or twice the reference clock input frequency. By using the programmable divider and phase selector, the user can select from up to 21 different output relationships. The outputs can be phase-adjusted in increments as small as 3.125 ns to tailor the clocks to exact system requirements.

Implemented in AMCC's proven 1.0 micron BiCMOS technology, the S4402 generates six TTL outputs, while the S4403 provides those six plus four duplicates (FOUT0A–FOUT3A) for a total of ten. Output enables are provided for the various banks, allowing clock control for board and system tests.

Figure 1. Clock Generator Block Diagram



FUNCTIONAL DESCRIPTION

Frequency and Phase Controls

The S4402/S4403 clock generators provide multiple outputs that are synchronized in both frequency and phase to a periodic clock input. Two select pins and an external feedback path allow the user to phase-adjust the six outputs (FOUT0–FOUT3, HFOUT, and X2FOUT) relative to the input clock REFCLK, as well as control their frequency.

The DIVSEL input controls the programmable divider that follows the voltage controlled oscillator (VCO). This doubles the lock range of the PLL by allowing the user to select a VCO frequency divided by four (DIVSEL Low) or by eight (DIVSEL High).

The frequency of the four FOUT0–FOUT3 outputs (and the duplicate set of the four FOUT0A–FOUT3A outputs on the S4403) is determined by the REFCLK clock frequency and the output that is tied back to the FBCLK input. In addition, the X2FOUT TTL output provides a clock signal identical to the FOUT0 output in the divide-by-four mode, and twice the FOUT0 frequency (maximum frequency of 80 MHz) in the divide-by-eight mode. The HFOUT TTL output provides a clock signal that is in phase with the FOUT0 output, but at half the FOUT0 frequency in both the divide-by-four and divide-by-eight modes. Refer to the Output Select Matrix in Table 3 for the specific relationships.

Phase adjustments can be made in increments as small as 3.125 ns. The minimum phase delay between FOUT0–FOUT3 signals is a function of the VCO frequency. The VCO frequency can be determined by multiplying the output frequency by the divide-by ratio of four or eight, controlled by DIVSEL. The minimum phase delay t is equal to the period of the VCO frequency:

$$t = 1 / \text{VCO freq}$$

Since the VCO can operate in the 160 MHz to 320 MHz range, minimum phase delay values can range from 6.25 ns to 3.125 ns. Table 1 shows various FOUT/VCO frequencies and the associated phase resolution.

The PHSEL1 and PHSEL0 inputs allow the user to select several phase relationships among the four FOUT0–FOUT3 TTL clock outputs. These choices can be seen in Table 2, and the Output Select Matrix provided in Table 3 describes the 21 output configurations available to the user. The two “Select Pins” columns specify the signal levels on the pins PHSEL0 and PHSEL1. These are active High signals. The column entitled “Output Fed to FBCLK” indicates which output (FOUT0–FOUT3,

HFOUT, or X2FOUT) is externally connected to the feedback input (FBCLK) to produce the resulting waveforms shown in the appropriate row in the table. The last seven columns specify the resulting phase and frequency relationships of each output to the user clock input (REFCLK). A negative value indicates the time by which the output rising edge precedes the input (REFCLK) rising edge. A positive value is the time by which the rising edge of the output follows the rising edge of the input clock.

Table 1. Example Phase Resolution

FOUT0–3 Freq	Divider Select	VCO Freq	Min Phase Resolution
80 MHz	4	320 MHz	3.125 ns
66 MHz	4	266 MHz	3.75 ns
50 MHz	4	200 MHz	5.0 ns
40 MHz	4	160 MHz	6.25 ns
40 MHz	8	320 MHz	3.125 ns
33 MHz	8	266 MHz	3.75 ns
25 MHz	8	200 MHz	5.0 ns
20 MHz	8	160 MHz	6.25 ns

Table 2. Phase Selections

PHSEL1	PHSEL0	Phase Relationship
0	0	All at same phase
0	1	FOUT0–FOUT3 outputs skewed by 90 degrees from each other
1	0	FOUT1 leads FOUT0 by minimum phase, FOUT2 lags FOUT0 by minimum phase, and FOUT3 lags FOUT0 by 90 degrees
1	1	FOUT1 lags FOUT0 by minimum phase, FOUT2 lags FOUT1 by minimum phase, and FOUT3 lags FOUT2 by minimum phase

Example:

In a typical system, designers may need several low-skew outputs, one early clock, one late clock, a clock at half the input clock frequency, and one at twice the input clock frequency. This system requirement can be met by setting PHSEL1 to 1, PHSEL0 to 0, and feeding back FOUT0 to the FBCLK input (Row 10 of Table 3). The result is that FOUT0 will be phase-aligned to REFCLK, FOUT1 will lead REFCLK by a minimum phase delay, FOUT2 will lag REFCLK by a minimum phase delay, FOUT3 will phase-lag REFCLK by 90°, HFOUT will be phase-aligned with REFCLK but at half the frequency, and X2FOUT will be either phase-aligned at the same frequency as the reference clock if DIVSEL = 0, or at twice the frequency if DIVSEL = 1.

Several other waveform examples and typical applications are provided on pages 5-194 and 5-195.

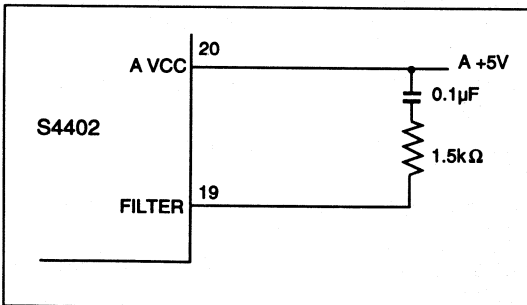
Enabling Outputs

The S4402 has two output-enable inputs that control which outputs toggle. (The S4403 has three output-enable inputs.) When held LOW, OUTEN0 controls the frequency doubler output X2FOUT and the half-frequency output HFOUT. OUTEN1 controls the FOUT0–FOUT3 outputs. The third input on the S4403, OUTEN2, controls the duplicate set of four outputs FOUT0A–FOUT3A. When an output enable pin is held High, its associated outputs are disabled and held in a High state.

Filter

The FILTER output is a tap between the analog output of the phase detector and the VCO input. This pin allows a simple external filter (Figure 2) to be included in the PLL. AMCC recommends the use of the filter component values shown. This filter was chosen for its ability to reduce the output jitter and filter out noise on the REFCLK input. The filter components should be in surface mounted packages with minimum lead inductance.

Figure 2. External PLL Filter



Reset

When the RESET pin is pulled low, all the internal states go to zero one clock cycle (from the VCO or REFCLK in the test mode) before the outputs go low. After the chip is reset, the PLL requires a resynchronization time of $\leq 5\text{ms}$ before lock is again achieved.

Lock Detect

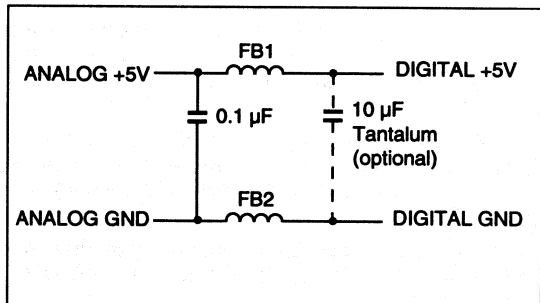
A lock detect function is provided by the LOCK output. When REFCLK and FBCLK are within 2–4 ns of each other, the PLL is in lock, and the LOCK output goes High.

Power Supply Considerations

Power for the analog portion of the S4402/S4403 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 3). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100 μH , and depends upon the frequency spectrum of the digital power supply noise. The ferrite beads should exhibit 75 Ω impedance at 10 MHz.

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

Figure 3. External Power Supply Filter



Test Capabilities

The TSTEN input puts the S4402/S4403 into a test mode and allows users to bypass the VCO and provide their own clock through the REFCLK input. When TSTEN is High, the VCO is turned off and the REFCLK signal drives the divider/phase adjust circuitry, directly sequencing the outputs. The TSTEN and REFCLK inputs join the divider circuitry after the initial divide-by-two stage. Therefore, REFCLK is divided by two in the divide-by-four mode and divided by four in the divide-by-eight mode.

PIN DESCRIPTIONS

Input Signals

REFCLK. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the FOUT0–FOUT3 outputs. Also replaces the VCO output when TSTEN is high (after first divide-by-two stage in divider phase control logic). See TSTEN.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the FOUT0–FOUT3 outputs. One output is selected to feed back to this input. (See Table 3.)

DIVSEL. Controls the divider circuit that follows the VCO. When DIVSEL is low, the VCO frequency is divided by four. When DIVSEL is high, the VCO frequency is divided by eight. (See Tables 1 and 3.)

PHSEL0. This input, along with PHSEL1, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

PHSEL1. Along with PHSEL0, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

OUTEN0. Active Low. Output enable signal that controls which outputs toggle. Controls the frequency doubler output (X2FOUT) and the half-frequency output (HFOUT).

OUTEN1. Active Low. Output enable signal that controls which outputs toggle. Controls the FOUT0–FOUT3 outputs.

OUTEN2. (S4403 only.) Active Low. Controls the duplicate set of outputs to FOUT0–FOUT3 (FOUT0A, FOUT1A, FOUT2A, AND FOUT3A).

RESET. Active Low. Initializes internal states for test purposes.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Therefore, REFCLK is divided by two in the divide-by-four mode, and divided by four in the divide-by-eight mode, and used to directly sequence the outputs.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and one capacitor) to be included in the PLL.

X2FOUT. Provides a clock signal identical to the FOUT0 output in the divide-by-four mode and twice the FOUT0 frequency (maximum of 80 MHz) in the divide-by-eight mode.

FOUT0. Clock output.

FOUT1. Clock output.

FOUT2. Clock output.

FOUT3. Clock output.

HFOUT. Provides a clock signal in phase with the FOUT0 output, but at half the FOUT0 frequency in both the divide-by-four and divide-by-eight modes.

LOCK. Goes high when REFCLK and FBCLK are within 2–4 ns of each other, demonstrating that the PLL is in lock.

FOUT0A. (S4403 only.) Clock output—duplicates FOUT0.

FOUT1A. (S4403 only.) Clock output—duplicates FOUT1.

FOUT2A. (S4403 only.) Clock output—duplicates FOUT2.

FOUT3A. (S4403 only.) Clock output—duplicates FOUT3.

Table 3. Output Select Matrix

Configuration Number	Select Pins		Output Fed to FBCLK	Output Phase Relationships					+4	+8
	PHSEL1	PHSEL0		FOUT0	FOUT1	FOUT2	FOUT3	HFOUT		
1	0	0	FOUT0-FOUT3	0	0	0	0	0/2	0	2(0)
2	0	0	HFOUT	2(0)	2(0)	2(0)	2(0)	0	2(0)	4(0)
3	0	0	X2FOUT (+8)	0/2	0/2	0/2	0/2	0/4		0
4	0	1	FOUT0	0	Q	2Q	3Q	0/2	0	2(0)
5	0	1	FOUT1	-Q	0	Q	2Q	-Q/2	-Q	2(-Q)
6	0	1	FOUT2	-2Q	-Q	0	Q	-2Q/2	-2Q	2(-2Q)
7	0	1	FOUT3	-3Q	-2Q	-Q	0	-3Q/2	-3Q	2(-3Q)
8	0	1	HFOUT	2(0)	2(Q)	2(2Q)	2(3Q)	0	2(0)	4(0)
9	0	1	X2FOUT (+8)	0/2	Q/2	2Q/2	3Q/2	0/4		0
10	1	0	FOUT0	0	-t	t	Q	0/2	0	2(0)
11	1	0	FOUT1	t	0	2t	Q+t	1/2	t	2(t)
12	1	0	FOUT2	-t	-2t	0	Q-t	-1/2	-t	2(-t)
13	1	0	FOUT3	-Q	-Q-t	-Q+t	0	-Q/2	-Q	2(-Q)
14	1	0	HFOUT	2(0)	2(-t)	2(t)	2(Q)	0	2(0)	4(0)
15	1	0	X2FOUT (+8)	0/2	-1/2	1/2	Q/2	0/4		0
16	1	1	FOUT0	0	t	2t	3t	0/2	0	2(0)
17	1	1	FOUT1	-t	0	t	2t	-1/2	-t	2(-t)
18	1	1	FOUT2	-2t	-t	0	t	-21/2	-2t	2(-2t)
19	1	1	FOUT3	-3t	-2t	-t	0	-31/2	-3t	2(-3t)
20	1	1	HFOUT	2(0)	2(t)	2(2t)	2(3t)	0	2(0)	4(0)
21	1	1	X2FOUT (+8)	0/2	1/2	21/2	31/2	0/4		0

- Notes:
1. "0" implies the output is aligned with REFCLK.
 2. "t" implies the output lags REFCLK by a minimum phase delay.
 3. "Q" implies the output lags REFCLK by 90° of phase
 4. "-t" implies the output leads REFCLK by a minimum phase delay.
 5. "-Q" implies the output leads REFCLK by 90° of phase.
 6. "2()" implies the output is at twice the frequency of REFCLK.

Legend

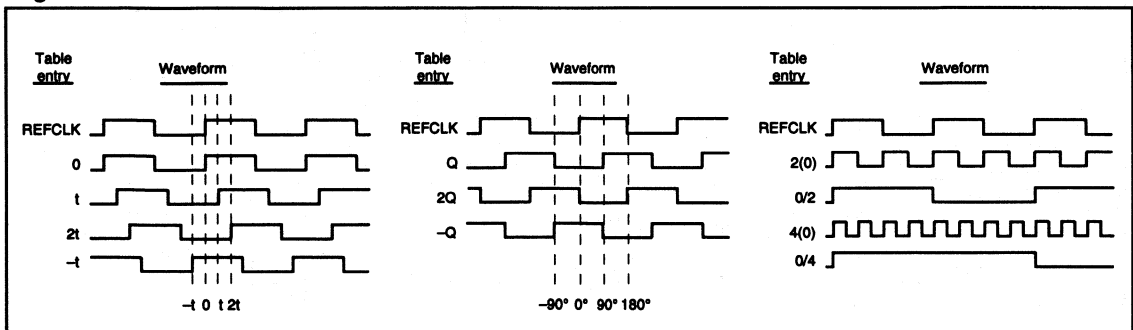
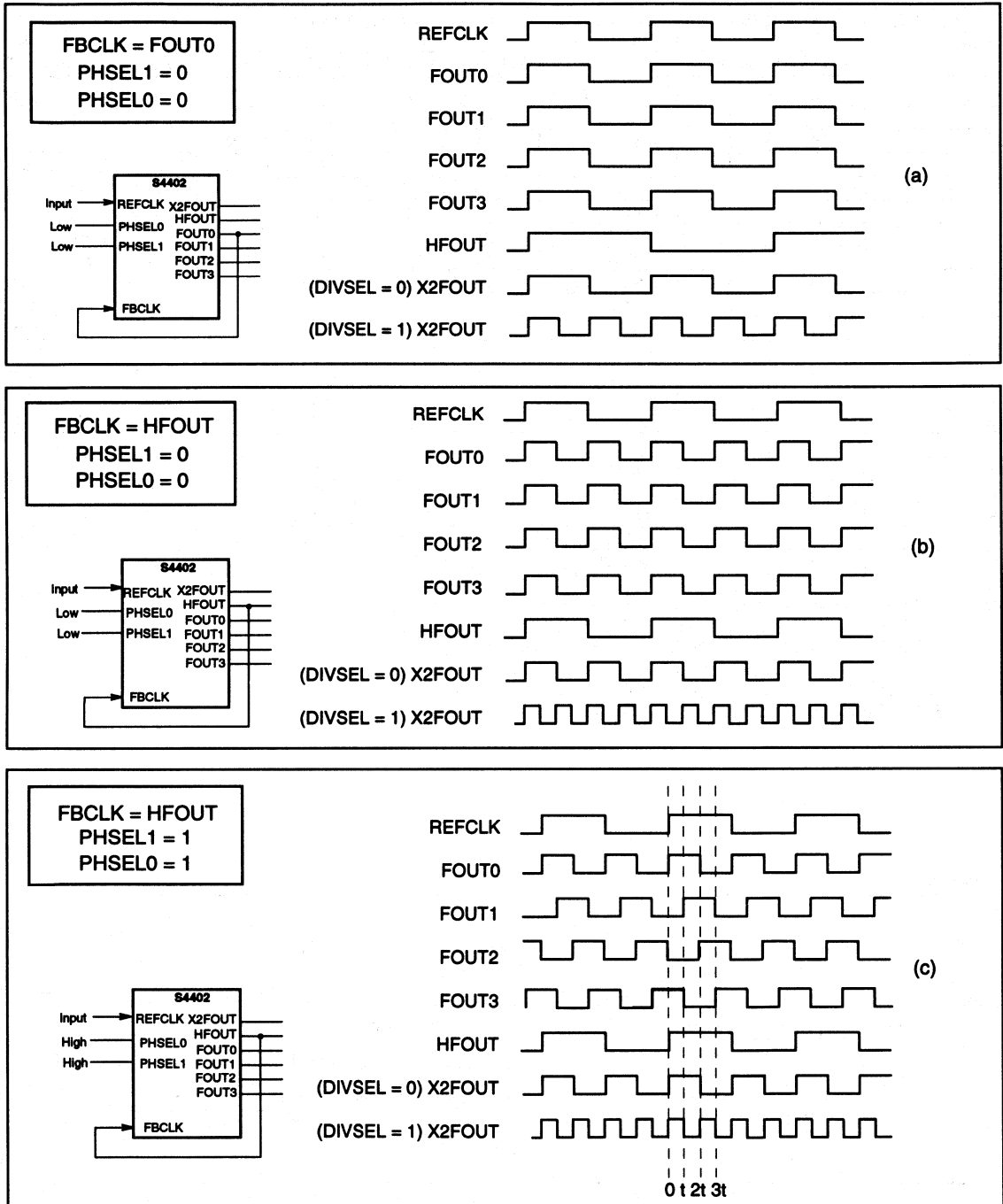


Figure 4. Configuration Examples

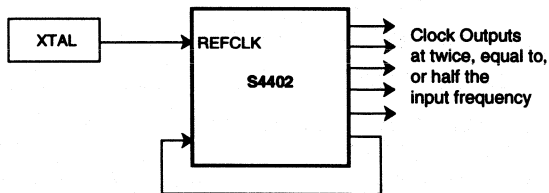


TYPICAL APPLICATIONS

The S4402/S4403 chips are designed to meet a large variety of system clocking requirements. Several typical applications are provided below.

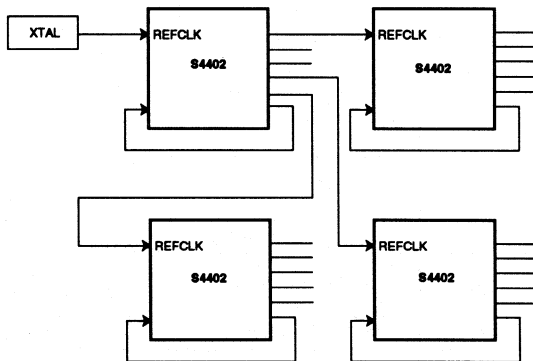
Application 1. High-Frequency, Low-Skew Clock Generation

One of the most basic capabilities of the S4402/S4403 devices is generating multiple phase-aligned low-skew clocks at various multiples of the input clock frequency. For example, in a multiple-board system a half-frequency clock can be generated for use across the backplane, where it is simpler to route a low-speed signal. This signal can then be doubled on the boards, and synchronization will be maintained.



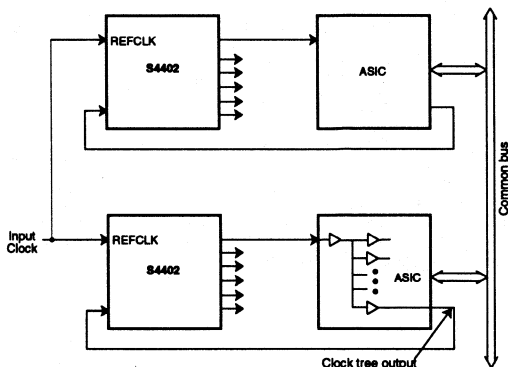
Application 2. Low-Skew Clock Distribution

One common problem in clocking high-speed systems is that of distributing several copies of a system clock while maintaining low skew throughout the system. The S4402/S4403 devices guarantee low skew among all the clocks in the system, as they have effectively zero delay between their input and output signals, with an output skew of less than 400 ps. The user can also adjust the phases of the outputs in increments as small as 3.125 ns, for load and trace length matching.



Application 3. Delay Compensation

Since the relative edges of the S4402/S4403 outputs can be precisely controlled, these chips can be used to compensate for different delays due to trace lengths or to internal chip delays, simplifying board layout and bus timing. In the example shown, the two ASICs have a difference of several nanoseconds in their propagation delays. The S4402s ensure that the output signals are aligned, so that the data valid uncertainty on the common bus is minimized.



ABSOLUTE MAXIMUM RATINGS

Commercial

TTL Supply Voltage VCC (VEE = 0)	7.0 V
TTL Input Voltage (VEE = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Commercial			Units
	Min	Nom	Max	
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

DC CHARACTERISTICS

Symbol	Parameter	DC Test Conditions	Min	Typ ¹	Max	Units
V _{IH} ²	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			V
V _{IL} ²	Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8	V
V _{IK}	Input clamp diode voltage	V _{CC} = Min, I _{IN} = -18mA		-0.8	-1.2	V
V _{OH}	Output HIGH voltage	V _{CC} = Min	I _{OH} = -12mA ³ (COM)	2.4		V
			I _{OH} = -24mA ³ (COM)	2.0		V
V _{OL}	Output LOW voltage	V _{CC} = Min, I _{OL} = 24mA ³ (COM)			0.5	V
I _{IH}	Input HIGH current	V _{CC} = Min, V _{IN} = 2.4V	OUTEN2		-200	μA
			Other		50	μA
I _I	Input HIGH current at max	V _{CC} = Max, V _{IN} = V _{CC}			1.0	mA
I _{IL}	Input LOW current	V _{CC} = Min, V _{IN} = 0.5V	OUTEN2		-500	μA
			Other		-50	μA
I _{OS} ⁴	Output short circuit current	V _{CC} = Max, V _{OUT} = 0V	-25		-100	mA
I _{CC}	Static	V _{CC} = Max			70	mA
I _{CC}	Total I _{CC} (Dynamic and Static)	V _{LOAD} = 25pF at 50 MHz			190	mA

1. Typical limits are at 25°C, V_{CC} = 5.0V.

2. These input levels should only be tested in a static, noise-free environment.

3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher and are optimized to balance rise and fall times.

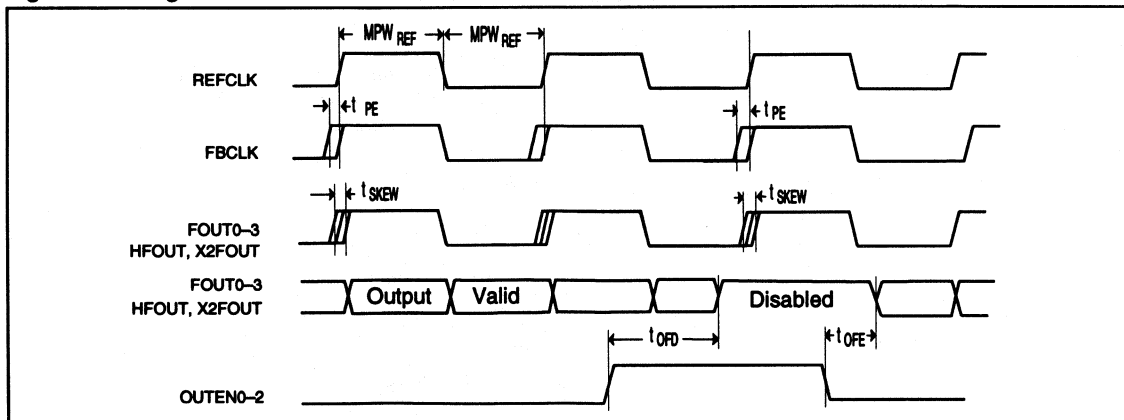
4. Maximum test duration is one second.

Table 4. AC Specifications

Symbol	Description	S4402/3-66		S4402/3-80		Units
		Min	Max	Min	Max	
f_{VCO}	VCO Frequency	160	266	160	320	MHz
f_{REF}	REFCLK Frequency	10	66	10	80	MHz
MPW_{REF}	REFCLK Minimum Pulse Width	7.0		6.0		ns
t_{PE}	Phase Error between REFCLK and FBCLK	-1.0	0	-1.0	0	ns
t_{PED}	Phase Error Difference from Part to Part ¹	0	750	0	750	ps
t_{SKEW}	Output Skew ²	0	400	0	400	ps
t_{DC}	Output Duty Cycle ³	45	55	45	55	%
f_{FOUT}	FOUT Frequency ⁴	20	66	20	80	MHz
f_{HFOUT}	HFOUT Frequency ⁴	10	33	10	40	MHz
f_{2XFOUT}	2XFOUT Frequency ⁴	40	66	40	80	MHz
t_{PS}	Nominal Phase Shift Increment	3.75	6.25	3.125	6.25	ns
t_{PSJ}	Phase Shift Variation ⁵	-250	+250	-250	+250	ps
t_{OFD}	Tpd OUTEN0-2 to FOUTs, Disable	2	7	2	7	ns
t_{OFE}	Tpd OUTEN0-2 to FOUTs, Enable	2	7	2	7	ns
t_{RF}	Input Rise/Fall Time	1	3	1	3	ns
t_{ORF}	FOUT Rise/Fall Time ⁶	0.5	1.5	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time ⁷		5		5	ms
t_j	Clock Stability ⁸		500		500	ps

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. Outputs loaded with 35pF, measured at 1.5V.
4. $C_{LOAD} = 35\text{ pF}$.
5. All phase shift increments and variation are measured relative to FOUT0 at 1.5V.
6. With 35 pF output loading (0.8 V to 2.0 V transition).
7. Depends on loop filter chosen. (Number given is for example filter.)
8. Clock period jitter with all FOUT outputs operating at 66 MHz and loaded with 25pF using loop filter shown. Parameter guaranteed, but not tested.

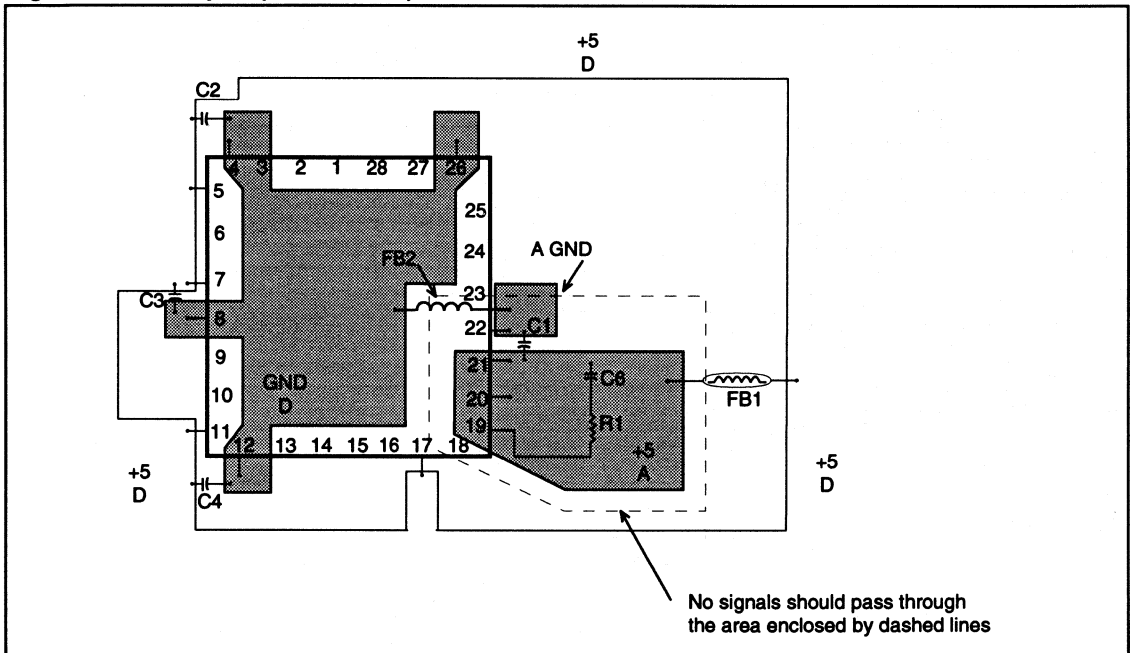
Figure 5. Timing Waveforms



BOARD LAYOUT CONSIDERATIONS

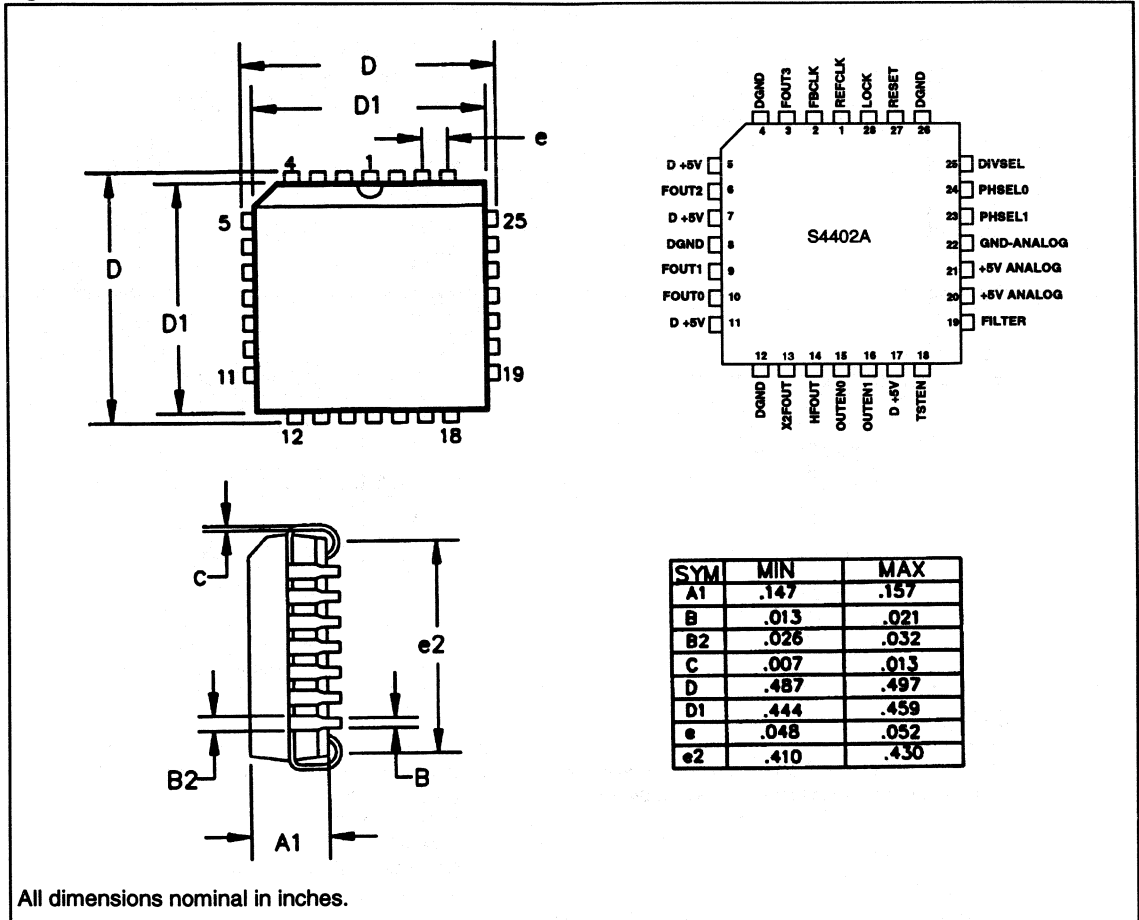
- The S4402/S4403 chips are sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.
- All decoupling capacitors (C1–C4 = 0.1 μ F) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4402/S4403 and the power and ground plane connections.
- No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 6) to avoid the possibility of noise due to crosstalk.
- The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.
- The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

Figure 6. Board Layout (S4402 shown)



Component	Description
C1–C4	0.1 μ F ceramic capacitor
C6	0.1 μ F ceramic capacitor
R1	1.5 K 10% resistor
FB1,FB2	Ferrite bead or inductor

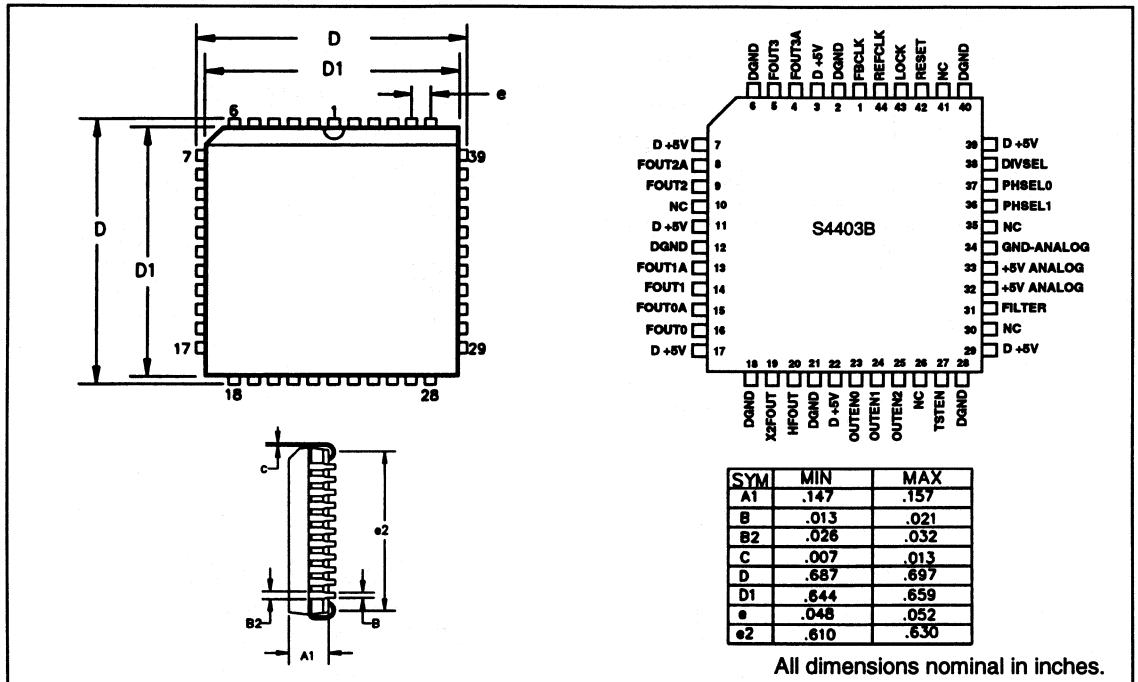
Figure 7. S4402 28 PLCC Package and Pinout



28 PLCC Thermal Resistance

Still Air	100 Linear Ft./Min	200 Linear Ft./Min
60°C/Watt	50°C/Watt	45°C/Watt

Figure 8. S4403 44 PLCC Package and Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- Device Number
- Package Type
- Speed Option
- Optional Shipping Configuration

S4402/03

A

- 66

/TD

Optional Shipping Configuration

Blank = tube

/D = dry pack

/TD = tape, reel and dry pack

Speed Option

- 66 = 66 MHz

- 80 = 80 MHz

Package Option

A = 28-pin PLCC (S4402)

B = 44-pin PLCC (S4403)

Device Number

S4402

S4403

Example: S4402A-66/D

28-pin PLCC package, shipped dry packed in the standard tube.

FEATURES

- Generates six clock outputs from 20 MHz to 80 MHz (HFOUT operates from 10 MHz to 40 MHz)
- Allows PECL or TTL reference input
- Provides differential PECL output at up to 160 MHz
- 21 selectable phase/frequency relationships for the clock outputs
- Compensates for clock skew by allowing output delay adjustment down to 3.125 ns increments
- TTL outputs have less than 400 ps maximum skew
- Lock Detect output indicates loop status
- Internal PLL with VCO operating at 160 to 320 MHz
- Test Enable input allows VCO bypass for open-loop operation
- Maximum 1.0 ns of phase error (750 ps from part to part)
- Proven 1.0 micron BiCMOS technology
- Single +5V power supply operation
- 44 PLCC package

APPLICATIONS

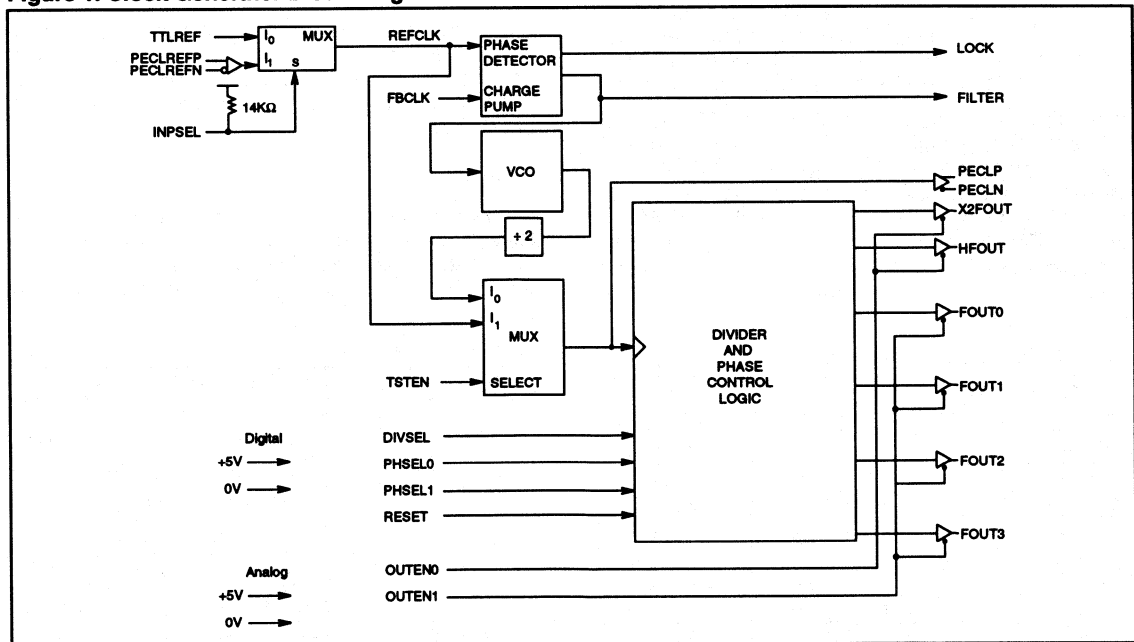
- CMOS ASIC Systems
- High-speed Microprocessor Systems
- Backplane Clock Deskew and Distribution

GENERAL DESCRIPTION

The S4405 BiCMOS clock generators allow the user to generate multiphase TTL clocks in the 10–80 MHz range with less than 400 ps of skew. Use of a simple off-chip filter allows an entire 160–320 MHz phase-locked loop (PLL) to be implemented on-chip. Divide-by-two and times-two outputs allow the ability to generate output clocks at half, equal to, or twice the reference clock input frequency. The reference is selectable to be either TTL or PECL. By using the programmable divider and phase selector, the user can select from up to 21 different output relationships. The outputs can be phase-adjusted in increments as small as 3.125 ns to tailor the clocks to exact system requirements.

Implemented in AMCC's proven 1.0 micron BiCMOS technology, the S4405 generates six TTL outputs and one differential PECL output. Output enables are provided for the various TTL banks, allowing clock control for board and system tests.

Figure 1. Clock Generator Block Diagram



FUNCTIONAL DESCRIPTION

This BiCMOS clock generator is designed to allow the user to generate TTL clocks, in the 10–80 MHz range, with less than 400 ps of skew. Implemented in AMCC's 1.0μ BiCMOS technology, the internal VCO, phase detector, and programmable divider and phase selector allow the user to tailor the TTL output clocks for his/her system needs. The internal VCO can operate between 160 to 320 MHz, and the programmability allows the user to generate TTL output clocks in the 10–80 MHz range, and a differential +5V referenced ECL output at 80–160 MHz.

The clock generator offers the user the ability to select the appropriate phase relationship among the four FOUT0–3 TTL clock outputs. The phase selection choices are shown in Table 2.

The clock generator also allows the user to choose the divide-by ratio between the VCO frequency and the frequency of the FOUT0–3 signals. The VCO frequency can be divided by 4 when DIVSEL is low, and divided by 8 when DIVSEL is high. The divide ratio between the VCO and the pseudo ECL outputs, PECLP and PECLN, is a fixed divide-by-2.

The clock generator also has two output enable inputs which can be used to control which outputs toggle. OUTEN0 controls the HFOUT and X2FOUT outputs, and OUTEN1 controls the FOUT0–3 outputs. When the output enables are high, the outputs are disabled, and held in a high state.

REFCLK can be driven by either the TTLREF or PECLREF inputs. The reference clock source is selected with the INPSEL input. When INPSEL is low, the TTLREF input is selected as the reference clock.

The FOUT0–3 outputs are the main TTL output clocks that the generator supplies. The frequency of these outputs is determined by the REFCLK clock frequency and the output clock that is tied to the FBCLK input. FOUT0–3 will be equal to REFCLK, half of REFCLK, or twice the frequency of REFCLK. The X2FOUT TTL output provides a clock signal that is identical to the FOUT0 output in the divide-by-4

mode, but twice the FOUT0 frequency (max. freq. of 66 MHz) in the divide-by-8 mode. The HFOUT TTL output provides a clock signal that is also in phase with the FOUT0 output, but at half the FOUT0 frequency.

FILTER is the analog signal from the phase detector going into the VCO. This pin is provided so a simple external filter (a single resistor and one capacitor) can be included in the phase-locked loop of the clock generator.

The LOCK output goes high when the reference clock and FBCLK are within 2–4 ns of each other. This output tells the user that the PLL is in lock.

Three pins are included for test purposes. TESTEN allows the chip to use the REFCLK signal instead of the VCO output to clock the chip. This is used during chip test to allow the counters and control logic to be tested independently of the VCO. The RESET pin initializes the internal counter flip-flops to zeros, but several clock cycles are necessary before the outputs go to a zero state.

The minimum phase delay between FOUT0–3 signals is a function of the VCO frequency. The VCO frequency can be determined by multiplying the output frequency by the divide-by ratio of four or eight. The minimum phase delay is equal to the period of the VCO frequency: $M_p = 1/\text{VCO freq.}$ Since the VCO can operate in the 160 MHz to 320 MHz range, the range of minimum phase delay values is 6.25 ns to 3.125 ns. Table 1 shows various FOUT/VCO frequencies and the associated phase resolution.

The charge pump and VCO portion of the chip use a separate analog power supply. This supply is brought onto the chip through a distinct set of power and ground pins. This supply should be free of digital switching noise.

Example:

In a typical system, designers may need several low-skew outputs, one early clock, one late clock, a clock at half the input clock frequency, and one at twice the input clock frequency. This system requirement

Table 1. Example Phase Resolution

FOUT0–3 Freq	Divider Select	VCO Freq	Min Phase Resolution
80 MHz	4	320 MHz	3.125 ns
66 MHz	4	266 MHz	3.75 ns
50 MHz	4	200 MHz	5.0 ns
40 MHz	4	160 MHz	6.25 ns
40 MHz	8	320 MHz	3.125 ns
33 MHz	8	266 MHz	3.75 ns
25 MHz	8	200 MHz	5.0 ns
20 MHz	8	160 MHz	6.25 ns

Table 2. Phase Selections

PHSEL1	PHSEL0	Phase Relationship
0	0	All at same phase
0	1	Outputs skewed by 90 degrees from each other
1	0	FOUT1 leads FOUT0 by minimum phase, FOUT2 lags FOUT0 by minimum phase, and FOUT3 lags FOUT0 by 90 degrees
1	1	Outputs skewed by minimum phase (determined by the divider selection, and the VCO frequency) from each other.

Note: The PECL output is not affected by the phase select inputs.

can be met by setting PHSEL1 to 1, PHSEL0 to 0, and feeding back FOUT0 to the FBCLK input (Row 10 of Table 3). The result is that FOUT0 will be phase-aligned to the reference clock, FOUT1 will lead the reference clock by a minimum phase delay, FOUT2 will lag the reference clock by a minimum phase delay, FOUT3 will phase-lag the reference clock by 90°, HFOUT will be phase-aligned with the reference clock but at half the frequency, and X2FOUT will be either phase-aligned at the same frequency as the reference clock if DIVSEL = 0, or at twice the frequency if DIVSEL = 1.

Enabling Outputs

The S4405 has two output-enable inputs that control which outputs toggle. When held LOW, OUTEN0 controls the frequency doubler output X2FOUT and the half-frequency output HFOUT. OUTEN1 controls the FOUT0–3 outputs. When an output enable pin is held High, its associated outputs are disabled and held in a High state.

Filter

The FILTER output is a tap between the analog output of the phase detector and the VCO input. This pin allows a simple external filter (Figure 2) to be included in the PLL. AMCC recommends the use of the filter component values shown. This filter was chosen for its ability to reduce the output jitter and filter out noise on the reference clock input.

Reset

When the RESET pin is pulled low, all the internal states go to zero, but the outputs will not go low until one clock cycle later (VCO/2 or period of the reference clock). After the chip is reset, the PLL requires a resynchronization time before lock is again achieved.

Lock Detect

A lock detect function is provided by the LOCK output. When the selected reference clock and FBCLK

are within 2–4 ns of each other, the PLL is in lock, and the LOCK output goes High.

Power Supply Considerations

Power for the analog portion of the S4405 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 3). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise. The ferrite beads should exhibit 75Ω impedance at 10 MHz.

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

BOARD LAYOUT CONSIDERATIONS

- The S4405 is sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.
- All decoupling capacitors (C1–C4 = 0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4405 and the power and ground plane connections.
- No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 4) to avoid the possibility of noise due to crosstalk.

Figure 2. External PLL Filter

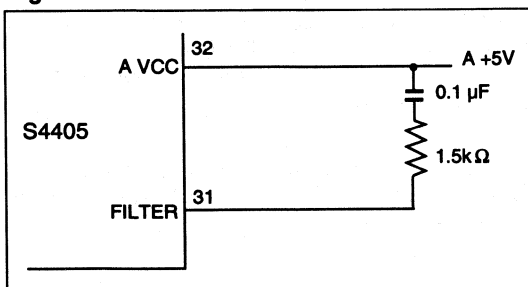
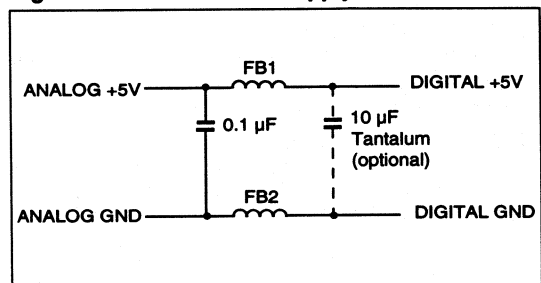
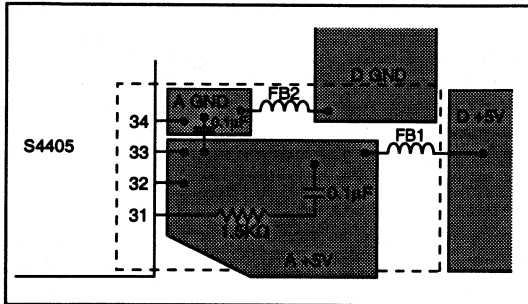


Figure 3. External Power Supply Filter



- The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.
- The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

Figure 4. Board Layout



Test Capabilities

The TSTEN input allows users to bypass the VCO and provide their own clock through the selected reference clock input. When TSTEN is High, the VCO is turned off and the REFCLK signal drives the divider/phase adjust circuitry, directly sequencing the outputs. The TSTEN and REFCLK inputs join the divider circuitry after the initial divide-by-two stage. Therefore, REFCLK is divided by two in the divide-by-four mode and divided by four in the divide-by-eight mode.

PIN DESCRIPTIONS

Input Signals

TTLREF. TTL. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the FOUT0–FOUT3 outputs. INPSEL is used to select between this reference and the PECL reference PECLREFP/N.

PECLREFP/N. Differential PECL. Frequency reference supplied by the user. Selectable by the INPSEL input.

FBCLK. Feedback clock that, along with the reference clock input, determines the frequency of the FOUT0–FOUT3 outputs. One output is selected to feed back to this input. (See Table 3.)

DIVSEL. Controls the divider circuit that follows the VCO. When DIVSEL is low, the VCO frequency is divided by four. When DIVSEL is high, the VCO frequency is divided by eight. (See Tables 1 and 3.)

PHSEL0. This input, along with PHSEL1, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

PHSEL1. Along with PHSEL0, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

OUTEN0. Active Low. Output enable signal that controls which outputs toggle. Controls the frequency doubler output (X2FOUT) and the half-frequency output (HFOUT).

OUTEN1. Active Low. Output enable signal that controls which outputs toggle. Controls the FOUT0–FOUT3 outputs.

RESET. Active Low. Initializes internal states for test purposes.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Therefore, REFCLK can be divided by two in the divide-by-four mode, and divided by four in the divide-by-eight mode, and used to directly sequence the outputs.

INPSEL. Allows user to select between TTLREF and PECLREF reference frequencies. When INPSEL is High, the PECLREF input is selected.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and capacitor) to be included in the PLL.

X2FOUT. Provides a clock signal identical to the FOUT0 output in the divide-by-four mode and twice the FOUT0 frequency (maximum of 80 MHz) in the divide-by-eight mode.

FOUT0. Clock output.

FOUT1. Clock output.

FOUT2. Clock output.

FOUT3. Clock output.

HFOUT. Provides a clock signal in phase with the FOUT0 output, but at half the FOUT0 frequency in both the divide-by-four and divide-by-eight modes.

PECLP/N. Differential PECL output, always one-half the VCO frequency.

LOCK. Goes high when the reference clock and FBCLK are within 2–4 ns of each other, demonstrating that the PLL is in lock.

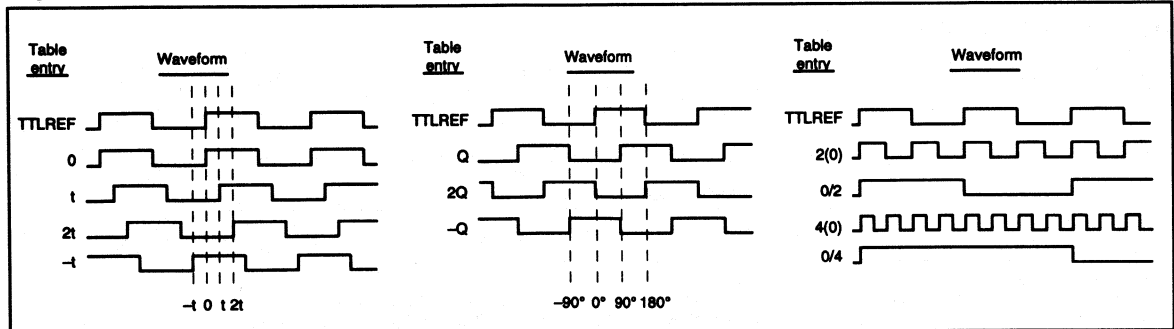
Table 3. Output Select Matrix

Configuration Number	Select Pins		Output Fed to FBCLK	Output Phase Relationships					+4	+8
	PHSEL1	PHSEL0		FOUT0	FOUT1	FOUT2	FOUT3	HFOUT		
1	0	0	FOUT0-FOUT3	0	0	0	0	0/2	0	2(0)
2	0	0	HFOUT	2(0)	2(0)	2(0)	2(0)	0	2(0)	4(0)
3	0	0	X2FOUT (+8)	0/2	0/2	0/2	0/2	0/4		0
4	0	1	FOUT0	0	Q	2Q	3Q	0/2	0	2(0)
5	0	1	FOUT1	-Q	0	Q	2Q	-Q/2	-Q	2(-Q)
6	0	1	FOUT2	-2Q	-Q	0	Q	-2Q/2	-2Q	2(-2Q)
7	0	1	FOUT3	-3Q	-2Q	-Q	0	-3Q/2	-3Q	2(-3Q)
8	0	1	HFOUT	2(0)	2(Q)	2(2Q)	2(3Q)	0	2(0)	4(0)
9	0	1	X2FOUT (+8)	0/2	Q/2	2Q/2	3Q/2	0/4		0
10	1	0	FOUT0	0	-t	t	Q	0/2	0	2(0)
11	1	0	FOUT1	t	0	2t	Q+t	1/2	t	2(t)
12	1	0	FOUT2	-t	-2t	0	Q-t	-1/2	-t	2(-t)
13	1	0	FOUT3	-Q	-Q-t	-Q+t	0	-Q/2	-Q	2(-Q)
14	1	0	HFOUT	2(0)	2(-t)	2(t)	2(Q)	0	2(0)	4(0)
15	1	0	X2FOUT (+8)	0/2	-1/2	1/2	Q/2	0/4		0
16	1	1	FOUT0	0	t	2t	3t	0/2	0	2(0)
17	1	1	FOUT1	-t	0	t	2t	-1/2	-t	2(-t)
18	1	1	FOUT2	-2t	-t	0	t	-2V/2	-2t	2(-2t)
19	1	1	FOUT3	-3t	-2t	-t	0	-3V/2	-3t	2(-3t)
20	1	1	HFOUT	2(0)	2(t)	2(2t)	2(3t)	0	2(0)	4(0)
21	1	1	X2FOUT (+8)	0/2	1/2	2V/2	3V/2	0/4		0

Notes:

1. "0" implies the output is aligned with the reference clock.
2. "t" implies the output lags the reference clock by a minimum phase delay.
3. "Q" implies the output lags the reference clock by 90° of phase.
4. "-t" implies the output leads the reference clock by a minimum phase delay.
5. "-Q" implies the output leads the reference clock by 90° of phase.
6. "2()" implies the output is at twice the frequency of the reference clock.
7. "1/2" implies the output is at half the frequency of the reference clock.
8. The PECLN/P Differential PECL output is not affected by the PHSEL inputs.

Legend



ABSOLUTE MAXIMUM RATINGS

TTL Supply Voltage VCC (GND = 0)	7.0 V
TTL Input Voltage (GND = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Nom	Max	Units
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

DC CHARACTERISTICS (TTL I/O)

Symbol	Parameter	DC Test Conditions	Min	Typ ¹	Max	Units
V _{IH} ²	Input HIGH Voltage (TTL)	Guaranteed input HIGH voltage for all inputs	2.0			V
V _{IL} ²	Input LOW Voltage (TTL)	Guaranteed input LOW voltage for all inputs			0.8	V
V _{IK}	Input clamp diode voltage	V _{CC} = Min, I _{IN} = -18mA		-0.8	-1.2	V
V _{OH}	Output HIGH Voltage	V _{CC} = Min	I _{OH} = -12mA ³	2.4		V
			I _{OH} = -24mA ³	2.0		V
V _{OL}	Output LOW Voltage	V _{CC} = Min			0.5	V
I _{IH}	Input HIGH Current	V _{CC} = Min, V _{IN} = 2.7V			10	µA
I _I	Input HIGH Current at Max	V _{CC} = Max, V _{IN} = V _{CC}			1.0	mA
I _{IL}	Input LOW Current	V _{CC} = Min, V _{IN} = 0.5V	INPSEL		-300	µA
			Others		-50	µA
I _{OS} ⁴	Output short circuit current	V _{CC} = Max, V _{OUT} = 0V	-25		-100	mA
I _{CC}	Static	V _{CC} = Max			95	mA
I _{CC} T	Total I _{CC} (Dynamic and Static)	C _{LOAD} = 25pF at 50 MHz			200	mA

DC CHARACTERISTICS (PECL I/O)

Symbol	Parameter	DC Test Conditions	Min	Typ ¹	Max	Units
V _{IH} ²	Input HIGH Voltage (PECL)	Guaranteed input HIGH voltage for all inputs	V _{CC} -1145		V _{CC} -600	V
V _{IL} ²	Input LOW Voltage (PECL)	Guaranteed input LOW voltage for all inputs	V _{CC} -2000		V _{CC} -1450	V
V _{OH}	Output HIGH voltage	V _{CC} = 5.0 V Load = 50Ω to V _{CC} -2V	V _{CC} -1075		V _{CC} -650	V
V _{OL}	Output LOW voltage		V _{CC} -1980		V _{CC} -1585	V

1. Typical limits are at 25°C, V_{CC} = 5.0V.

2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher and are optimized to balance rise and fall times.

4. Maximum test duration one second.

Table 4. AC Specifications

Symbol	Description	S4405B-66		S4405B-80		Units
		Min	Max	Min	Max	
f_{VCO}	VCO Frequency	160	266	160	320	MHz
f_{REF}	REFCLK Frequency	10	66	10	80	MHz
MPW_{REF}	REFCLK Minimum Pulse Width	5.0		5.0		ns
t_{PE}	Phase Error between TTLREF and FBCLK	-1	0	-1	0	ns
t_{PEP}	Phase Error between PECLREF and FBCLK	-3	-1	-3	-1	ns
t_{PED}	Phase Error Difference from Part to Part ¹	0	750	0	750	ps
t_{SKEW}	Output Skew ² (TTL)	0	400	0	400	ps
t_{DC}	Output Duty Cycle	45	55	45	55	%
f_{PECL}	PECLP/N Frequency	80	132	80	160	MHz
f_{FOUT}	FOUT Frequency ³ (TTL)	20	66	20	80	MHz
f_{HFOUT}	HFOUT Frequency ³	10	33	10	40	MHz
f_{2XFOUT}	2XFOUT Frequency ³	40	66	40	80	MHz
t_{PS}	Nominal Phase Shift Increment	3.75	6.25	3.125	6.25	ns
t_{OFD}	Tpd OUTEN0-2 to FOUTs, Disable	2	7	2	7	ns
t_{OFE}	Tpd OUTEN0-2 to FOUTs, Enable	2	7	2	7	ns
t_{IRF}	Input Rise/Fall Time	1	3	1	3	ns
t_{ORF}	FOUT Rise/Fall Time ⁴	0.5	1.5	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time ⁵		5		5	ms

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. $C_{LOAD} = 35$ pF.
4. With 35 pF output loading (0.8 V to 2.0 V transition).
5. Depends on loop filter chosen. (Number given is for example filter.)

Figure 5. Timing Waveforms

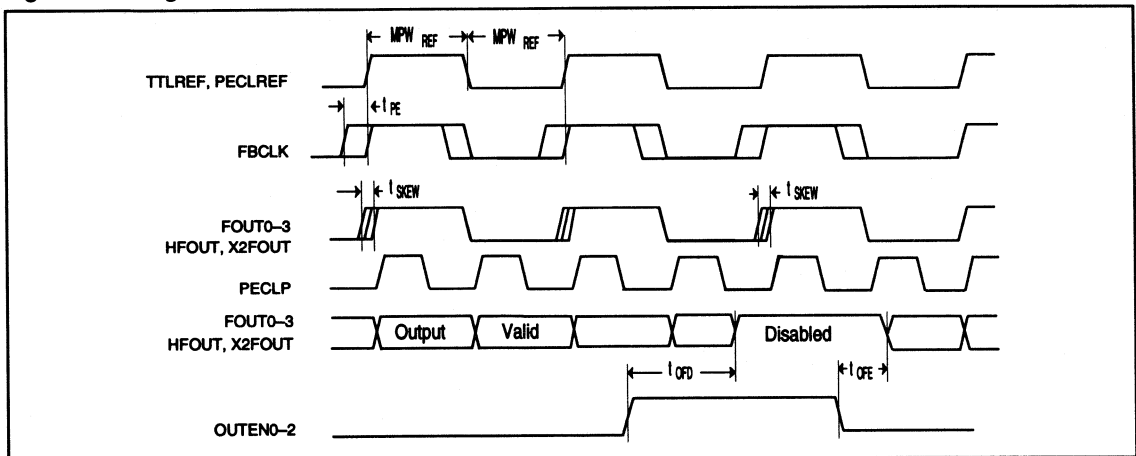
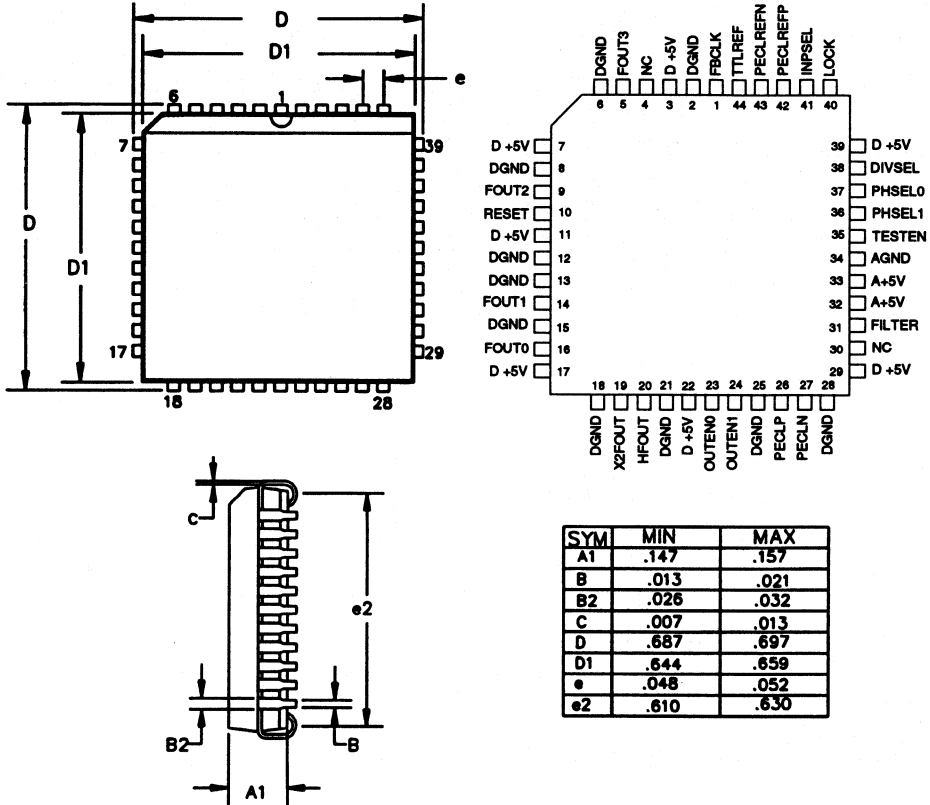


Figure 6. S4405 44 PLCC Package and Pinout

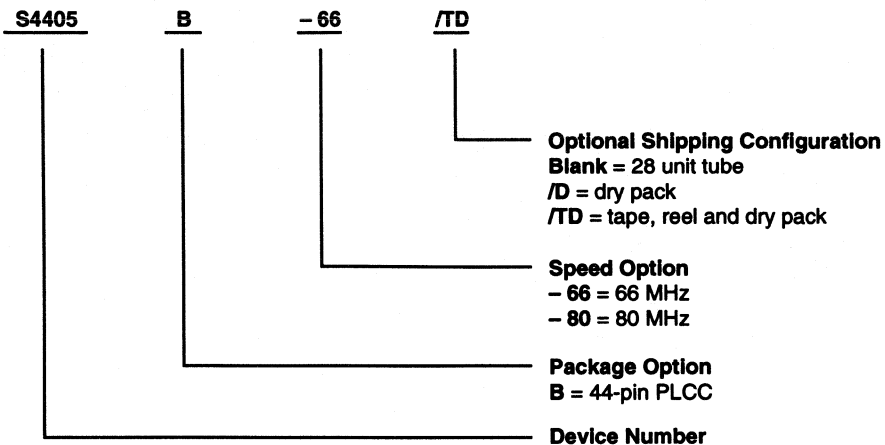


All dimensions nominal in inches.

Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Speed Option (if applicable)**
- **Optional Shipping Configuration**



Example: S4405B-66/D
44-pin PLCC package, 66 MHz, dry packed in the standard tube.

FEATURES

- Generates outputs from 20 MHz to 66 MHz
- Four groups of three outputs (12 outputs total)
- Eight user-selectable output functions for each group
- TTL compatible outputs, with <1.5-ns edge rates
- Performs clock doubling, dividing, invert, lead/lag placement
- Internal VCO running between 160 to 266 MHz
- 1.0μ BiCMOS technology
- Output skew less than 500 ps
- 52 PQFP package

APPLICATIONS

- High-performance microprocessor systems
- CMOS ASIC systems
- Backplane clock deskew and distribution
- Compatible with Intel's Pentium™ processor

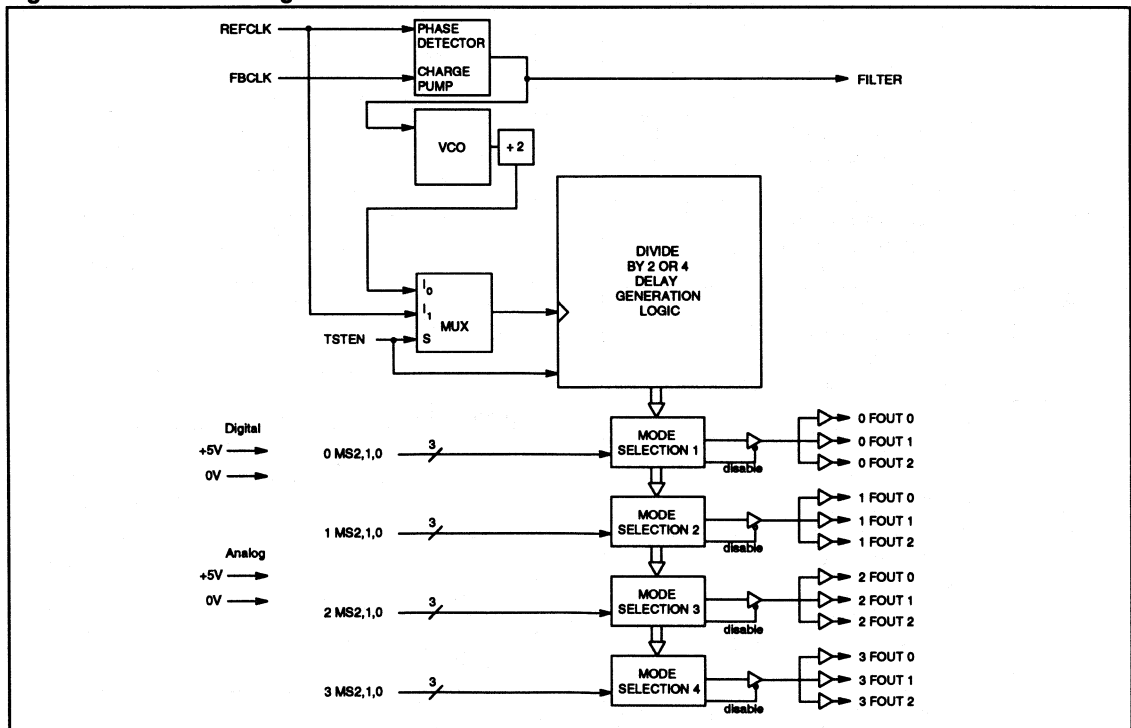
GENERAL DESCRIPTION

The S4406 BiCMOS clock generator provides 12 TTL outputs with less than 500 ps of skew. Implemented in AMCC's 1.0μ BiCMOS technology, the internal PLL and divider/delay selector logic allow the user to individually tailor the (4) TTL output groups to the system's needs. The internal VCO can operate between 160 to 266 MHz, and the programmability allows the user to generate output clocks in the 20–66 MHz range.

The S4406 offers the user the ability to select the appropriate phase and frequency relationship for each of the four groups of three TTL clock outputs.

In addition to clock doubling and inversion functions, the S4406 allows any output groups to lead or lag the others by the minimum phase delay of 3.75–6.25 ns.

Figure 1. S4406 Block Diagram



FUNCTIONAL DESCRIPTION

The 12 xFOUT0–2 outputs are the main TTL output clocks that the generator supplies. The mode selection choices are shown in Table 1 and waveform definitions are given in Figure 2. The “x” represents the output group number (1–4). The frequency of these outputs is determined by the REFCLK clock frequency and the output clock that is tied to the FBCLK input (xFOUT0–2 can be equal to REFCLK, half of REFCLK, or twice the frequency of REFCLK).

Example:

In order to meet bus timing specifications for a typical system, designers may need three outputs at 66 MHz for the system clock and processor, a 33-MHz output for the cache controller, and a 33-MHz delayed output for a memory management unit. This system requirement can be met using the S4406 by setting the mode select pins for the first group of outputs (0MS2,1,0) to 111, the second group (1MS2,1,0) to

Table 1. Mode Selection Options

xMS2,1,0	MODE DESCRIPTION	xFOUT0,1,2
000	Disabled.	Logical Hi
001	All three outputs at the fundamental output frequency, but early by a minimum phase delay.	f – t
010	All three outputs at half the fundamental output frequency and inverted.	1/2
011	All three outputs at the fundamental output frequency and inverted.	1
100	All three outputs at half the fundamental output frequency, but delayed by a minimum phase delay.	f/2 + t
101	All three outputs at the fundamental output frequency, but delayed by a minimum phase delay.	f + t
110	All three outputs at half the fundamental output frequency.	f/2
111	All three outputs at the fundamental output frequency.	f

Note: If f is fed back, the fundamental frequency is equal to REFCLK.
If f/2 is fed back, the fundamental frequency is twice REFCLK.

110, and the third group (2MS2,1,0) to 101. In this configuration, one of the 33-MHz outputs should be fed back to the FBCLK input. This example makes use of only three of the four output banks, leaving the fourth available for any other clock signals needed.

Filter

FILTER is the analog signal from the phase detector going into the VCO. This pin is provided so a simple external filter (a single capacitor and resistor) can be included in the phase locked loop of the clock generator. See Figure 3.

Phase Delay

The minimum phase delay between xFOUT0–2 signals is a function of the VCO frequency. The VCO frequency can be determined by multiplying the fundamental output frequency by four, or half the fundamental frequency by eight. The minimum phase delay is equal to the period of the VCO frequency: $t = 1/(\text{VCO freq.})$. Since the VCO can operate in the 160-MHz to 266-MHz range, the range of minimum phase delay values is 6.25 ns to 3.75 ns (See Table 2).

Figure 2. Waveform Definitions

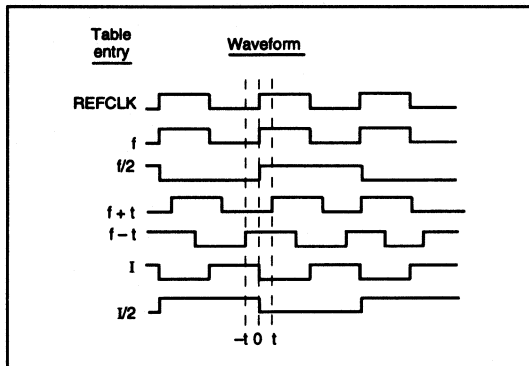
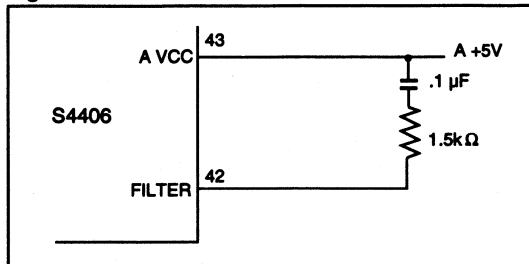


Figure 3. External PLL Filter



Test Capabilities

TESTEN allows the chip to use the REFCLK input instead of the VCO output to clock the chip. This is used during chip test to allow the counters and control logic to be tested independently of the VCO. In addition, when TESTEN is brought High, an internal RESET pulse is generated. This initializes the internal counter flip-flops to zeros, and at the end of the next clock cycle, the outputs go to a zero state. TESTEN can also be used for board testing to allow the user to control the output clocks from the S4406 by inputting the board clock to the REFCLK input.

Table 2. VCO Operating Frequencies

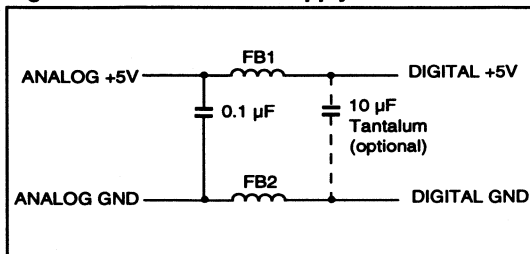
xFOU0-2	VCO FREQ	MIN PHASE DELAY
66.6 MHz	266 MHz	3.750 ns
50 MHz	200 MHz	5.000 ns
40 MHz	160 MHz	6.250 ns
33.3 MHz	266 MHz	3.750 ns
25 MHz	200 MHz	5.000 ns
20 MHz	160 MHz	6.250 ns

The bank containing the output used as feedback must be in one of the $f/2$ modes to ensure the VCO is operating within its 160-266 MHz range.

Power Supply Considerations

Power for the analog portion of the S4406 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 4). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or induc-

Figure 4. External Power Supply Filter



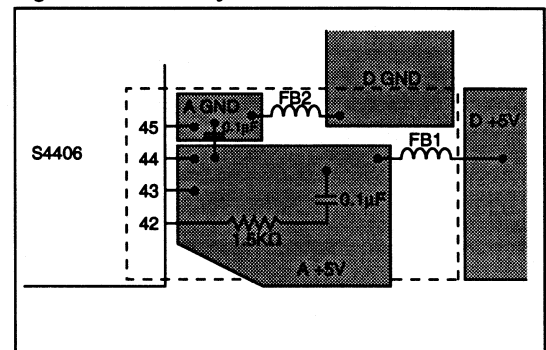
tors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise.

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

BOARD LAYOUT CONSIDERATIONS

- The S4406 chips are sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.
- All decoupling capacitors ($C1-C4 = 0.1 \mu\text{F}$) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4406 and the power and ground plane connections.
- No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 5) to avoid the possibility of noise due to crosstalk.
- The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.
- The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

Figure 5. Board Layout



PIN DESCRIPTIONS**Input Signals**

REFCLK. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the outputs. Also replaces the VCO output when TSTEN is high (after first divide-by-two stage in divider phase control logic). See TSTEN.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the outputs. One output is selected to feed back to this input.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Also, when brought High, generates an internal Reset pulse that initializes the internal counter flip-flops to zero.

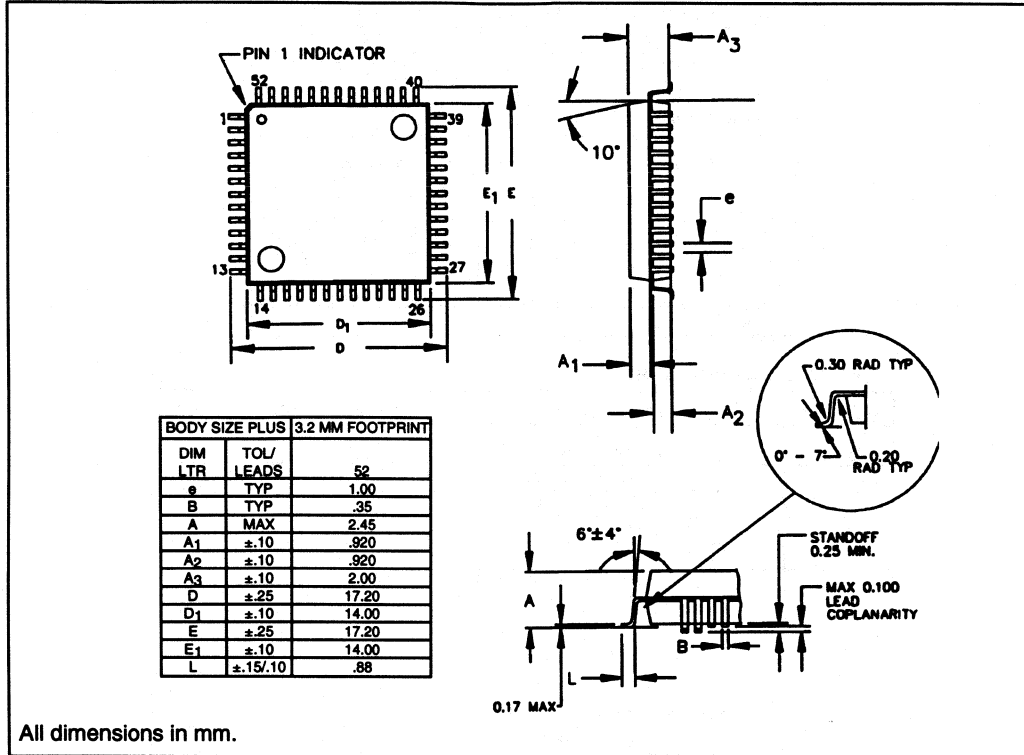
xMS2,1,0. Mode selection inputs that allow selection of the phase and frequency relationship of each of the four banks of three clock outputs. The "x" represents the output group number (0–3). Refer to Table 1 for mode selection options.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and one capacitor) to be included in the PLL.

xFOUT0–2. Clock signal outputs. Refer to Table 1 and Figure 4 for a description of output options.

Figure 6. 52-pin PQFP Package



DC CHARACTERISTICS

Symbol	Parameter	DC Test Conditions	Min	Typ ¹	Max	Units
V _{IH} ²	Input HIGH Voltage	Guaranteed input HIGH voltage for all inputs	2.0			V
V _{IL} ²	Input LOW Voltage	Guaranteed input LOW voltage for all inputs			0.8	V
V _{IK}	Input clamp diode voltage	V _{CC} = Min, I _{IN} = -18 mA		-0.8	-1.2	V
V _{OH}	Output HIGH Voltage	V _{CC} = Min, I _{OH} = -12 mA ³	2.4			V
		I _{OH} = -24 mA ³	2.0			V
V _{OL}	Output LOW Voltage	V _{CC} = Min, I _{OL} = 24 mA ³			0.5	V
I _{IH}	Input HIGH Current	V _{CC} = Min, V _{IN} = 2.4V			-200	μA
		4MS2,3MS2,1,0			50	μA
		Other			1.0	mA
I _I	Input HIGH Current at Max	V _{CC} = Max, V _{IN} = V _{CC}			1.0	mA
I _{IL}	Input LOW Current	V _{CC} = Min, V _{IN} = 0.5V			-500	μA
		4MS2,3MS2,1,0			-50	μA
		Other			-50	μA
I _{OS} ⁴	Output short circuit current	V _{CC} = Max, V _{OUT} = 0V	-25		-100	mA
I _{CC}	Static	V _{CC} = Max			70	mA
I _{CC} T	Total I _{CC} (Dynamic and Static)	C _{LOAD} = 25 pF at 50 MHz			200	mA

1. Typical limits are at 25°C, V_{CC} = 5.0V.
2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher.
4. Maximum test duration one second.

ABSOLUTE MAXIMUM RATINGS

TTL Supply Voltage VCC (VEE = 0)	7.0 V
TTL Input Voltage (VEE = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature T _J	+ 130°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Nom	Max	Units
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

Table 3. AC Specifications

Symbol	Description	Min	Max	Units
f _{VCO}	VCO Frequency	160	266	MHz
f _{REF}	REFCLK Frequency	20	66	MHz
t _{IRF}	Input Rise/Fall Time	1	3	ns
MPW _{REF}	REFCLK Minimum Pulse Width	5.0		ns
t _{PE}	Phase Error between REFCLK and FBCLK	-1.0	0	ns
t _{PED}	Phase Error Difference from Part to Part ¹	0	750	ps
t _{SKEW}	Output Skew ² across all outputs	0	500	ps
t _{SKEWA}	Output Skew ² within any bank	0	250	ps
t _{DC}	Output Duty Cycle ³	45	55	%
f _{FOUT}	FOUT Frequency ⁴	10	66	MHz
t _{PS}	Nominal Phase Shift Increment ⁵	3.75	6.25	ns
t _j	Clock Stability ⁶		500	ps
t _{ORF}	FOUT Rise/Fall Time ⁷	0.5	1.5	ns
t _{LOCK}	Loop Acquisition Time ⁸		5	ms
t _{PSV}	Phase Shift Variation ⁵	-250	+250	ps

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. Outputs loaded with 35 pF, measured at 1.5 V.
4. C_{LOAD} = 35 pF.
5. All phase shift increments and variation are measured relative to 0FOUT0 at 1.5 V.
6. Clock period jitter with all FOUT outputs operating at 66MHz loaded with 25 pF using loop filter shown. Parameter guaranteed, but not tested.
7. With 35 pF output loading (0.8 V to 2.0 V transition).
8. Depends on loop filter chosen. (Number given is for example filter.)

Figure 7. Timing Waveforms

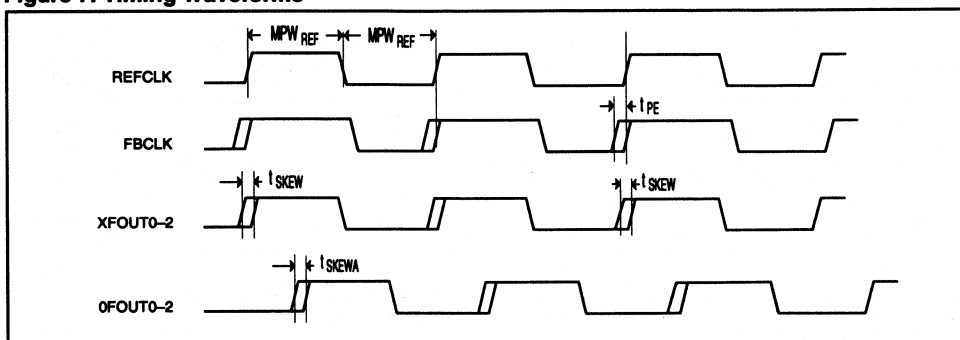
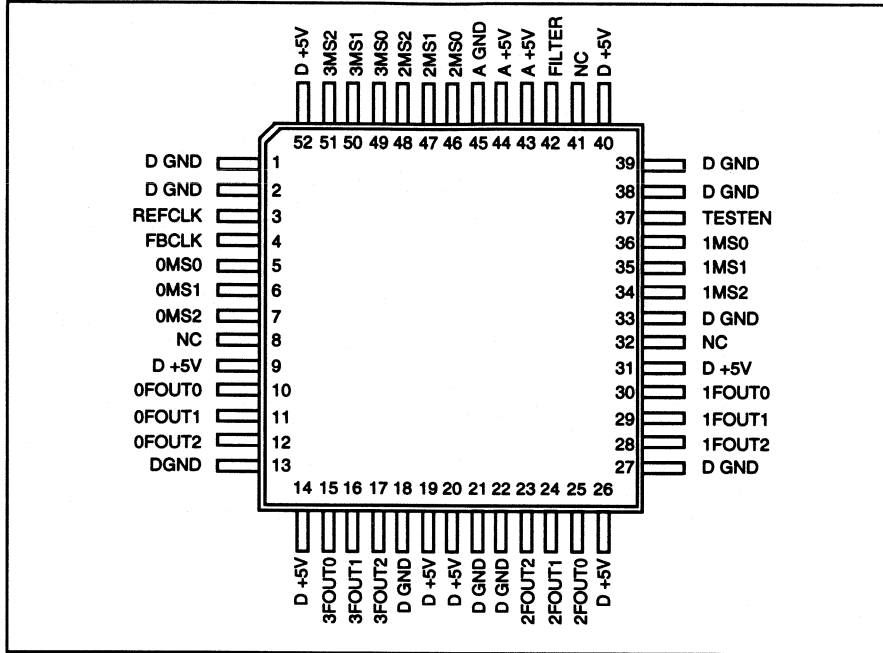


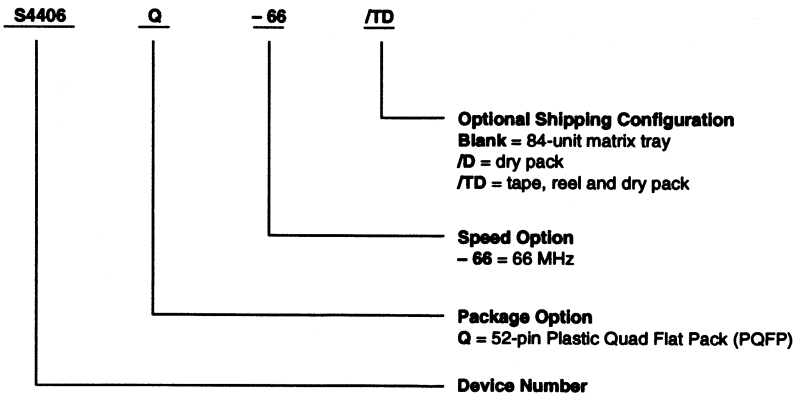
Figure 8. S4406 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- Device Number
- Package Type
- Speed Option (if applicable)
- Optional Shipping Configuration



Example: S4406Q-66/D
52-pin PQFP package, 66 MHz, shipped dry packed in the standard matrix tray.

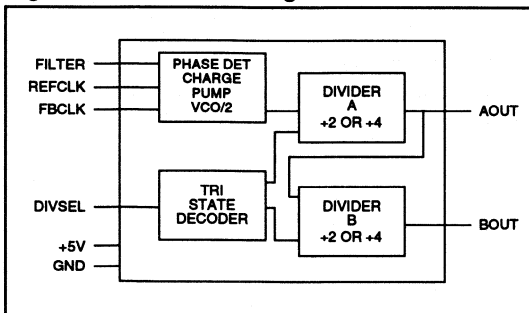
FEATURES

- Performs X2 and X4 Multiplication on Input Clock Frequency
- Eliminates the need for High Speed Crystals
- Simplifies Clock Routing by Reducing High-Speed Clock Traces
- Generates 2 TTL Outputs, 50 and 100 MHz max
- Output Skew ± 200 ps max
- 160–400 MHz PLL
- Space Saving 8-pin SIP or SOIC
- Reduces System EMI Generation
- Less than 0.3 W at 80 MHz
- Proven 1.5 Micron BiCMOS Technology

APPLICATIONS

- “Deskewing” ASIC Devices
- RISC and High Performance Microprocessor Systems
- Clocking synchronous DRAMS and Memory Modules

Figure 1. S4501 Block Diagram



GENERAL

The S4501 has two clock inputs, REFCLK and FBCLK and two outputs AOUT and BOUT providing signals at 2X and 4X the REF frequency. The frequency of AOUT depends on DIVSEL and the choice of outputs (frequencies) fed back to the FBCLK input. See Figure 1.

The S4501 Clock Multiplier allows a 1/2 or 1/4 speed clock to be routed to the device which in turn produces 2X or 4X multiples to meet high speed clock requirements.

The S4501 can also be used as a “zero-delay” buffer to provide multiple frequency outputs in sync with the reference clock.

In applications requiring ASIC “deskewing,” using an output of the ASIC as FBCLK to the S4501 allows that output (and others related to it) to be synchronized to the REFCLK to within ± 500 ps. The S4501’s PLL will then actively align the clock of the ASIC to compensate for its nominal propagation delay as well as any variation due to process or operating conditions.

Table 1. AC Performance Summary

Description	Min	Max	Units
Input Frequency	10	100	MHz
Phase Error	—	± 500	ps
Output Skew		± 200	ps
Output Freq.	10	100	MHz

Table 2. DC Performance Summary

Description	Min	Max	Units
Output Current	-24	+24	mA
Voh @ -16 mA	24		V
Vol @ +24 mA		0.5	V
Icc		55	mA

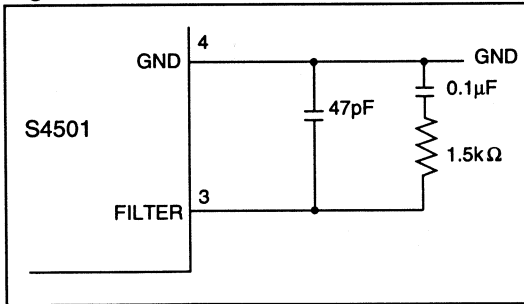
Filter

The FILTER output is a tap between the analog output of the phase detector and the VCO input. This pin allows a simple external filter (Figure 2) to be included in the PLL. AMCC recommends the use of the filter component values shown. This filter was chosen for its ability to reduce the output jitter and filter out noise on the REFCLK input. The filter components should be in surface mounted packages with minimum lead inductance.

Power Supply Considerations

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

Figure 2. External PLL Filter



PIN DESCRIPTIONS

Input Signals

REFCLK. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the A and B outputs.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the A and B outputs. One output is selected to feed back to this input. (See Table 3, DIVSEL is Tri-State Logic.)

DIVSEL. Controls the divider circuit that follows the VCO. Uses tri-state logic where low $V_{CC}/2$, mid =

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and one capacitor) to be included in the PLL.

AOUT. TTL output. Frequency depends on VCO speed and DIVSEL level.

BOU. TTL output. $1/2$ or $1/4$ the frequency of AOUT depending on DIVSEL level.

Table 3. DIVSEL is Tri-State Logic

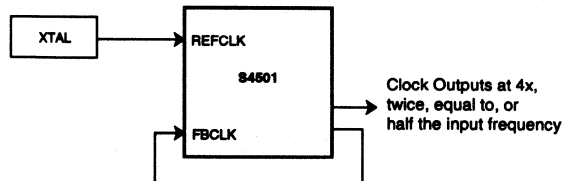
DIVSEL	DIVIDER A	DIVIDER B	Where:
L	X/4	A/4	L=GND M=VCC/2 H=VCC X=VCO/2
M	X/4	A/2	
H	X/2	A/4	

TYPICAL APPLICATIONS

The S4501 is designed to meet a large variety of system clocking requirements. Several typical applications are provided below.

Application 1. High-Frequency, Low-Skew Clock Generation

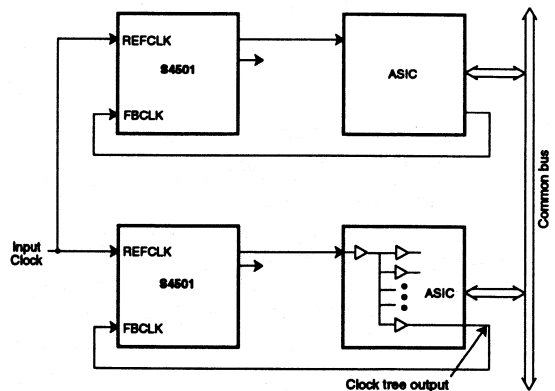
One of the most basic capabilities of the device is generating phase-aligned clocks at various multiples of the input clock frequency. For example, in a multiple-board system a half-frequency clock can be generated for use across the backplane, where it is simpler to route a low-speed signal. This signal can then be doubled on the boards, and synchronization will be maintained.



Application 2. Delay Compensation

Since the relative edges of the REFCLK and FBCLK inputs are precisely controlled, the S4501 can be used to compensate for different delays due to trace lengths or to internal chip delays, simplifying board layout and bus timing. In the example shown, the two ASICs have a difference of several nanoseconds in their propagation delays. The S4501 ensures that the output signals are aligned, so that the data valid uncertainty on the common bus is minimized.

Temperature and voltage effects on prop delays through the ASICs can also be minimized by the S4501's on-board PLL when in this configuration.



Absolute Maximum Ratings

Commercial

TTL Supply Voltage VCC (VEE = 0)	7.0 V
TTL Input Voltage (VEE = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature T _J	+ 130°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions

Parameter	Commercial			Units
	Min	Nom	Max	
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

DC Characteristics

Symbol	Parameter	DC Test Conditions	Min	Typ ¹	Max	Units
V _{IH} ²	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			V
V _{IL} ²	Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8	V
V _{IK}	Input clamp diode voltage	VCC = Min, I _{IN} = -18mA		-0.8	-1.2	V
V _{OH}	Output HIGH voltage	VCC = Min	I _{OH} = -12mA ³ (COM)	2.4		V
			I _{OH} = -24mA ³ (COM)	2.0		V
V _{OL}	Output LOW voltage	VCC = Min			0.5	V
I _{IH}	Input HIGH current	VCC = Min, V _{IN} = 2.4V			50	μA
I _I	Input HIGH current at max	VCC = Max, V _{IN} = VCC			1.0	mA
I _{IL}	Input LOW current	VCC = Min, V _{IN} = 0.5V			-50	μA
I _{OS} ⁴	Output short circuit current	VCC = Max, V _{OUT} = 0V	-25		-100	mA
I _{CC}	Static	VCC = Max			50	mA
I _{CC}	Total I _{CC} (Dynamic and Static)	V _{LOAD} = 25pF at 50 MHz			75	mA

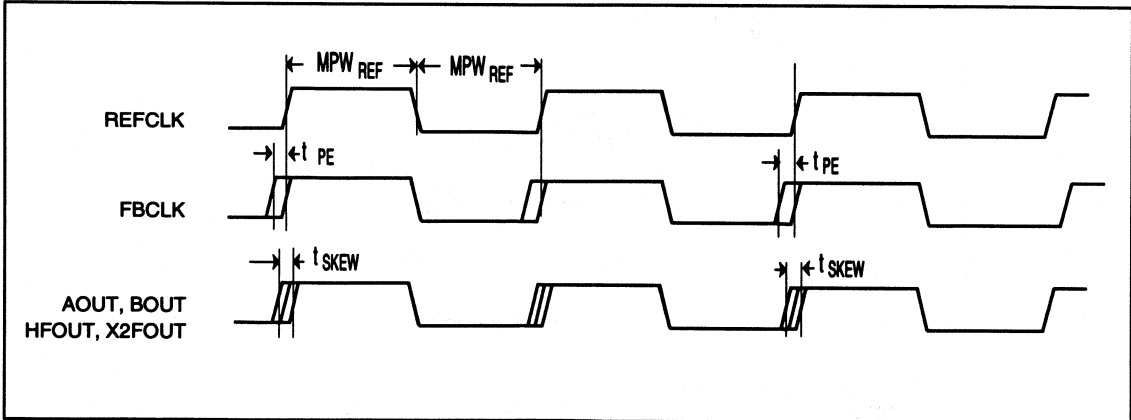
1. Typical limits are at 25°C, V_{CC} = 5.0V.
2. These input levels should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher and are optimized to balance rise and fall times.
4. Maximum test duration is one second.

Table 4. AC Specifications

Symbol	Description	Min	Max	Units
f_{VCO}	VCO Frequency	160	400	MHz
f_{REF}	REFCLK Frequency	10	100	MHz
MPW_{REF}	REFCLK Minimum Pulse Width	4		ns
t_{PE}	Phase Error between REFCLK and FBCLK	-500	+500	ns
t_{PED}	Phase Error Difference from Part to Part ¹	0	750	ps
t_{SKEW}	Output Skew ²	0	400	ps
t_{DC}	Output Duty Cycle ³	45	55	%
f_{FOUT}	AOUT Frequency ⁴	20	100	MHz
f_{HFOUT}	BOUT Frequency ⁴	10	50	MHz
t_{RF}	Input Rise/Fall Time	1	3	ns
t_{ORF}	AOUT, BOUT Rise/Fall Time ⁵	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time ⁶		5	ms
t_j	Clock Stability ⁷		500	ps

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. Outputs loaded with 35pF, measured at 1.5V.
4. $C_{LOAD} = 35$ pF.
5. With 35 pF output loading (0.8 V to 2.0 V transition).
6. Depends on loop filter chosen. (Number given is for example filter.)
7. Clock period jitter with both outputs operating at 66 and 33 MHz, loaded with 25pF using loop filter shown. Parameter guaranteed, but not tested.

Figure 5. Timing Waveforms



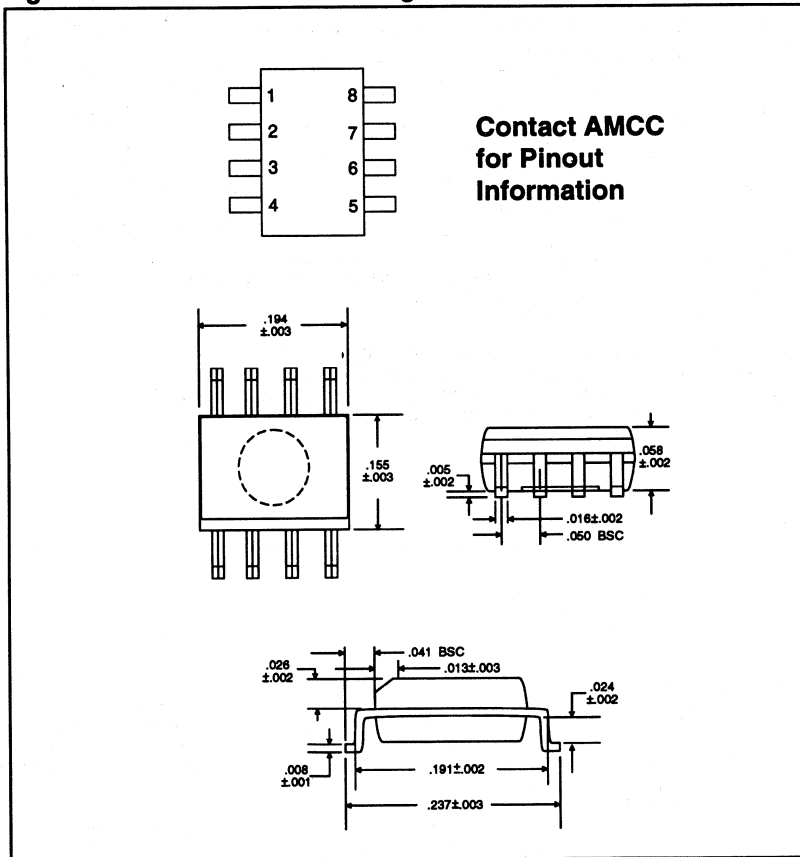
BOARD LAYOUT CONSIDERATIONS

- The S4501 is sensitive to noise on the +5V and Filter pins. Care should be taken during board layout for optimum results.
- All decoupling capacitors (0.1 μ F) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4501 and the power and ground plane connections.

ramic chip caps) and placed on top of board between S4501 and the power and ground plane connections.

- No dynamic signal lines should pass through or beneath the filter circuitry area to avoid the possibility of noise due to crosstalk.

Figure 5. 8-Pin SOIC Pinout/Package



Ordering Information

GRADE	PLL CLOCK GENERATOR	PACKAGE
S-commercial	4501	S-8-pin SOIC



FEATURES

- Multiplies input reference frequency by integers 2-32
- Digitally programmable output clock frequencies from 10 MHz to 300 MHz
- Two (2) groups of independent clock outputs
 - One group consists of differential PECL outputs
 - One group is a pair of TTL outputs
- Proprietary TTL output drivers with:
 - Complementary 24 mA peak outputs, source and sink
 - Source series termination
 - Edge rates less than 1.5 ns
- Low 250 ps reference typ clock jitter (PECL outputs), 400 ps max
- 1.1 mW or less power dissipation, frequency and load dependent
- 150 MHz to 300 MHz phase-locked loop VCO frequency range
- Advanced BiCMOS process technology
- Space saving 28 PLCC package

GENERAL DESCRIPTION

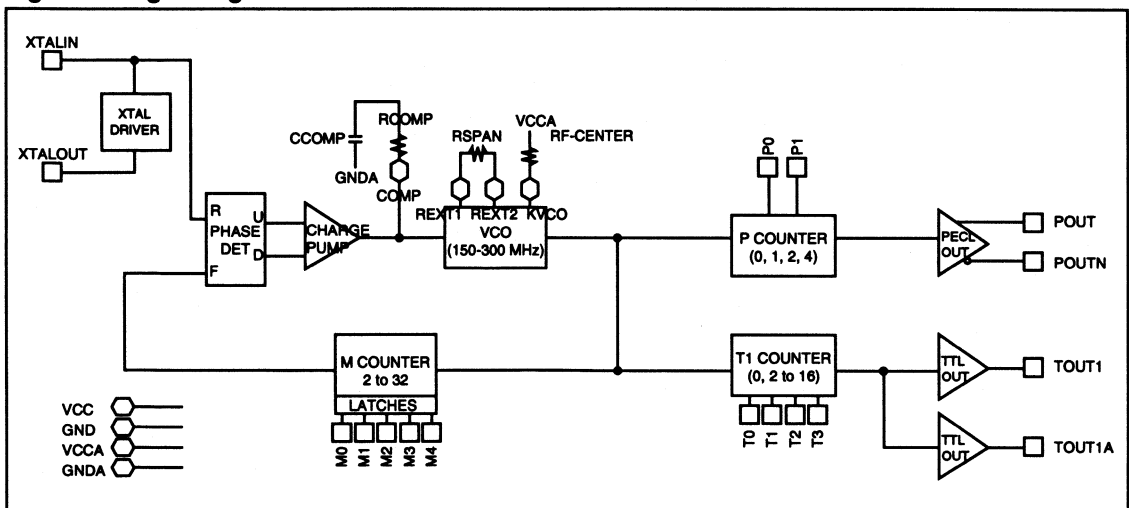
The S4503 is a clock synthesizer which utilizes phase-locked loop technology to provide two (2) independently selectable output frequencies in the 10 MHz to 300 MHz range. A reference input may be provided by either a low cost crystal or a TTL frequency source.

The first of the two (2) output frequency groups consists of a pair of differential PECL (Positive referenced ECL) outputs which will operate up to 300 MHz. The second group (TTL) consist of two outputs with selectable frequency, up to 80 MHz.

The final frequency for each group is digitally selected via three programmable counters. One counter is used to set the internal VCO frequency between 150 MHz to 300 MHz, and the others are used to divide the VCO frequency from 2 thru 16 (TTL) and 1, 2 or 4 (PECL).

All phase-locked loop elements are provided on chip with the exception of the passive components needed for the loop filter function and VCO.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature -55°C to +150°C
 V_{CC} Potential to Ground -0.5V to +7.0V
 Input Voltage -0.5V to +V_{CC}
 Static Discharge Voltage >1750V
 Maximum Junction Temperature +130°C
 Latch-up Current >200 mA
 Operating ambient temperature 0°C to +70°C

Capacitance (package)

Input Pins 5.0 pF
 TTL Output Pins 5.0 pF
 PECL Output Pins 5.0 pF

AC Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C

Symbol	Description	Conditions	MIN	MAX	Units
F _{VCO}	VCO Frequency		150	300	MHz
F _{XTL}	XTL Frequency, Fundamental	XTLIN to XTLOUT	5	25	MHz
F _{TTL}	TTL Input Frequency	Standard TTL Levels	5	80	MHz
F _{out}	PECL Out Frequency		37	300	MHz
T _{OUTn}	TTL Out Frequency		9	80	MHz
T _{SKEW T-T}	TTL to TTL Output Skew	TTL Leading Edges at +1.5V		250	ps
T _{SYM-T}	T _{OUT} Symmetry	Measured at 1.5V		±1.5	ns
T _{SYM-P}	PECL Out Symmetry	Measured at differential crossing points		±250	ps
T _J	PECL Clock Jitter, pk to pk			400	ps

Notes:

1. Max cycle to cycle jitter.
2. Output symmetry is the deviation from a 50% duty cycle.
3. All AC parameters are tested or guaranteed by characterization.

Electrical Characteristics
 $V_{CC} = +5.0V \pm 5\%$, $T_a = 0^\circ C$ to $+70^\circ C$

Symbol	Parameter	Conditions	Min	Max	Units
$V_{OH}(PECL)$	Output HIGH Voltage, ECL	50 Ohms to $V_{CC}2V$	$V_{CC}1075$	$V_{CC}650$	mV
$V_{OL}(PECL)$	Output LOW Voltage, ECL	50 Ohms to $V_{CC}2V$	$V_{CC}1980$	$V_{CC}1585$	mV
$V_{OH}(TTL)$	Output HIGH Voltage	$F_{OUT} = 80$ MHz max, $C_L = 10pF$	24		V
$V_{OL}(TTL)$	Output LOW Voltage, TTL	$F_{OUT} = 80$ MHz max, $C_L = 10pF$		0.6	V
$V_{IH}(TTL)$	Input (TTL) HIGH Voltage	All TTL Inputs	2.0	V	V
$I_{IL}(TTL)$	Input (TTL) LOW Voltage	All TTL Inputs	-0.5	0.8	V
$I_{OH}(PECL)$	Output HIGH Current	50 Ohms to $V_{CC}2.0$		25	mA
$I_{OL}(PECL)$	Output LOW Current	50 Ohms to $V_{CC}2.0$		8	mA
$I_{IH}(TTL)$	Input HIGH Current	$V_{in} = V_{CC}$		200	μA
$I_{IL}(TTL)$	Input LOW Current	$V_{in} \leq 0.8$		50	μA
I_{OHS}^1	Output HIGH Short Current	Output High, $V_{OUT}=0V$, Typical	-55		mA
I_{OLS}^1	Output LOW Peak Current	Output Low, $V_{OUT}=V_{CC}$, Typical	55		mA
I_{CC}	Supply Current	TTL Outputs to 20 pF @ 50 MHz		210	mA
POWER	Power Dissipation	TTL Outputs to 20 pF @ 50 MHz		1.1	mW

1. Maximum test duration one second.
2. All DC parameters are tested or guaranteed by characterization.

The S4503 TTL outputs feature source series termination of approximately 40 Ohms to assist in matching 50–75 ohm P.C. board environments.

DC Characteristics

The S4503 has been designed specifically for clock distribution. In the development of this product, AMCC has made several modifications to the historic “high drive, totem pole outputs” producing AMCC’s dynamically adjusting source series terminated outputs. As a result of this, the S4503 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	$I_{OH} = -8$ mA	2.4V	
V_{OL}	$I_{OL} = 4$ mA		0.6V

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

The S4503 synthesizer employs a phase locked loop (PLL) which includes a "multiplying" counter to produce a high frequency internal reference oscillator from a low cost, low frequency crystal. This high frequency internal reference is the output of a voltage controlled oscillator or VCO. This single VCO frequency is sub divided down to selectable TTL output frequencies. One positive (+5V) referenced complementary ECL (PECL) output (Pout) pair is also provided.

The M counter is a frequency "multiplying" feedback counter that divides down the VCO frequency, before applying it to the phase detector. Thus the VCO frequency is the product of the input reference (crystal) frequency and the M counter modulus. This divide down counter modulus is externally selected to any integer value from 2 to 32 by a five bit binary coded value, plus 1, entered into input latches via the preset input pins M0 through M4. The M0 to M4 inputs have the binary weight of $M0=2^0$ through $M4=2^4$. The M0-4 inputs are low or 0 if not connected. NOTE: an entry of all binary zeros will not count down and is, therefore, invalid. Designs that will load the M counter inputs from an external register that powers-up with the outputs in a hi-Z state will need to use external resistors to ensure the S4503 M counter inputs are never all zeros.

The output frequency divide down counters "P & T" each have individual select input pins which may be actively driven by CMOS/TTL outputs or strapped to +Vcc (as a 1) or non-connected as appropriate. Non-connected inputs are biased low or 0. When the binary coded value of zero is entered into these counter preselect inputs, their outputs are disabled, thereby saving AC output power. Output symmetry is very close to 50% duty cycle with both odd and even division modulus due to an odd division correction employed at the counter's output. Refer to the counter preset tables for the binary coded preselect input values to division modulus.

The TTL output drivers of the T counter are source series terminated by internal resistors of ~40 Ohms to avoid the need for external termination. This series termination was chosen to match 50 to 75 Ohm transmission line traces into end of line load capacitance of ~20 pF. Refer also to the AMCC Clock Driver Application Note #1. The complementary PECL output emitter followers can source 25 mA from +Vcc and should be externally terminated at the end of the

transmission line into an equivalent 50 Ohm resistance to +Vcc - 2V.

The analog VCO circuitry requires some external passive loop filter components mounted very close to the required S4503 package pins. A VCO frequency centering resistor, RFcenter, is connected between KVCO and +VCCA, the analog +5V. A frequency span resistor, Rspan, is connected between pins REXT1 and REXT2. A loop filter series resistor-capacitor pair, RCOMP & CCOMP is connected between pin Comp and analog ground GNDA. Note that the analog ground (GNDA) and +5V (+VCCA) are to be isolated (decoupled) from the noisier digital and output power leads VCC and GND.

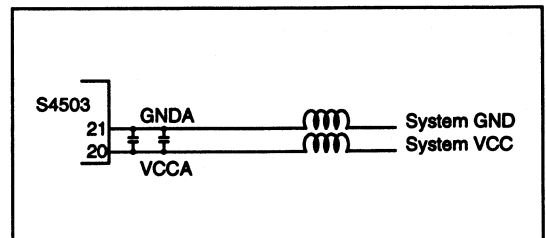
The input to the XTALIN pin will be a series resonant crystal of fundamental frequency from 5 to 25 Mhz. The external addition of series or shunt capacitance to "pull" the frequency is up to the user's discretion. An external series resistor may be required to limit the drive current from the XTALOUT pin with low ESR crystals.

When the XTALIN pin is driven by an external TTL clock source, the XTALOUT pin is not connected and the peak TTL amplitude should not exceed 3 volts. TTL output signals should be in the range of 5-80 MHz.

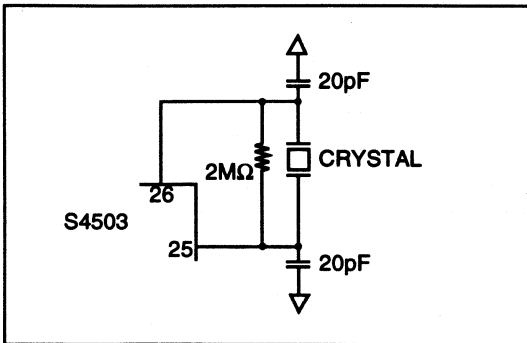
BOARD LAYOUT CONSIDERATIONS

To minimize the impact of board noise on the operation of the S4503, the following guidelines should be followed.

- The analog VCCA and GNDA need to be isolated from the digital supplies. This can be accomplished by creating small analog power and ground planes next to the S4503 under the filter and VCO components. These analog planes can be connected to the digital planes through wire jumpers, small inductors (5-100 uH), or ferrite beads. If the digital supply noise is too large (>100mV), the inductors or ferrite beads will be necessary.



- Decoupling capacitors of 0.1 and 0.01 uF are needed. Three pairs should be placed as close to the S4503 power and ground pins as possible. One pair should be used to decouple the analog VCC and GND, while the others are for the digital supplies. The V_{tt} supply will also need to be decoupled using 0.1 and 0.01 uF capacitors. These components should be surface mounted chip capacitors, to reduce the parasitic inductance.
- No dynamic signal lines should pass through or beneath the filter circuitry area, to avoid the possibility of noise due to crosstalk.
- The crystal oscillator will need to have a 2 M ohm shunt resistor connected between the terminals of the external crystal, and two 20 pF capacitors connected from each pin of the crystal to VCC (or GND). These components are necessary to ensure the oscillator will operate at the correct frequency.



- The loop filter and VCO components must be surface mounted to reduce the parasitic inductance, and the components are connected to the analog power and ground planes, rather than the digital planes.

FILTER AND VCO COMPONENT SELECTION

The S4503 is designed to operate over a wide range of VCO frequencies. Because of this, it is necessary to modify the values of Rspan and Rfcenter in order to get the best performance at a given frequency.

When operating the S4503 with the VCO in the 150–225 MHz region, the values for the VCO components are:

Rspan = 470 Ohms, Rfcenter = 390 Ohms

When operation the S4503 with the VCO in to 225–300 Mhz, the values for the VCO components are:

Rspan = 390 Ohms, Rfcenter = 820 Ohms

The loop filter components, Rcomp and Ccomp, do not change values at different frequencies. The correct values for these components are:

Rcomp = 2.7K Ohms, Ccomp = 0.1uF

All of the resistor values are 5% and 1/8 watt.

Power Management

The overall goal of managing the power dissipated by the S4503 is to limit its junction (die) temperature to 130°C. A major component of the power dissipated internally by the S4503 is determined by the load that each TTL output drives and the frequency that each output is running. The following table summarizes these dependencies.

FREQUENCY	C _{LOAD} =5pF	C _{LOAD} =10pF	C _{LOAD} =15pF	C _{LOAD} =25pF	C _{LOAD} =40pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	132 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	65 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	60 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The above output power must then be added to the core power (700 mW) of the S4503 to determine the total power being dissipated by the S4503. This total power is then multiplied by the S4503's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the S4503. For greatest reliability this junction temperature should not exceed 130°C. The thermal resistance for the S4503 soldered to a multi-layer PCB is as follows:

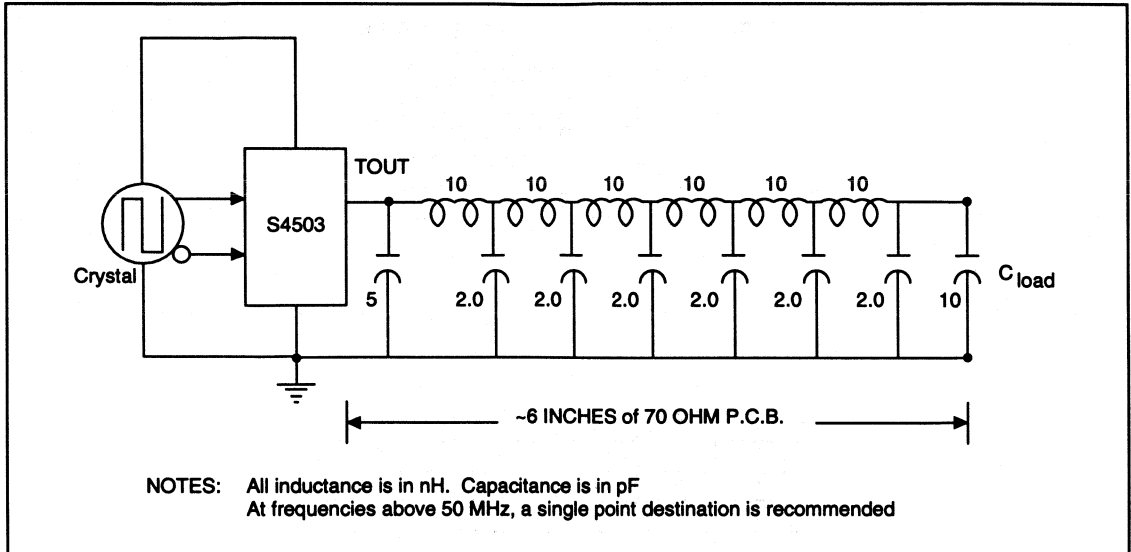
	Still Air	100 Lin Ft/Min	200 Lin Ft/Min
Thermal Resistance	50°C/Watt	45°C/Watt	40°C/Watt

Designing the S4503 for "Real Loads"

The S4503 is designed to provide clean clock transitions when presented with a realistic load. The assumptions are that the S4503 will be driving a selected length(s) of 70 Ohm (Z₀) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading can cause overall impedance to drop to under 60 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with capacitive loads ranging up to 20 pF at frequencies up to 80 MHz. Higher capacitive loads (greater than 25 pF) at high frequencies (greater than 50 MHz) may require the like output drivers to be strapped in parallel.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented on the following page. This is a mid-point model and can be modified to reflect a specific end use. More details concerning this are presented in the Application Note.

Evaluation Circuit



S4503 M- Counter Division Table

M0	M1	M2	M3	M4	MODULUS
0	0	0	0	0	INVALID
1	0	0	0	0	2
0	1	0	0	0	3
1	1	0	0	0	4
0	0	1	0	0	5
1	0	1	0	0	6
0	1	1	0	0	7
1	1	1	0	0	8
0	0	0	1	0	9
1	0	0	1	0	10
0	1	0	1	0	11
1	1	0	1	0	12
0	0	1	1	0	13
1	0	1	1	0	14
0	1	1	1	0	15
1	1	1	1	0	16

M0	M1	M2	M3	M4	MODULUS
0	0	0	0	1	17
1	0	0	0	1	18
0	1	0	0	1	19
1	1	0	0	1	20
0	0	1	0	1	21
1	0	1	0	1	22
0	1	1	0	1	23
1	1	1	0	1	24
0	0	0	1	1	25
1	0	0	1	1	26
0	1	0	1	1	27
1	1	0	1	1	28
0	0	1	1	1	29
1	0	1	1	1	30
0	1	1	1	1	31
1	1	1	1	1	32

[Where: $M(0:4) + 1 = \text{MODULUS}$ and $M0 = 2^0, M1 = 2^1, M2 = 2^2, M3 = 2^3, M4 = 2^4$]

S4503 Output Counter Division Table

P0	P1	P-MODULUS
0	0	DISABLED
1	0	1
0	1	2
1	1	4

T0	T1	T2	T3	T-1 MODULUS
0	0	0	0	DISABLED
1	0	0	0	2
0	1	0	0	3
1	1	0	0	4
0	0	1	0	5
1	0	1	0	6
0	1	1	0	7
1	1	1	0	8
0	0	0	1	9
1	0	0	1	10
0	1	0	1	11
1	1	0	1	12
0	0	1	1	13
1	0	1	1	14
0	1	1	1	15
1	1	1	1	16

Where $T1(0:3) + 1 = \text{MODULUS}$ and

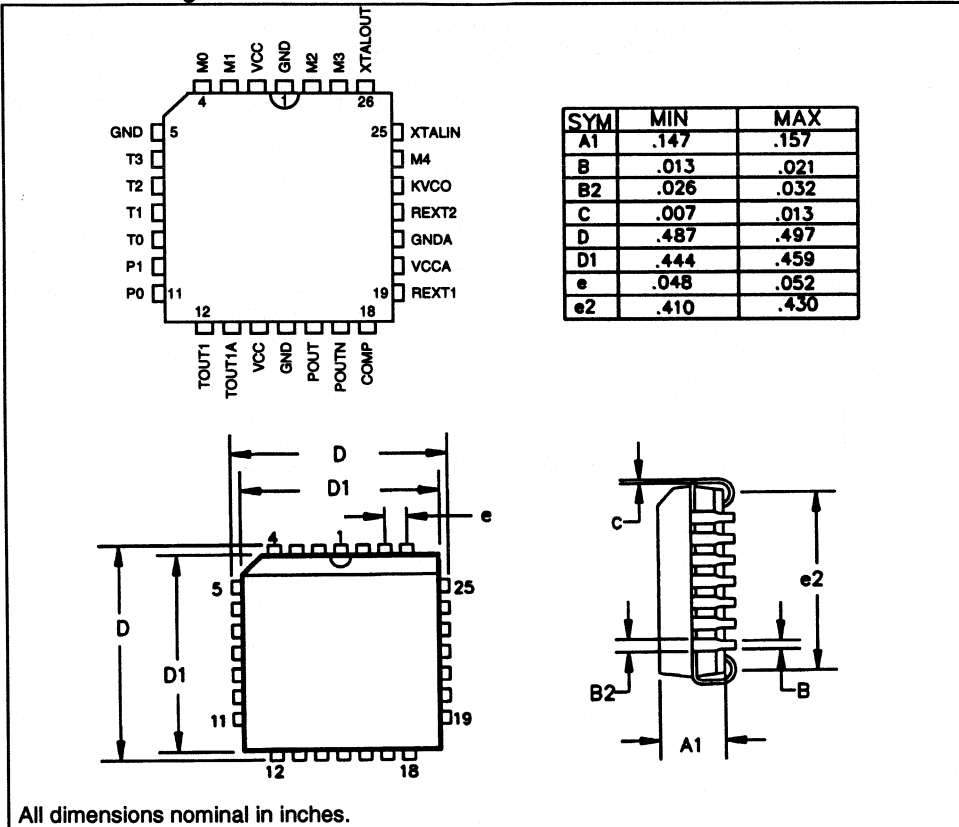
$$T0 = 2^0$$

$$T1 = 2^1$$

$$T2 = 2^2$$

$$T3 = 2^3$$

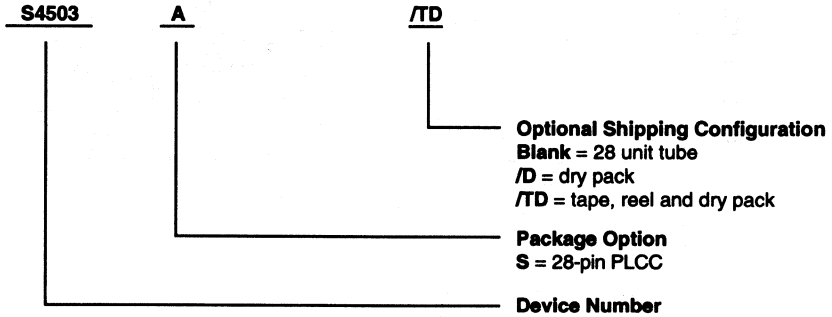
28 PLCC Package and Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Optional Shipping Configuration**



Example: S4503A/D
28-pin PLCC package, shipped dry packed in the standard tube.

FEATURES

- Provides two Rambus compatible clock outputs from 240 to 270 MHz
- Uses low cost 14.318 MHz crystal as reference for 267 MHz output
- Low Jitter, <150 ps
- Output skew <100ps
- 45/55% duty cycle
- On-chip filter requires no external components
- Eight-pin, .150" SOIC
- Operates from a single 3.3V ±10% supply
- Input crystal requires no external components

APPLICATIONS—RDRAM BASED

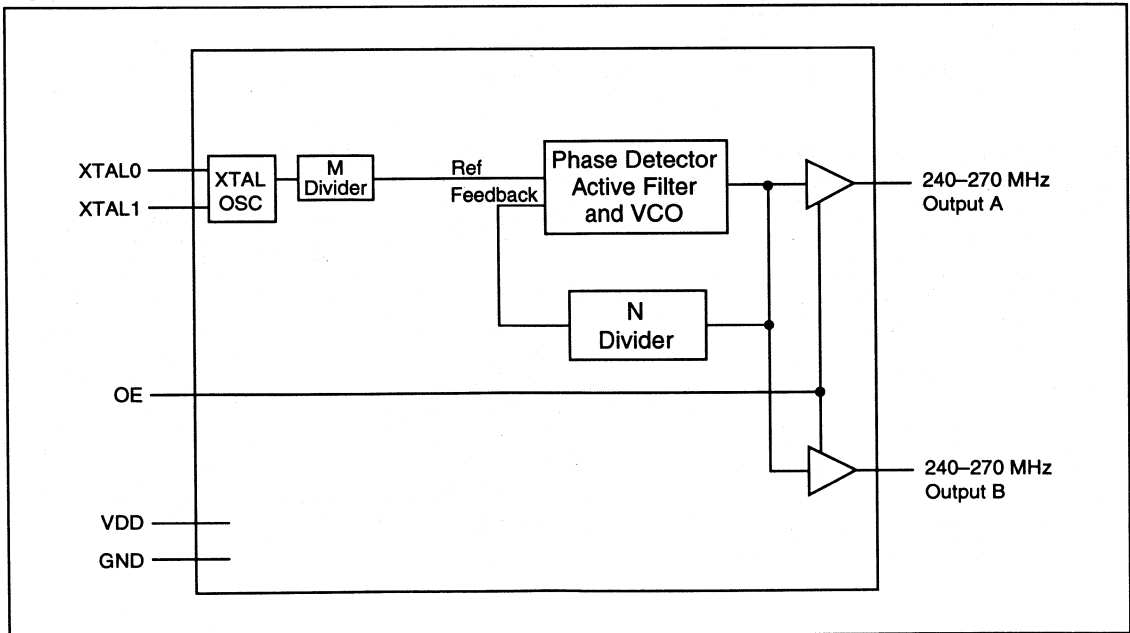
- Graphics Accelerators
- PC Memory
- Set-Top Boxes
- Games

DESCRIPTION

AMCC's advanced PLL technology allows the S4505S to provide two Rambus-compatible, 267 MHz clocks from a low cost 14.318 MHz crystal. Other reference crystals can be used to produce other output frequencies within the 240–270 MHz range. An external series resistor allows the output to be matched to the Rambus transmission line impedance needed for each application.

AMCC utilizes its high speed, low-jitter PLL technology developed for telecom and precision clocking applications to provide outputs which meet the low jitter and symmetrical duty cycle requirements of RAMBUS system clocks.

Figure 1. Block Diagram



Absolute Maximum Ratings

Parameter	Description	Value	Unit
V _{DD}	Power supply vs. GND	-0.5 to +5.0	V
V _{IN}	Input voltage, and pin vs. GND	-0.5 to V _{DD} +0.5	V
Storage Temp.	Maximum temperature during storage	170°	°C

Note: Stresses greater than the absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Specifications (T_A = 0°C – 70°C, V_{DD} = 3.3 ± 0.3V)

Parameter	Description	Conditions	Min	Max	Unit
V _{IH}	Input HIGH voltage	OE Pin	2.0		V
V _{IL}	Input LOW voltage	OE Pin		0.8	V
I _{IH}	Input HIGH current	OE Pin		50	uA
I _{IL}	Input LOW current	OE Pin – Internal pull-up		300	uA
P _D	Power Dissipation	Dynamic		350	mW

Output Characteristics

All specifications are compatible with Rambus requirements.

Symbol	Description	Comments	Min	Typ	Max	Unit
Z ₀	Line impedance	Rambus compatible	25		50	Ω
V _{TERM}	Line termination voltage	Rambus compatible	2.45		2.9	V
V _T	Switching threshold voltage	Rambus compatible	1.9		2.4	V
V _S	Output voltage swing	Rambus compatible	1.1		1.6	V

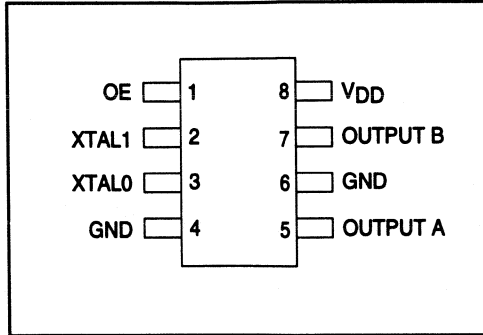
AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

All specifications are compatible with Rambus requirements.

Symbol	Description	Test Condition	Min	Typ	Max	Unit
F _{XTAL}	Crystal frequency		12.86	14.318	14.46	MHz
F _{OUT}	Output frequency	Typ with 14.318 MHz input ¹	240	267	270	MHz
F _{ACC}	Frequency accuracy	Using 50 ppm crystal	-1500		+500	PPM
T _R , T _F	Output clock rise/fall time	20% to 80%	0.2		0.5	ns
T _{DC}	Duty cycle	STD Rambus System Load	45	50	55	%
T _{JPP}	Jitter, peak-to-peak			50	150	ps
T _{PU}	Power-up time	From OFF to clocks stable			10	ms
T _{SKEW}	Output A to B skew	Equal loads			100	ps

1. Output frequency multiplier is 56/3 times the input crystal frequency.

S4505S Pinout — 8-Pin SOIC



Pin Descriptions

Pin #	Description
1	Output enable, Active HIGH, Internal pull-up
2	Crystal connection, nominally 14.318 MHz for 267 MHz output
3	Crystal connection — Series Resonant
4, 6	Ground
5, 7	Output A, B — 240–270 MHz clock outputs, open drain — should be terminated externally to match Rambus specifications
8	Power — 3.3V ± 10%

INTRODUCTION

As today's personal computers (PC) and systems push into the 50Mhz realm and beyond, the minimization of system clock skew becomes more important. Clock skew eats into the effective clock period that is available to perform other tasks. Using generic driver chips and careful board layout, current systems can achieve about 4ns of system clock skew. A 4ns clock skew at 25Mhz is 10% of the clock period, while at 66Mhz this same 4ns skew eats up 26% of the system clock period. At 50Mhz and higher, the allowable clock skew is approximately 2ns-3ns. Clearly this requires a new method of clock generation and distribution.

The key to the reduction of clock skew lies in the development of PLL clock generators, low skew clock drivers, and understanding how to distribute and route the clock signals.

The S4402/S4403 use AMCC's 1.0 micron BiCMOS technology to generate 10-80Mhz multiphase TTL clocks with less than +/-200ps of skew. The S4402 offers 6 output drivers, four at the primary output frequency, one at two times the primary frequency, and one at half the primary frequency. The S4403 offers 10 output drivers: four pairs at the primary

output frequency, one at twice the primary frequency, and one at half the primary frequency.

The phase relationships between the outputs are programmable. Four different output configurations are available to provide synchronous outputs, quadrature phase delay outputs, minimum phase delay outputs, and a mixture of minimum and quadrature phase delay outputs.

The times-two output and the half frequency output, allow the S4402/03 to multiply and divide the reference clock input for distribution to the system clock loads. This feature is very useful to eliminate the EMI problems of distributing high frequency clocks across the entire system.

PLL CLOCK GENERATOR OVERVIEW

The basic concepts of phase-locked loops are fairly simple. The diagram in Figure 1 shows the fundamental blocks of the S4402/03 PLL. The task of the PLL is to minimize the frequency and phase differences between the reference clock input (REFCLK) and the feedback clock input (FBCLK). In this case, the PLL clock generator can be considered a "zero delay" clock buffer.

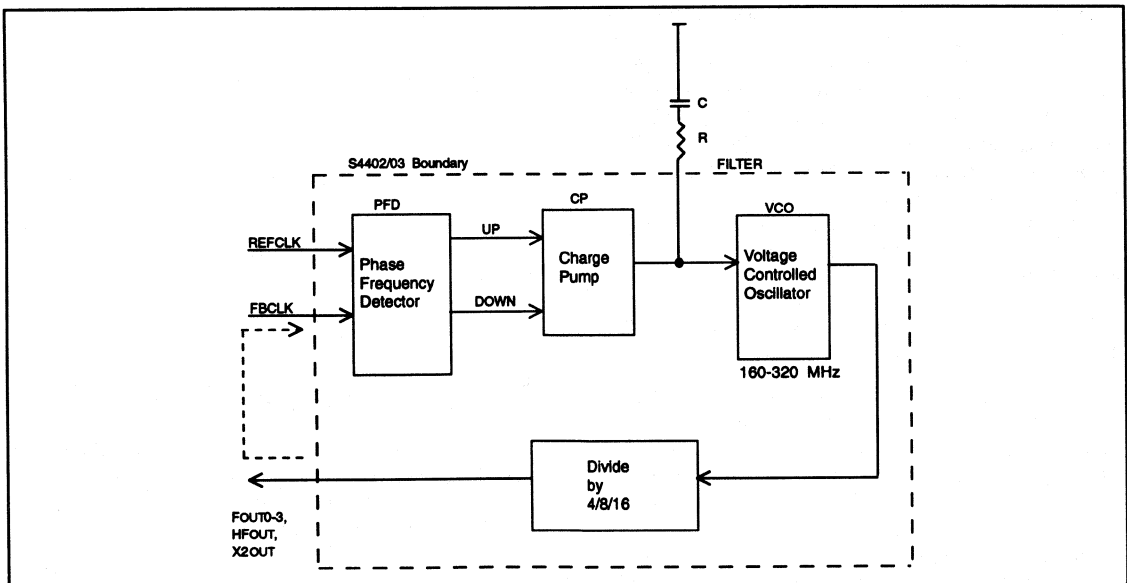


Figure 1 – Phase-Locked Loop of S4402/03

The Phase Frequency Detector (PFD) compares the reference and feedback clocks and provides a signal to the Charge Pump (CP) that tells the charge pump to increase or decrease the voltage into the Voltage Controlled Oscillator (VCO). This in turn increases or decreases the oscillator frequency, thereby changing the frequency or phase of the feedback clock.

The CP converts the digital signals from the PFD into a change in voltage at the external filter pin. This change in voltage is supplied to the VCO input. The CP can provide very small changes in the VCO control voltage that will modify the phase of the VCO output, or it can provide larger changes in the control voltage to change the VCO frequency.

The VCO simply responds to the control voltage at its input and generates an output clock frequency which is proportional to the voltage at its input. This high frequency clock signal goes into the internal logic of the S4402/03 and is divided by four, eight, or sixteen before appearing at the various chip outputs.

By selecting one of the S4402/03 outputs as the feedback clock, the loop is closed, and the internal PLL will try to make the rising edge of the output connected to the feedback input line up with the rising edge of the reference clock input. Due to the closed loop nature of this action, delays between the reference clock output and the subsequent arrival of the feedback clock input can occur without causing the chip to lose lock. Therefore, an external buffer can be introduced into the loop, and an output from the buffer fed back to the feedback input. This provides a simple means of increasing the output drive capability of the S4402. Another option is to introduce an external counter into the loop, and connect an output from the counter into the feedback input. This allows the S4402/03 to accept a lower reference clock frequency.

The two most important specifications for PLL clock generators are phase error and output skew.

Phase error is defined as the delay between the reference input and the feedback input when the chip is locked. When an output is used to drive the feedback input, the phase error can also be specified as a propagation delay. The S4402/03 clock generators have a maximum phase error (across all temperatures, supply voltages, and frequencies) of 1.0ns. On a given chip there will be less than 1.0ns of delay between the REFCLK input and the FBCLK input. Furthermore, at a given frequency, temperature, and

supply voltage, the maximum variation in phase error across all parts is less than 750ps. Plus, at a given frequency, the maximum variation in phase error across all parts, is less than 1.25ns, over any temperature and supply voltage difference. These are important specifications in determining total system clock skew.

Output skew is defined as the delay between synchronous outputs. The S4402/03 clock generators have a maximum output skew of +/- 200ps. This means that with equal loading, all the rising outputs will switch within 400ps of each other.

CLOCK DISTRIBUTION ON A BOARD

The first few system clock skew examples are based upon the idea that all the clock loads are located within a single board.

The simplest configurations are that of a single S4402/03 or of multiple S4402/03s in parallel being driven from a single reference source. In Figure 2 the clock generators C1 and C2 are driven from the same crystal oscillator output. The clock skew associated with a single clock generator, such as C1 by itself, is simply the output skew specification of 400ps (+/- 200ps max).

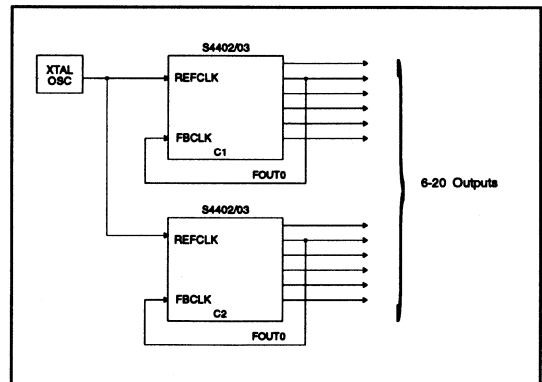


Figure 2 – Clock Distribution on a Board

In the case where the output from the crystal oscillator drives no additional chips on the board, except the clock generators, the total clock skew across all the S4402/03s can be calculated as:

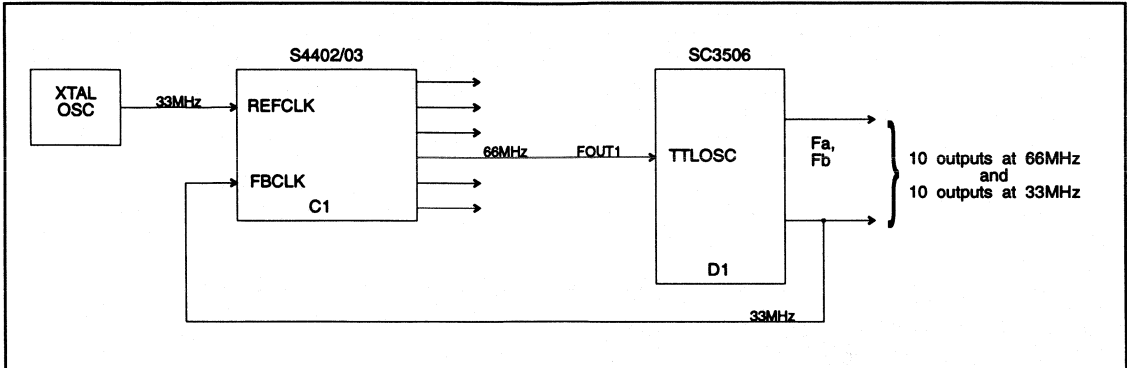


Figure 3 – Clock Distribution on a Board: S4402 with an SC3506

$$\begin{aligned} \text{Total skew} &= T_{pev} + T_{skew} \\ &= 750ps + 400ps \\ \text{Total skew} &= 1.150ns \text{ (max.)} \end{aligned}$$

where,

$$\begin{aligned} T_{pev} &= \text{the maximum variation in phase error across all parts at a given frequency, temperature and supply voltage.} \\ T_{skew} &= \text{the maximum output skew on any part.} \end{aligned}$$

In this first example, the total clock skew across C1 and C2 depends upon the phase error and the output skew of each chip. Rather than use the total range of phase error for all possible frequencies,

temperatures, and supply voltages, this configuration allows the use of the chip to chip variation in phase error. This is possible because the clock generators will be placed close to the crystal oscillator, and therefore experience the same temperature and power supply environment.

The second example, in Figure 3, shows the use of an S4402 clock generator to multiply the 33MHz crystal oscillator output up to 66MHz before applying it to the input of the SC3506 clock driver. This is accomplished by feeding back one of the divide-by-two outputs of the SC3506 to the FBCLK input of the S4402/03. This configuration allows the use of a slower crystal oscillator to generate 10 outputs at 66MHz and 10 outputs at 33MHz.

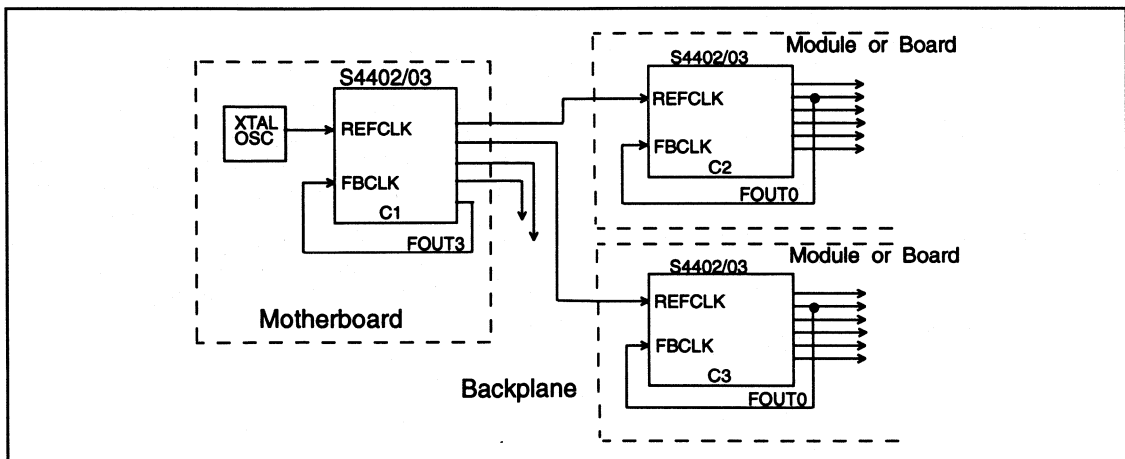


Figure 4 – Clock Distribution Between Boards

Because the output of the SC3506 is fed back to the FBCLK input of the S4402, the delay through the SC3506 is not important in the calculation of the total output clock skew. The total output clock skew is determined solely by the output skew specification of the SC3506, and is therefore, less than 500ps (max.) for the SC3506-1.

CLOCK DISTRIBUTION BETWEEN BOARDS

Most systems do not consist of a single board containing all the computing, memory, I/O, and display functions. A typical system configuration would likely have a central board that ties the system together (the motherboard), and a series of additional modules or expansion boards, that allow the user to update and upgrade the system.

Ideally, the master clock needs to be distributed to the synchronous logic on the motherboard, and each of the expansion boards, with no skew.

Figure 4 shows a configuration using an S4402/03 to distribute the master clock to the motherboard and the expansion boards. On each board or module, the master clock copy is received by another S4402/03, and distributed to the rest of the board.

The maximum clock skew between the motherboard clocks (outputs of C1) and the module clocks (outputs of C2 and C3) can be calculated as:

$$\begin{aligned} \text{C1-to-C2 skew} &= \text{Tskew(C1)} \\ &\quad + \text{Tpmax(C2)} \\ &\quad + \text{Tskew(C2)} \\ &= 400\text{ps} \\ &\quad + 1.0\text{ns} \\ &\quad + 400\text{ps} \end{aligned}$$

$$\text{C1-to-C2 skew} = 1.80\text{ns (max.)},$$

where,

$$\text{Tpmax(C2)} = \text{the maximum absolute value of phase error for C2.}$$

$$\text{Tskew(C1 or C2)} = \text{the maximum output skew for each chip.}$$

The total system skew will be determined by the maximum skew across all the modules. This total system skew can be calculated, using the results of the C1-to-C2 skew calculation, as:

$$\begin{aligned} \text{Total skew} &= \text{C1-to-C2skew(max.)} \\ &\quad - \text{C1-to-C3skew(max.)} \\ &= 1.80\text{ns} \\ &\quad - \text{C1-to-C3skew(max.)} \end{aligned}$$

$$\begin{aligned} \text{C1-to-C3skew} &= \text{Tpevfmin(C3)} \\ &\quad + \text{Tskew(C3)} \\ &= [\text{Tpmax(C3)} - \text{Tpevf}] \\ &\quad + \text{Tskew(C3)} \\ &= [1.0\text{ns} - 1.25\text{ns}] \\ &\quad + -400\text{ps} \end{aligned}$$

$$\text{C1-to-C3skew} = -650\text{ps (max.)}$$

$$\text{Total skew} = 1.80\text{ns} - [-650\text{ps}]$$

$$\text{Total skew} = 2.45\text{ns (max.)}$$

where,

$$\text{Tpevf} = \text{the maximum chip to chip variation in phase error at a given frequency, across all temperatures and supply voltages.}$$

$$\text{Tpevfmin(C3)} = \text{the most negative phase error of C3 versus C2, based upon a Tpevf variation between C2 and C3.}$$

In this calculation, the objective is to determine the widest variation in output skew between the C2 and C3 clock generators. The calculations make use of the fact that at a given frequency, but with unequal temperatures and supply voltages, the maximum variation in phase error between any two parts is less than 1.25ns. This specification is used to make the maximum skew variation of C3 versus C1 be -650ps, when the maximum skew variation of C2 versus C1 is 1.80ns. With this, the maximum size of the output switching window around C1 is equal to 2.45ns.

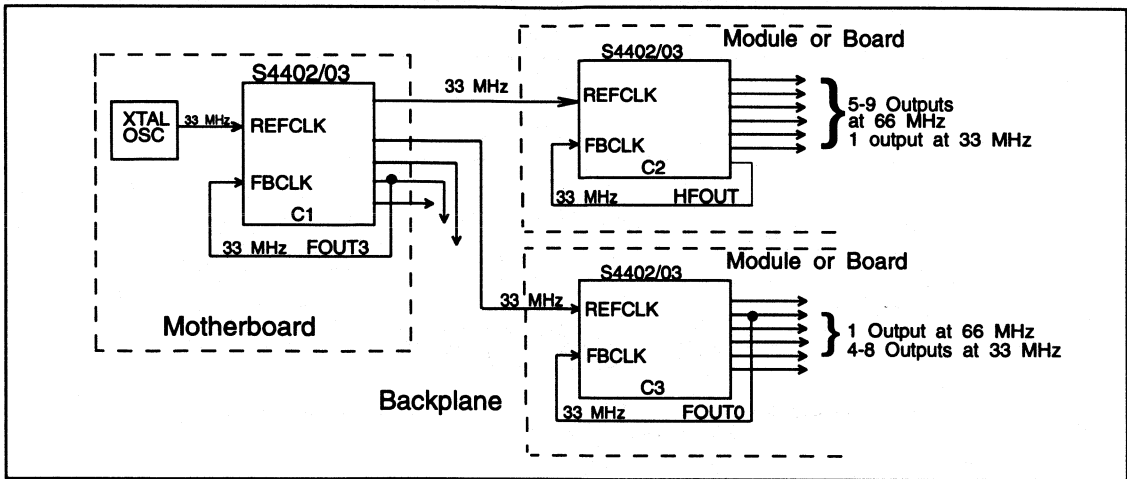


Figure 5 – Clock Dividing and Multiplication for Distribution Between Boards

Figure 5 shows the use of the S4402/03 as a clock multiplier and divider in a board to board clock distribution scheme. In this example, the motherboard clock generator, C1, is used to distribute multiple copies of the crystal oscillator frequency of 33MHz. These 33MHz outputs are routed point to point down the backplane to each of the expansion boards or modules. In this manner, it is possible to route slower frequency outputs on the backplane, and reduce the crosstalk, signal noise, and EMI problems.

The S4402/03 chip on each module can be programmed to multiply the 33MHz backplane clock signal to its previous 66MHz value, or it can create a set of 33MHz clock outputs. With this technique, each module or board can be selectively operated at the crystal oscillator frequency, 2X that frequency, or 1/2 the oscillator frequency.

In this application, the total system clock skew is also 2.45ns. The calculation of system clock skew in this example is the same as that for the previous example.

Figure 6 shows a special application of the S4402/03. In this application, data is to be synchronously transferred between boards in the system. The difficulty arises from the fact that in a system, the data delay from one board to the next varies depending upon location. This delay uncertainty, and the total system clock skew, combine to make the job of providing sufficient hold time, at the input register on each board, a difficult task.

For this example, assume the system reference clock on each board is generated by an S4402/03 that is located in a central location, typically the motherboard. From a previous example (Figure 5), this gives a total system clock skew of 2.45ns.

Based upon this 2.45ns clock skew, a scenario can be drawn in which the data that is clocked out from one board reaches its neighbor before the neighboring card has stored the previous data into the input register with sufficient hold time. A solution to this problem is to delay the time at which data is clocked out of all the boards.

In this solution, the data is clocked into each input register, on a clock edge that is synchronous with the system reference clock. A short time later (3–6ns), new data is clocked out onto the backplane data bus. This will provide sufficient hold time at each board, provided that the delay between the two register clocks is at least equal to the system clock skew plus the hold time of the input register.

The example in Figure 6 uses registers with a hold specification between 0.5ns and 1.3ns. Based on these values, the delay between the register clocks on each board must be at least 2.95ns to 3.75ns. In the minimum phase mode of operation, the S4402/03 can be configured to provide 3.75ns delays between output clocks at 33MHz, and is an ideal solution for this problem. FOUT0 is synchronous to the system reference clock, and is used to clock the input registers R1 and R3. FOUT1 is delayed from

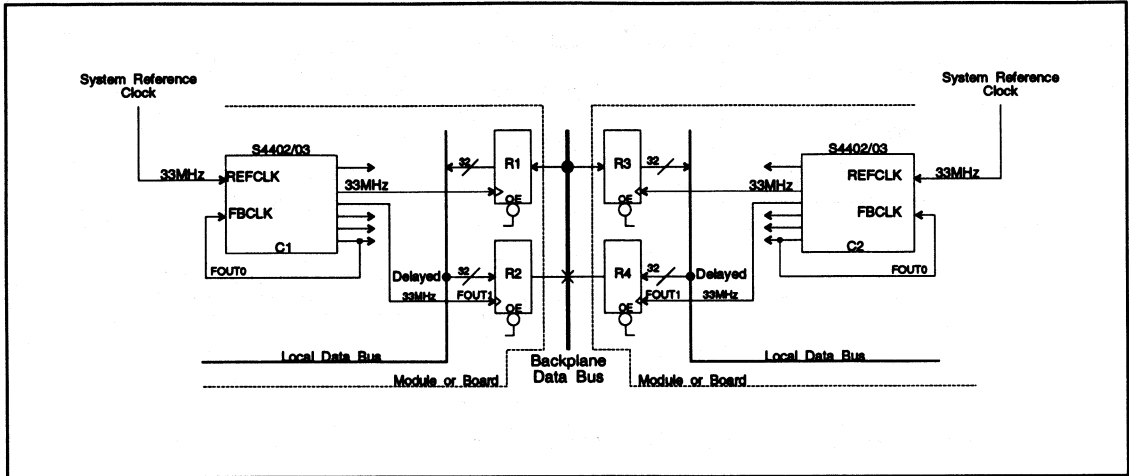


Figure 6 – Data Distribution Between Boards

FOUT0 by 3.75ns, and is used to clock the output registers R2 and R4. If additional delay is necessary, FOUT2 could replace FOUT1, and provide 7.5ns of delay between FOUT0 and FOUT2.

ASIC DESKEWING

In systems where there are multiple ASICs sharing a common synchronous bus, great care must be taken to ensure that data transfers on the bus can happen as rapidly as possible. Each ASIC must be simulated to ensure that its data setup, hold, and clock to data output times will work with each of the other chips. The designer must assume that each of the ASICs could be operating at any point on its performance curve; therefore, the propagation delays, setup, and hold times are increased to compensate for the variability of each of the ASICs. These increased specifications for each ASIC reduce the maximum attainable performance of the data bus by consuming a portion of the bus cycle time.

Figure 7 demonstrates a couple of ways to reduce the uncertainty of each ASIC's performance. In this figure, an S4402/03 is used to ensure that the output transitions of each ASIC occur synchronously to the system clock. If all the output transitions on the data bus occur at the same point in time, then the setup times for each ASIC can be minimized. With the clock to data output delays effectively reduced to zero, and the setup and hold times minimized, the available bus bandwidth is increased and data traffic can flow at a higher rate.

In the upper half, C1 takes a 25MHz master clock and generates a 50MHz clock for the ASIC A1. This 50MHz clock is buffered through the ASIC's internal clock buffer tree, before clocking a divide by two output flip flop. This 25MHz output clock is fed back to the S4402/03 chip and the rising edge of this signal is aligned to the rising edge of the 25MHz master clock.

In the lower half, C2 takes the 25MHz master clock and generates two 25MHz outputs that are in quadrature (90 degrees out of phase with each other). These 25MHz clocks are exclusive OR'ed inside the ASIC to create the 50MHz internal clock for

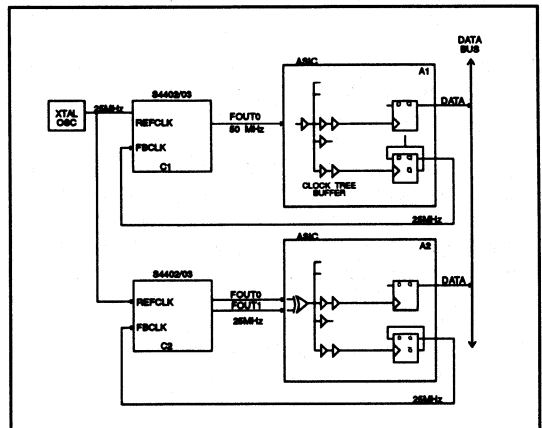


Figure 7 – ASIC Deskewing

the ASIC. This 50Mhz internal clock is again buffered in the same way as the rest of the ASIC clocks, and then divided by two at the output, and aligned with the 25Mhz master clock.

For these two schemes to work correctly, the designer must do three things. The ASIC internal clock buffering must be matched. In other words, the delay from the point at which the buffer tree begins to expand sideways, to the point at which the clocks arrive at the clock input to the output flip flops, must be equal. The output flip flop macros and the delay from the flip flop output to the external pins, must also be equal. And the interconnect length between the ASICs and the S4402/03s must be minimized and equal.

GENERAL GUIDELINES FOR CLOCK DISTRIBUTION

For all of the examples described previously, there are a number of general design guidelines that need to be applied in order to achieve the best performance. These guidelines are:

1. Clock traces need to have equal lengths and impedance.
2. The clock traces must be treated as transmission lines, and therefore use controlled impedance traces.
3. The clock signal termination strategy must be decided early. Series termination will reduce

the termination power requirement, but the loads must be clustered at the end of the clock line (<2" stubs).

4. Clock signal capacitive loads must be equal.
5. Do not heavily load the clock output drivers. With heavy loads, two outputs can be paralleled to increase the drive capability.
6. Clocks distributed across backplanes should be point to point connections. This will remove the transit time skew introduced as the signal propagates down the backplane past each board.
7. Be generous with decoupling capacitors. Each power and ground pin of the generators and drivers should be decoupled with 0.1uF ceramic chip capacitors.

SUMMARY

As shown, with careful design of the clocking scheme for a synchronous system, and the correct choice of clock generators and drivers, it is possible to reduce the system clock skew down to 0.4ns to 2.45ns.

The S4402/03 clock generator chips provide the user with the option to tackle the clock distribution problem in many different ways. The controlled output skew of less than 400ps, and the ability to generate clocks at frequencies up to 80Mhz, make the S4402 and S4403 the ideal choice for today's high performance systems.

FEATURES

- Generates outputs from 25 MHz to 80 MHz
- Four groups of three outputs (12 outputs total)
- Eight user-selectable output functions for each group
- Proprietary output drivers with:
 - Dual-sloped falling edge
 - On-chip source series termination
 - LVTTTL compatible outputs, with <1.5-ns edge rates
- Eliminates ground-bounce and undershoot problems encountered with Bipolar and CMOS drivers
- Performs clock doubling, dividing, invert, lead/lag placement
- Internal VCO running between 50 to 100 MHz
- On-chip loop filter
- Output skew less than 350 ps
- 52 PQFP package
- Operates from 3.3V VCC

APPLICATIONS

- High-performance microprocessor systems
- Compatible with Intel's Pentium™ processor

GENERAL DESCRIPTION

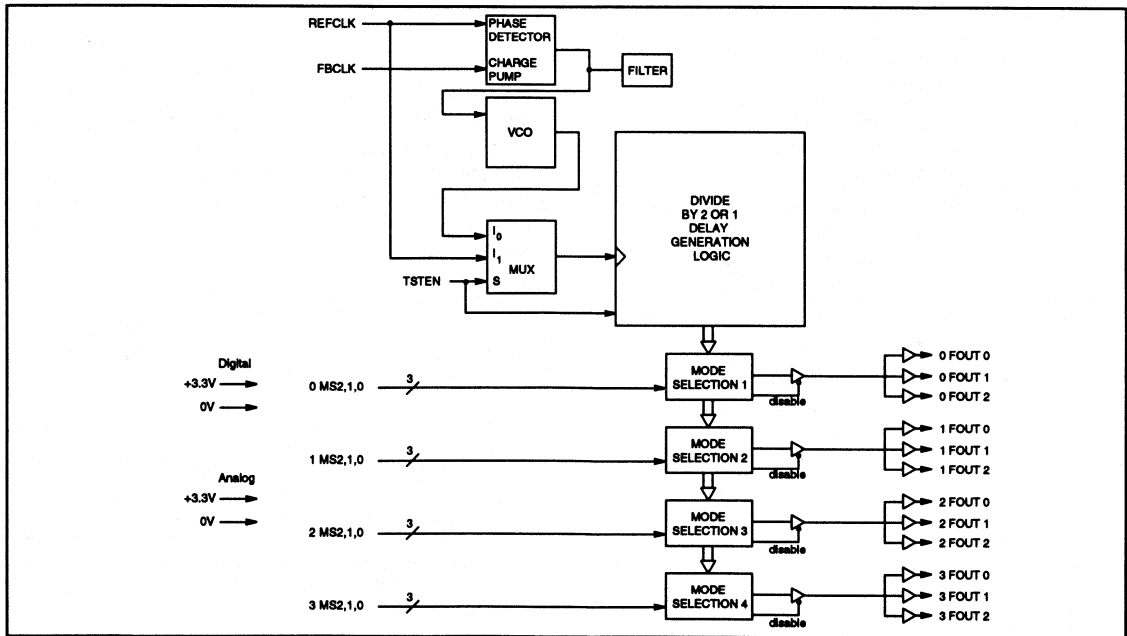
The S4LV406 BiCMOS clock generator provides 12 LVTTTL outputs with less than 350 ps of skew. Implemented in AMCC's 1.0μ BiCMOS technology, the internal PLL and divider/delay selector logic allow the user to individually tailor the (4) LVTTTL output groups to the system's needs. The internal VCO can operate between 50 to 100 MHz, and the programmability allows the user to generate output clocks in the 25–80 MHz range.

The S4LV406 offers the user the ability to select the appropriate phase and frequency relationship for each of the four groups of three LVTTTL clock outputs.

In addition to clock doubling and inversion functions, the S4LV406 allows any output groups to lead or lag the others by the minimum phase delay of 1.25–2.50 ns.

The S4LV406 uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide "source (series) termination" at the LVTTTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output-switching noise, distortion, and EMI.

Figure 1. S4LV406 Block Diagram



FUNCTIONAL DESCRIPTION

The 12 xFOUT0–2 outputs are the main LVTTL output clocks that the generator supplies. The mode selection choices are shown in Table 1 and waveform definitions are given in Figure 2. The “x” represents the output group number (1–4). The frequency of these outputs is determined by the REFCLK clock frequency and the output clock that is tied to the FBCLK input (xFOUT0–2 can be equal to REFCLK, half of REFCLK, or twice the frequency of REFCLK).

Example:

In order to meet bus timing specifications for a typical system, designers may need three outputs at 66 MHz for the system clock and processor, a 33-MHz output for the cache controller, and a 33-MHz delayed output for a memory management unit. This system requirement can be met using the S4LV406 by setting the mode select pins for the first group of outputs (0MS2,1,0) to 111, the second group (1MS2,1,0) to 110, and the third group (2MS2,1,0) to 101. In this

Table 1. Mode Selection Options

xMS2,1,0	MODE DESCRIPTION	xFOUT0,1,2
000	Disabled.	Logical Hi
001	All three outputs at the fundamental output frequency, but early by a minimum phase delay.	f – t
010	All three outputs at half the fundamental output frequency and inverted.	1/2
011	All three outputs at the fundamental output frequency and inverted.	1
100	All three outputs at half the fundamental output frequency, but delayed by a minimum phase delay.	f/2 + t
101	All three outputs at the fundamental output frequency, but delayed by a minimum phase delay.	f + t
110	All three outputs at half the fundamental output frequency.	f/2
111	All three outputs at the fundamental output frequency.	f

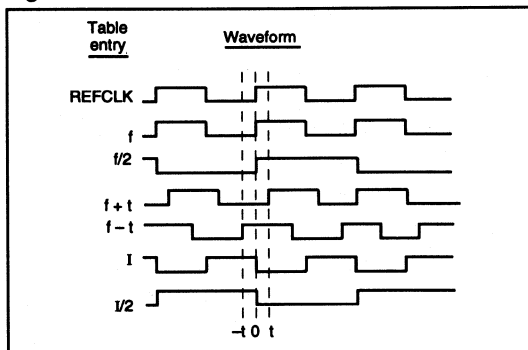
Note: If f is fed back, the fundamental frequency is equal to REFCLK.
If f/2 is fed back, the fundamental frequency is twice REFCLK.

configuration, one of the 33-MHz outputs should be fed back to the FBCLK input. This example makes use of only three of the four output banks, leaving the fourth available for any other clock signals needed.

Phase Delay

The minimum phase delay between xFOUT0–2 signals is a function of the VCO frequency. The VCO frequency is equal to the fundamental output frequency. The minimum phase delay is equal to the period of the VCO frequency divided by 8: $t = 1/(\text{VCO freq} \times 8)$. Since the VCO can operate in the 50-MHz to 100-MHz range, the range of minimum phase delay values is 1.25 ns to 2.50 ns (See Table 2).

Figure 2. Waveform Definitions



Test Capabilities

TESTEN allows the chip to use the REFCLK input instead of the VCO output to clock the chip. By-passing the VCO and using REFCLK makes the S4LV406 into a programmable clock buffer, however, the programmable mode choices are limited. The VCO is needed to create the inversion and minimum phase delay modes. So when TESTEN is active, the only options are XMS2,1,0 = 000,110, and 111, for each bank of outputs.

Table 2. VCO Operating Frequencies

xFOUT0–2	VCO FREQ	MIN PHASE DELAY
80 MHz	80 MHz	1.56 ns
66 MHz	66 MHz	1.89 ns
50 MHz or 100 MHz	50 MHz	2.50 ns or 1.25 ns*
33 MHz*	66 MHz	1.89 ns
25 MHz*	50 MHz	2.50 ns

* The bank containing the output used as feedback must be in one of the f/2 modes to ensure the VCO is operating within its 50-100 MHz range.

Power Supply Considerations

Power for the analog portion of the S4LV406 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 3). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100μH, and depends upon the frequency spectrum of the digital power supply noise. The ferrite beads should exhibit 75Ω impedance at 10 MHz.

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

Figure 3. External Power Supply Filter

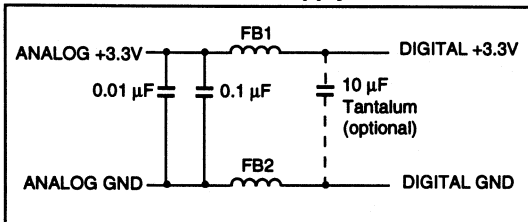
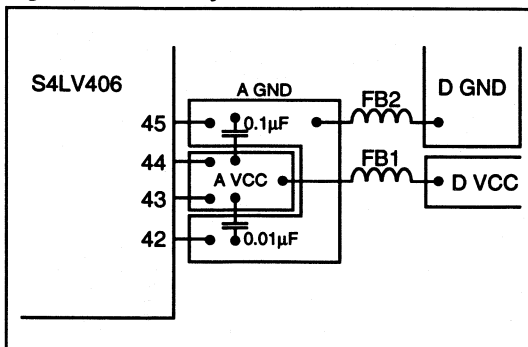


Figure 4. Board Layout



BOARD LAYOUT CONSIDERATIONS

- The S4LV406 chips are sensitive to noise on the Analog supplies. Care should be taken during board layout for optimum results.
- All decoupling capacitors (C1–C4 = 0.1 μF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4LV406 and the power and ground plane connections.
- The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip. The analog decoupling capacitors must be placed within 1/8 inch of the analog supply pins on the top surface of the board.
- The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

PIN DESCRIPTIONS

Input Signals

REFCLK. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the outputs. Also replaces the VCO output when TSTEN is high. See TSTEN.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the outputs. One output is selected to feed back to this input.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Also, when brought High, generates an internal Reset pulse that initializes the internal counter flip-flops to zero.

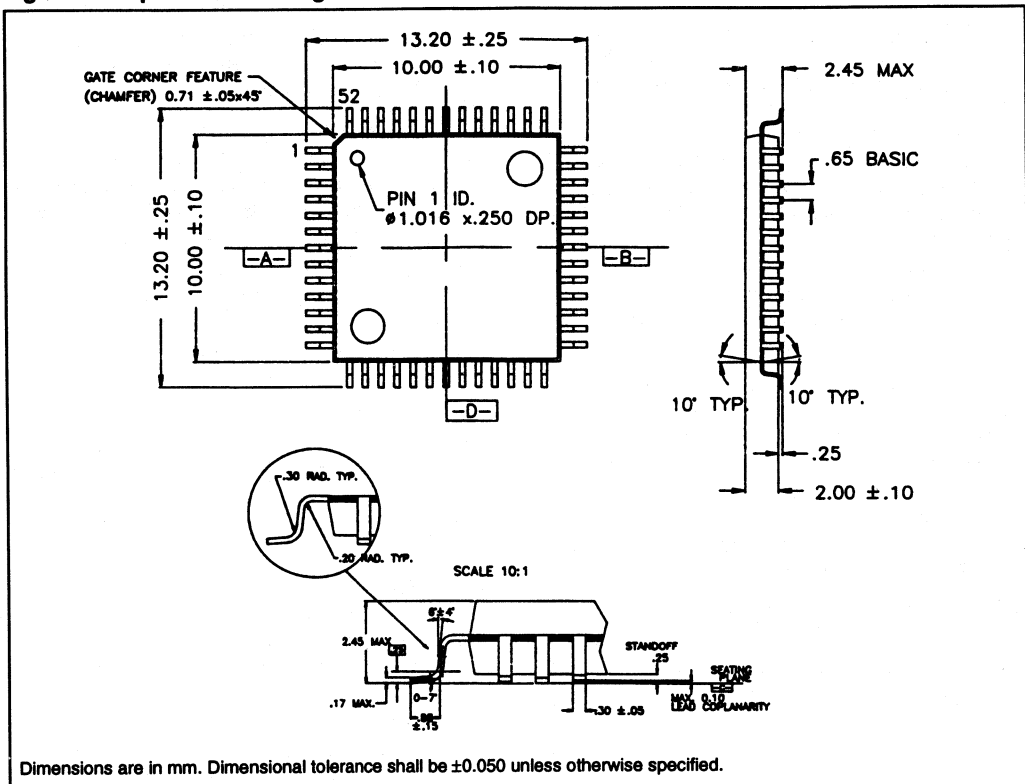
xMS2,1,0. Mode selection inputs that allow selection of the phase and frequency relationship of each of the four banks of three clock outputs. The “x” represents the output group number (0–3). Refer to Table 1 for mode selection options.

WTST. Active High. Used for AMCC test purposes only. Leave unconnected.

Output Signals

xFOUT0–2. Clock signal outputs. Refer to Table 1 and Figure 3 for a description of output options.

Figure 5. 52-pin PQFP Package



DC CHARACTERISTICS

Symbol	Parameter	DC Test Conditions	Min	Typ ¹	Max	Units
V_{IH}^2	Input HIGH Voltage	Guaranteed input HIGH voltage for all inputs	2.0			V
V_{IL}^2	Input LOW Voltage	Guaranteed input LOW voltage for all inputs			0.8	V
V_{IK}	Input clamp diode voltage	$V_{CC} = \text{Min}$, $I_{IN} = -18 \text{ mA}$		-0.8	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$, $I_{OH} = -2 \text{ mA}^3$	2.4		$V_{CC} + .3$	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$, $I_{OL} = 2 \text{ mA}^3$			0.4	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Min}$, $V_{IN} = 2.4 \text{ V}$			6	mA
					50	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Min}$, $V_{IN} = 0.5 \text{ V}$			1	mA
					-50	μA
I_{OS}^4	Output short circuit current	$V_{CC} = \text{Max}$, $V_{OUT} = 0 \text{ V}$	-55			mA
I_{CC}	Static	$V_{CC} = \text{Max}$			75	mA
I_{CCT}	Total I_{CC} (Dynamic and Static)	$C_{LOAD} = 10 \text{ pF}$ at 80 MHz			210	mA

1. Typical limits are at 25°C , $V_{CC} = 3.3 \text{ V}$.
2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher. Includes 100mV for on-chip series termination.
4. Maximum test duration one second.

ABSOLUTE MAXIMUM RATINGS

LVTTTL Supply Voltage VCC	-0.5V to 4.6V
LVTTTL Input Voltage	-0.5V to Vcc + 0.5V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 140°C
Storage Temperature	-55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Nom	Max	Units
LVTTTL Supply Voltage (VCC)	3.0	3.3	3.6	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	140	°C

Table 3. AC Specifications

Symbol	Description	Min	Max	Units
f_{VCO}	VCO Frequency	50	100	MHz
f_{REF}	REFCLK Frequency	25	80	MHz
t_{IRF}	Input Rise/Fall Time	1	3	ns
MPW_{REF}	REFCLK Minimum Pulse Width	5.0		ns
t_{PE}	Phase Error between REFCLK and FBCLK	-250	+250	ps
t_{PED}	Phase Error Difference from Part to Part ¹	0	300	ps
t_{SKEW}	Output Skew ² across all outputs	0	350	ps
t_{SKEWA}	Output Skew ² within any bank	0	250	ps
t_{DC}	Output Duty Cycle ³	45	55	%
f_{FOUT}	FOUT Frequency ⁴	25	80	MHz
t_{PS}	Nominal Phase Shift Increment ⁵	1.25	2.50	ns
t_j	Clock Stability ⁶		250	ps
t_{ORF}	FOUT Rise/Fall Time ⁷	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time ⁸		5	ms
t_{PSV}	Phase Shift Variation ⁵	-100	+100	ps

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. Outputs loaded with 10 pF, measured at 1.5 V.
4. $C_{LOAD} = 10$ pF.
5. All phase shift increments and variation are measured relative to 0FOUT0 at 1.5 V.
6. Clock period jitter with all FOUT outputs operating at 80MHz loaded with 10 pF. Parameter guaranteed, but not tested.
7. With 10 pF output loading (0.8 V to 2.0 V transition).
8. Depends on loop filter chosen. (Number given is for example filter.)

Figure 6. Timing Waveforms

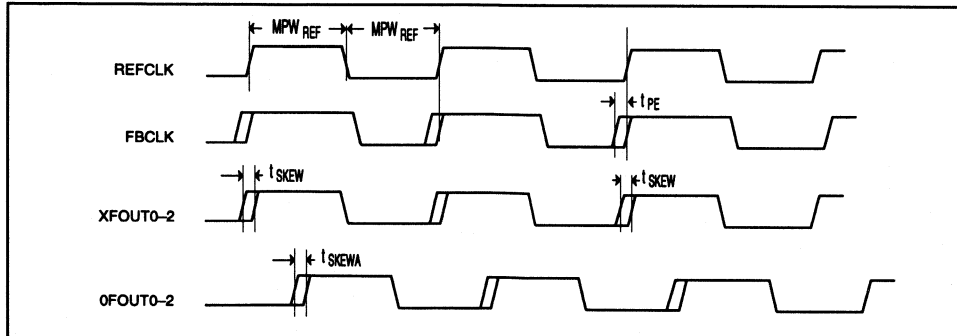
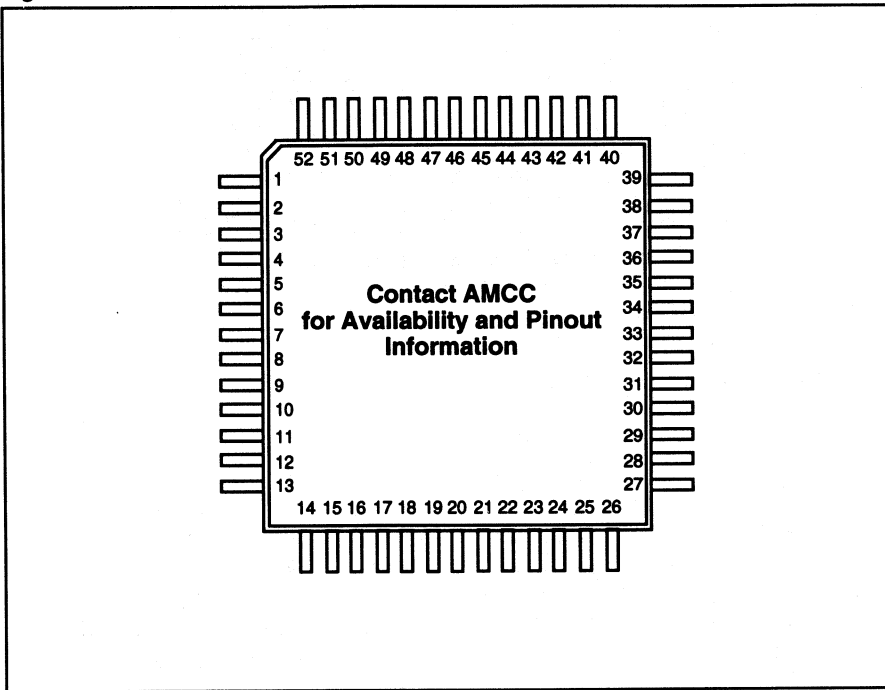


Figure 7. S4LV406 Pinout



Ordering Information

GRADE	PLL CLOCK GENERATOR	PACKAGE	MAX FREQ
S-Commercial	S4LV406	Q-52 PQFP	80

X
Grade

XXXX
Part number

X
Package

XX
Speed

CONTENTS

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Q20000 FEATURES

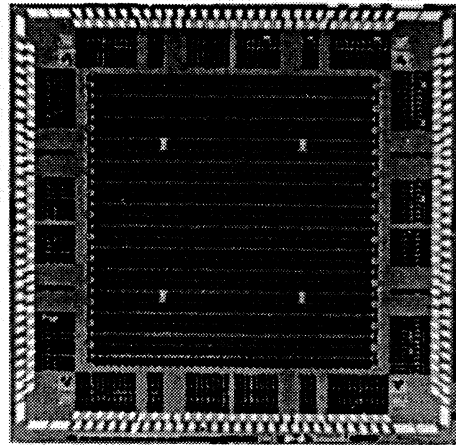
- Up to 18,700 gates, channelless architecture
- 100 ps equivalent gate delays
- Low power (.5-1.0 mW/gate)
- 10K, 10KH, 100K ECL and mixed ECL/TTL capability
- Structured arrays with 1.25 GHz PLLs*
- High precision programmable delay line macro
- Speed/power programmability
- Single cell 25 and 50 ohm parallel termination drive
- Symmetrical rise and fall times
- Operation over commercial and military ranges
- Up to 100% utilization

DESCRIPTION

The AMCC Q20000 Series of logic arrays is comprised of eight products ranging in density from 671 to 18,700 equivalent gates (full adder counting method) including structured arrays with 1.25 GHz PLLs.* The Turbo series is optimized to provide high performance and proven reliability to today's advanced hi-rel commercial and military semicustom applications.

Q20000 arrays are designed to operate at frequencies as high as 1.25 GHz. These Turbo arrays achieve this very high performance by combining an advanced one micron process with innovative A.C.-coupled active drive circuitry. The combination of this advanced process and patented circuit design technique has achieved operating performance efficiencies as much as eight times over previous bipolar families.

An extensive library of SSI, MSI and LSI logic macros, including a high resolution programmable delay line, is currently available in conjunction with AMCC's MacroMatrix® design kit. The library features speed/power options that allow the designer to maximize critical path speed while minimizing overall chip power. MacroMatrix is available for Mentor 8.x for both HP700 and SUN platforms.



Q20080 Die

Table 1. Performance Summary

PARAMETER	VALUE
Typical gate delay (1)	100–250 ps
Maximum toggle frequency	1.25 GHz
Maximum TTL input frequency	100 MHz
Maximum TTL output frequency	60 MHz
Maximum ECL input frequency (DIFF)	1.25 GHz
Maximum ECL output frequency	
single ended	350 MHz
Darlington (single ended, mixed mode only)	600 MHz
differential	1.0 GHz
CML (2)	1.25 GHz
ECL I/O pair delay (min/max)	330/560 ps

1 Based upon the use of complex macros and availability of speed/power options.

2 1.25 GHz CML output available on Q20P010 and Q20P025 only.

Table 2. Product Summary

Parameter	Q20004	Q20010	Q20025	Q20045	Q20080	Q20120	Q20P010*	Q20P025*	Q20M100
Equivalent Gates -Flip Flop (1)	450	979	2687	4520	7494	12518	649	2178	8980
	-Full Adder (2)	671	1469	4032	6782	11242	18777	973	3272
Core Cells	123	267	733	1233	2044	3414	177	595	2450
I/O Cell Count (3)	30	68	102	130	164	200	34	51	195
Structured Array Blocks	–	–	–	–	–	–	PLL	PLL	Memory
Power (W)(4)	<1W	1–2	2–3	3–5	5–9	8–14	1.5–2.5	2–4	10–17

1 Computed using 11 gate equivalent, 3 cell 3:1 MUXed D Flip-Flop – FF48 Macro.

2 Computed using 11 gate equivalent, 2 cell, One bit Full Adder, AD05 Macro.

3 Available I/O signals depends upon package and macro selection. Some I/O macros utilize more than one I/O cell.

4 Assumes 50% Inputs, 50% Outputs, Mixed mode supply. Utilization determines actual array power dissipation.

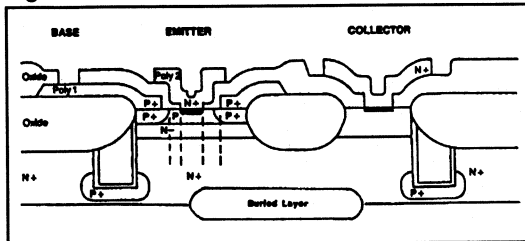
*Refer to the Q20P025/P010 data sheet for further information.

TECHNOLOGY

The Q20000 Series of ultra high performance ECL/TTL logic arrays are fabricated using a one micron bipolar process incorporating polysilicon emitter contacts, trench oxide isolation and an advanced base emitter structure (Figure 1). The $1\mu\text{m}$ wide trench reduces the collector substrate capacitance to less than half and doubles packing density when compared to conventional oxide isolated devices.

The minimum emitter feature size of $1\mu\text{m} \times 2\mu\text{m}$ (.6 \times 1.6 effective) combined with the low capacitance of the double poly, trench isolated process, achieves a cut-off frequency (F_T) of 14 GHz. The three level metal interconnect system employs fine pitch geometries of $4\mu\text{m}$ first, $5\mu\text{m}$ second and $7\mu\text{m}$ for the third level.

Figure 1. Process Cross Section



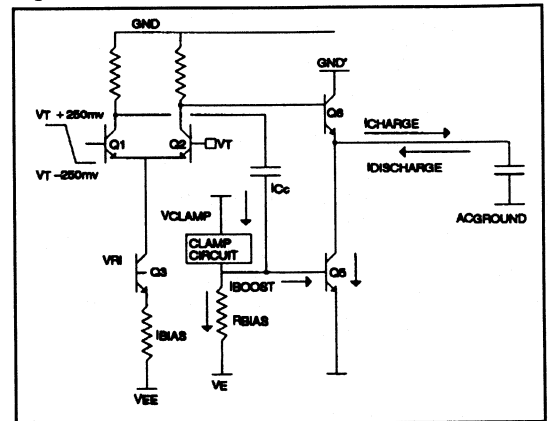
DESIGN INNOVATIONS

Conventional ECL structures use an output emitter follower biased with a static current source. When replicated and used hundreds or thousands of times per array these static current sources consume large amounts of current. As gate densities increase, this static current becomes a large power burden

To overcome this power burden, AMCC developed a patented dynamic discharge circuit (Figure 2) in place of the static current source for the emitter follower. This dynamic discharge circuit is comprised of a capacitively coupled active pull down arrangement. The static power requirements of this innovative technique are reduced substantially. Output skews between rising and falling edge delays are virtually eliminated and are significantly less affected by interconnect loading. This circuit technique in effect "Turbo Charges" the output.

The Turbo circuit is beneficial for circuits operating as high as 600 MHz and is used for the majority of macro functions in Q20000 series designs. For circuit paths operating up to 1.2 GHz, the Q20000

Figure 2. Q20000 Internal Cell Turbo Driver



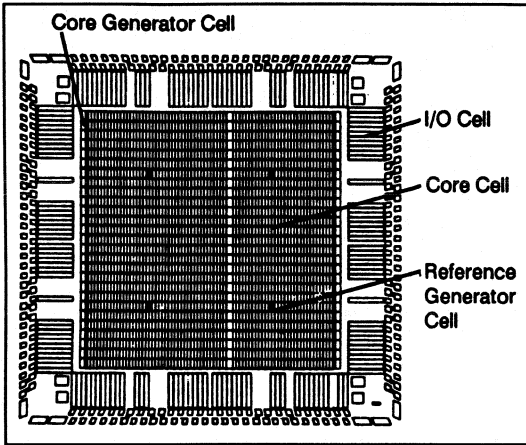
Series Macro Library includes functions with the traditional ECL output emitter follower structure. Refer to the "High Frequency Design Rules" section of the Q20000 Series Design Manual for further details on appropriate macro choices.

The I/O cell also benefits from the innovative Turbo design. Off chip skews for ECL outputs (10KH or 100K) as well as loading effects over conventional emitter follower structures are greatly improved. If a dual supply is available, the I/O cell can be configured with a Darlington output stage plus Turbo. This option allows a single I/O cell the ability to drive a 25 ohm parallel terminated line at reduced switch current, therefore reducing power requirements. Table 1 gives a brief summary of the I/O performance figures for the Q20000 family.

ARRAY ARCHITECTURE

The Q20000 Series is the industry's first ECL logic array family to utilize a channelless architecture called **Sea-of-Cells®**. The Sea-of-Cells organization eliminates the dedicated routing channels between cells used in channeled array architectures, thereby doubling the core density. Utilization is maintained at above 95% because of three levels of metal interconnect and AMCC's state-of-the-art place and route software. First level metal is used primarily for macro definition while second and third level metal handle inter-macro routing. The reduced static power of the Turbo cell allows power and ground distribution to be interspersed on the second and third level of metal, eliminating the need for a dedicated power plane.

Figure 3. Q20080 Die Organization



Like previous ECL logic array families from AMCC, the internal core cell of the Q20000 Series uses logic efficient three level series gated structures. The three level structure can operate over the full military temperature (-55°C ambient to +125°C case) and voltage range of 10KH or 100K logic because of AMCC's unique design. Table 3 lists representative macro functions and the number of cells required for implementation. A latch can be implemented in only one cell.

The I/O cells are designed to interface with either 10KH, 100K or TTL thresholds. For over 1 GHz operation, a differential CML output structure is also available for use with selected I/O cells and package pins.

Each I/O cell in the array family can be either an input or an output. Bi-directional operation is achieved by paralleling any two adjacent I/O cells. The flexible I/O structure of the Q20000 family allows operation in either 100% ECL I/O, 100% TTL I/O and mixed ECL/TTL I/O in either dual supply or single supply modes.

Table 3. Functional Density

MACRO FUNCTION	CELL USAGE	MACRO NAME
Flip-Flop with AR; A/AN outputs	2	FF12
Flip-Flop with EXORed Data; Q output	2	FF22
Flip-Flop with 3:1 MUXed Data, Q output	3	FF48
D Latch	1	LA11
4:1 Mux	2	MX21
2 Input Exclusive-OR, Y output	1	EX30
4-Bit Carry Look Ahead Adder	24	ADD00
4-Bit Counter with AR, AS	26	CTR02
8-Bit Comparator	40	CMP00

STRUCTURED ARRAYS

Three members of the Q20000 family feature embedded functions. The Q20P025 and Q20P010 arrays include a 1.25GHz PLL with 2500 and 1000 usable logic gates. The Q20M100 array includes eight 32x18 bit RAM blocks (total 4K) and 10,000 usable gates. Refer to the Q20P010/025 and Q20M100 data sheets for further details.

PACKAGING

The Q20000 Series logic arrays are available in a range of standard packages including thermally enhanced plastic, surface-mountable ceramic chip carriers and ceramic pin grid arrays (see Table 4). For complete details consult the AMCC Packaging Guide.

HIGH SPEED/LOW POWER MACROS

The Q20000 Series macro library offers maximum flexibility in the optimization of circuit performance and power consumption. A full complement of macros is offered with low power, standard and high speed options. The high speed options require somewhat more power than standard, but provide a significant improvement in propagation delay and/or maximum operating frequency. The low power versions of macros can be used to reduce power consumption in non-critical paths.

Table 4. Q20000 Series Packaging Matrix Θ_{ja} in °C/W (Still Air)

Package	Q20004	Q20010 *Q20P010	Q20025 *Q20P025	Q20045	Q20080	Q20120 *Q20M100
Plastic 44 PLCC	48					
Plastic 52 PQFP	46					
Plastic 100 EDQUAD		28	28			
Plastic 120 EDQUAD			18			
Plastic 208 EDQUAD				17	17	
Ceramic 44 LDCC	36					
Ceramic 100 LDCC		41				
Ceramic 132 LDCC			36			
Ceramic 196 LDCC				26	25	
Ceramic 224 LDCC					22	19
Ceramic 100 PGA		26				
Ceramic 149 PGA			25			
Ceramic 209 PGA				21		
Ceramic 251 PGA					19	
Ceramic 301 PGA						17

Table 5. Macro Speed Power Options: Example

GT65 — 8-INPUT OR	High Speed	Standard	Low Power
T_{PD} min/max (ps) ⁽¹⁾	87/160	103/189	167/298
I_{EE} (mA)	1.12	0.776	0.455
Max Operating Freq. (MHz)	1200	800	600

⁽¹⁾ $T_{pd} = [T_{PD(+)} + T_{PD(-)}] / 2$. Path shown is any input to Y output.

Table 5 illustrates the effects of speed/power selections on equivalent gate delay and power consumption. As the table indicates the overall macro performance versus power consumption can be varied significantly depending upon the option selected.

The circuit designer can make the selection of speed/power options at the time of schematic capture on a supported engineering workstation. Through simulation, the designer can fine-tune the circuit to provide the required mix of performance and power savings.

The macro section in the final portion of this data sheet provides additional information on speed/power trade-offs.

Table 6. Signal Interface Options

INPUT	BIDIRECTIONAL	OUTPUT
TTL	TTL Transceivers	TTL Totem Pole TTL Tri-State TTL Open Collector
ECL 10K and 10KH	ECL 10K and 10KH Transceivers	ECL 10K and 10KH
ECL 100K	ECL 100K Transceiver	ECL 100K
CML		CML Open Collector

PROGRAMMABLE DELAY LINE MACRO (PD00S)

The PD00S is a programmable delay macro in the Q20000 gate array library that provides a timing generation or deskew function for precision timing applications, such as ATE, instrumentation, clock distribution, and high speed buses.

Key features of the PD00S include:

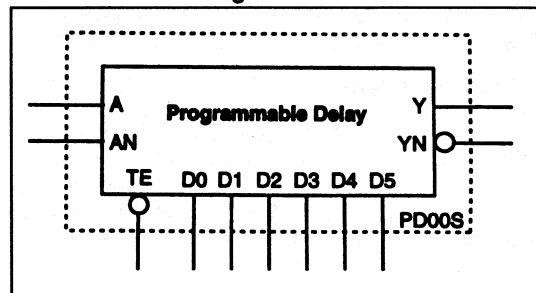
- Up to 30 delay lines per array possible
- Local macro voltage regulation for superior crosstalk performance
- Cascadable for greater delay range
- 46 core cells in size
- Ring oscillator mode for testability
- 6 decode bits for 63 selectable delay steps

A differential signal is applied to input pin A/AN, is modified with the addition of a delay specified by the binary input address pins D(0:5), and emerges at output pins Y/YN. The test enable input (TE) is held high for normal operation. When the TE input is put low in the test mode, the Y/YN output is internally inverted and fed back to the A/AN input thus allowing the PD00S to function as a ring oscillator and enable operation verification. Changing the binary code of address pins D(0:5), changes the frequency of Oscillations of the PD00S macro that allows for convenient testing of accuracy through delta frequency measurements.

Performance Summary

Accuracy	≤80 ps
Resolution (typ)	40 ps
Minimum delay range	2.1 ns
IEE (typ)	22 mA
Max frequency	250 MHz
Minimum pulse width	2 ns
Minimum propagation delay	1.30 ns
Linearity to D1	—
No missing codes in 80 ps steps	—

Functional Block Diagram



1. (Y, YN) = A, AN
2. NOMINAL DELAY = $(40 \cdot D_0 + 80 \cdot D_1 + 160 \cdot D_2 + 320 \cdot D_3 + 640 \cdot D_4 + 1280 \cdot D_5 + 1300)$ ps
3. TE = LOW, Puts PD00S in Ring Oscillator Mode
4. TE = High, Normal Mode

CUSTOM MACROS

To further enhance the functionality of the Q20000 Series macro library, AMCC has developed a macro development system. It uses a correct-by-construction approach to develop macros that meet all the pertinent design rules. As individual circuit applications warrant, macros with unique characteristics can be developed to optimize the array design.

FLEXIBLE I/O STRUCTURE

The Q20000 Series I/O cells are configurable to provide a universal range of interface options for both single and dual supply modes. The mixed ECL/TTL capabilities allow interface to both technologies on a single chip without the use of external translators. (Refer to Table 6.)

DESIGN INTERFACE

AMCC has structured its circuit design interface to provide maximum flexibility while ensuring design correctness. For implementations using an engineering workstation, AMCC provides MacroMatrix software. MacroMatrix works in conjunction with Mentor 8.X to provide the following capabilities:

- Schematic Capture
- Logic Simulation
- Pre-Layout Delay Estimation (Front Annotation)
- Array and Technology-Specific Rules Checks (ERC's)
- Estimated Power Computation
- Layout Netlist Generation
- Post-Layout Timing Verification (Back Annotation)
- Graphical Floor Planning (IPL)
- Dynamic Timing and Test Vector Analysis (RaceCheck™)

Upon submission of the design database to AMCC, a comprehensive review of the circuit is performed making use of the very same EWS and MacroMatrix tools used by the designer. No "golden simulator" is employed to verify the timing of the design. No translation of the logic data is required so the chance of non-design-related errors is virtually eliminated.

AMCC DESIGN SERVICES

AMCC also provides a number of additional support services including:

- Local and Factory Applications Engineering Support
- Complete Design Documentation
- Full Design Implementation Service—Turnkey

ECL INTERFACE

The Q20000 Series arrays can interface to standard and positive reference (+5V) ECL 10K, 10KH and 100K levels. ECL inputs can enter the array from any I/O cell and, in some cases, may be connected directly to core cells without additional buffering. Additionally, signals can be input differentially to remove common mode noise.

ECL outputs can leave the arrays from any I/O cell. Different configurations of the I/O cells provide for a 50 ohm or 25 ohm output drive. Differential CML outputs are available for high frequency paths.

The Q20000 Series allows for a special type of ECL output macro which incorporates a Darlington output configuration. These macros maintain standard ECL 10K, 10KH and 100K output levels, while netting an improvement in drive capability and toggle frequency over standard ECL outputs. While requiring dual power supplies, the Darlington output macros will accommodate 25 or 50 ohm loads in a single I/O location while maintaining ECL standard levels.

Bidirectional ECL operation is available using two adjacent I/O cells.

TTL INTERFACE

TTL signals can enter from any I/O cell. Once on-chip, TTL signals are automatically converted to internal voltage levels for internal logic operations.

Signals leaving the array are translated from an internal voltage level to TTL level in the I/O cell. Following this translation, TTL outputs are available in totem pole, 3-state or open collector configurations. TTL outputs, like inputs, can be configured with any I/O cell.

Bidirectional TTL operation is available in single cell and dual I/O cell implementations.

POWER SUPPLY CONFIGURATIONS

On the Q20000 Series arrays there are four basic interface configurations: single-supply ECL, single-supply TTL, and dual-supply and single-supply mixed TTL/ECL. Power supply requirements for each mode of operation are shown in Table 7.

Table 7. I/O Power Supply Configuration

I/O MODE	V_{EE}	V_{CC}
ECL 100K	-4.2 to -4.8V*	—
ECL 10K, 10KH	-4.7 to -5.7V	—
ECL 100K	-4.2 to -4.8V*	4.5 to 5.5V
ECL 10K, 10KH	-4.7 to -5.7V	4.5 to 5.5V
ECL 100K/TTL	-4.2 to -4.8V*	4.5 to 5.5V
ECL 10K, 10KH/TTL	-4.7 to -5.7V	4.5 to 5.5V

*May be configured with a -5.7 supply. Consult AMCC for DC parametrics

INTERNAL LOGIC CELL CAPABILITIES

The Q20000 Series internal logic cells are all identical in structure and are uniformly positioned in a Sea-Of-Cells matrix across the internal core area of the array. Each cell contains 13 uncommitted transistors and 13 resistors. The cells are individually configurable to provide a variety of logic functions through the use of the Q20000 Series macro library. The macro library provides SSI, MSI and some basic LSI functions. The higher functionality macros provide the advantages of higher speed, lower power and increased circuit density over a logically equivalent SSI macro implementation.

Figure 4

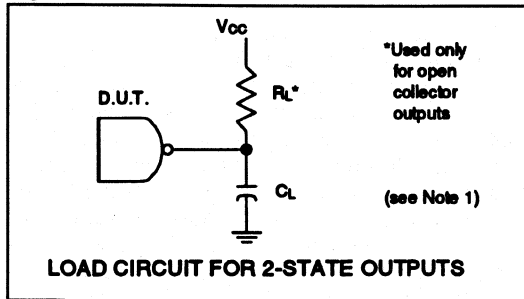


Figure 5

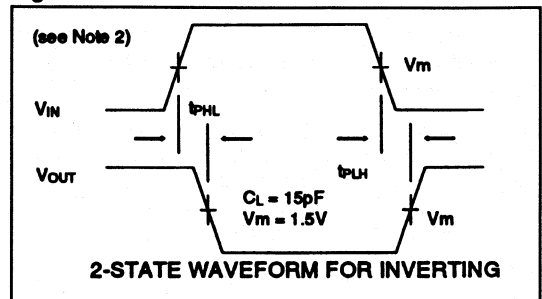


Figure 6

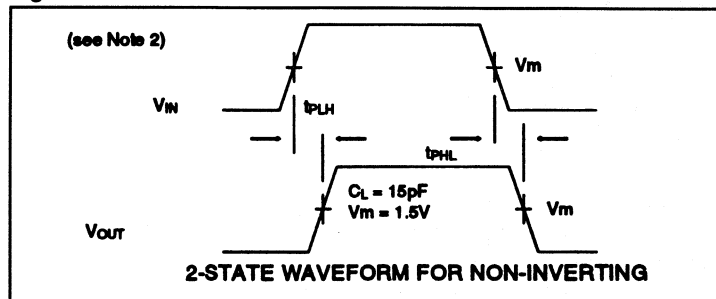


Figure 7

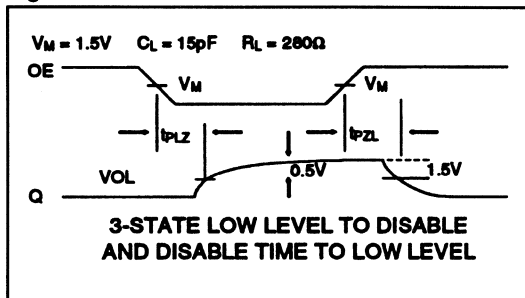


Figure 8

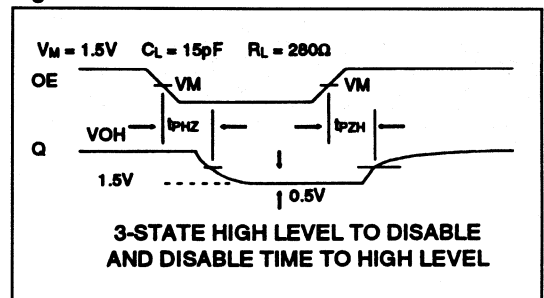
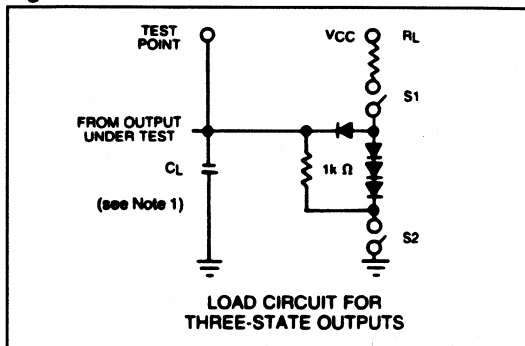


Figure 9



3-STATE TEST CIRCUIT SWITCH TABLE

TEST FUNCTIONS	S1	S2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pHZ}	Closed	Closed
t_{pLZ}	Closed	Closed

NOTES:

- Standard TTL load circuit used for macro specification. C_L includes probe, jig and package.
- $V_{IN} = 0$ to 3.0 volts.

Figure 10

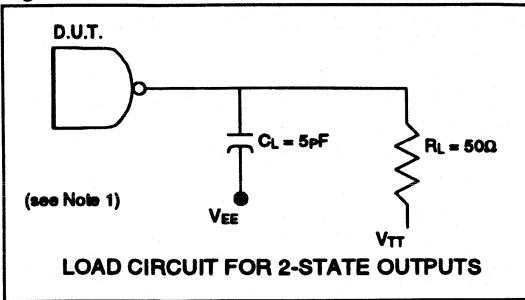


Figure 11

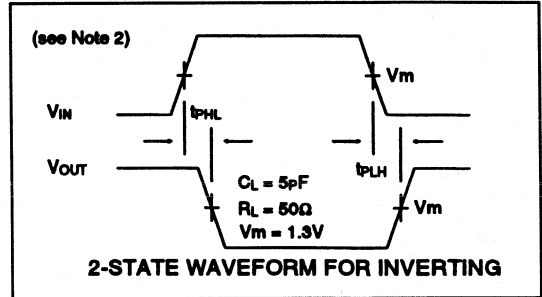
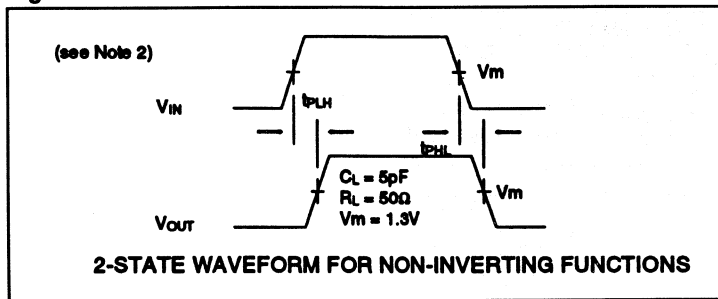


Figure 12



NOTES:

1. Standard ECL load circuit used for macro specification. See Figure 10.
2. $V_{IN} = V_{IHMAX}$ to V_{ILMIN} .

RECOMMENDED OPERATING CONDITIONS — COMMERCIAL				
PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE}) $V_{CC} = 0$ 10K, 10KH Mode 100K Mode	-4.94	-5.2	-5.46	V
	-4.2	-4.5	-4.8*	V
	—	1.0	3.0	ns
ECL Input Signal Rise/Fall Time	—	1.0	3.0	ns
ECL Input Voltage	-2.0			V
TTL Supply Voltage (V_{CC})	4.75	5.0	5.25	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	0 (ambient)		70 (ambient)	°C
Junction Temperature			130	°C

RECOMMENDED OPERATING CONDITIONS — MILITARY				
PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE}) $V_{CC} = 0$ 10K, 10KH Mode 100K Mode	-4.7	-5.2	-5.7	V
	-4.5	-4.5	-4.8*	V
	—	1.0	3.0	ns
ECL Input Signal Rise/Fall Time	—	1.0	3.0	ns
TTL Supply Voltage (V_{CC})	4.5	5.0	5.5	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	-55 (ambient)		125 (case)	°C
Junction Temperature			150	°C

* -5.7V is possible. Consult AMCC for ECL 100K DC parametric operating at this voltage.

ABSOLUTE MAXIMUM RATINGS*	
ECL Supply Voltage V_{EE} ($V_{CC} = 0$)	-8.0 VDC
ECL Input Voltage ($V_{CC} = 0$)	GND to -2.0 V
ECL Output Source Current (continuous)	-50mA DC
TTL Supply Voltage V_{CC} ($V_{EE} = 0$)	7.0 V
TTL Input Voltage ($V_{EE} = 0$)	5.5 V
Operating Temperature	-55°C (ambient) to +125°C (case)
Operating Junction Temperature T_J	+150°C
Storage Temperature	-65°C to +150°C

*Long term exposure at these limits may result in permanent change or damage to the circuits. Actual circuit operation at these conditions is not recommended nor implied.

AC ELECTRICAL CHARACTERISTICS							
SYMBOL	PARAMETER	TEST CONDITIONS	COM 0°C/+70°C		MIL -55°C/+125°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PD}^{ECL}	ECL Input Propagation Delay Including Buffer IE94S		59	263	57	281	ps
t_{PD}^{TTL}	TTL Input Propagation Delay Including Buffer IT50H		93	535	65	602	ps
t_{OPD}^{ECL}	ECL Output Propagation Delay — Darlington OK40S	No Load	185	340	157	356	ps
t_{OPD}^{TTL}	TTL Output Propagation Delay	Standard OT67S	2213	4292	2056	4375	ps
t_{FPD}	Internal Equivalent Gate Delay	Low Power	120	250	120	250	ps
		Standard	105	175	105	175	ps
F_{max}	Internal Flip/Flop Toggle Freq.	High Speed		1.25		1.25	GHz
F_{in}^{ECL}	ECL Input Frequency at Package Pin 1	Single-Ended		600		600	MHz
		Differential High Speed		800		800	MHz
		Driver		1.25		1.25	GHz
F_{out}^{ECL}	ECL Output Frequency at Package Pin 1	Single-Ended		350		350	MHz
		Differential		1.25		1.25	GHz
		Darlington		600		600	MHz
		CML		1.25		1.25	GHz
F_{in}^{TTL}	TTL Input Frequency at Package Pin 1	Standard		60		60	MHz
		High Speed		100		100	MHz
F_{out}^{TTL}	TTL Output Frequency at Package Pin	Low Power		20		20	MHz
		Standard		45		45	MHz

ECL 10K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -5.2V_{1,8}$

					T_{case}	UNIT
	-55°C	0°C	25°C	70°C	125°C	
V_{OHmax}^3	$V_{CC}-850$	$V_{CC}-770$	$V_{CC}-730$	$V_{CC}-650$	$V_{CC}-575$	mV
V_{IHmax}^5	$V_{CC}-800$	$V_{CC}-720$	$V_{CC}-680$	$V_{CC}-600$	$V_{CC}-525$	mV
V_{OHmin}^3	$V_{CC}-1080$	$V_{CC}-1000$	$V_{CC}-980$	$V_{CC}-920$	$V_{CC}-850$	mV
V_{IHmin}^5	$V_{CC}-1255$	$V_{CC}-1145$	$V_{CC}-1105$	$V_{CC}-1045$	$V_{CC}-1000$	mV
V_{ILmax}^5	$V_{CC}-1510$	$V_{CC}-1490$	$V_{CC}-1475$	$V_{CC}-1450$	$V_{CC}-1400$	mV
V_{OLmax}	$V_{CC}-1655$	$V_{CC}-1625$	$V_{CC}-1620$	$V_{CC}-1585$	$V_{CC}-1545$	mV
V_{OLmin}	$V_{CC}-1980$	$V_{CC}-1980$	$V_{CC}-1980$	$V_{CC}-1980$	$V_{CC}-1980$	mV
V_{ILmin}^5	$V_{CC}-2000$	$V_{CC}-2000$	$V_{CC}-2000$	$V_{CC}-2000$	$V_{CC}-2000$	mV
I_{IH}^2MAX	30	30	30	30	30	μA
I_{IL}^2MAX	-5	-5	-5	-5	-5	μA

ECL 100K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -4.5V_{3,8}$

SYMBOL	PARAMETER	TEST DC CONDITIONS	COMM 0°/+70°C			MIL -55°/+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
			V_{OH}	Output Voltage HIGH	Loading is 50 Ohms to -2V	$V_{CC}-1035$		$V_{CC}-850$	
V_{OL}	Output Voltage LOW	Loading is 50 Ohms to -2V	$V_{CC}-1830$		$V_{CC}-1605$	$V_{CC}-1880$		$V_{CC}-1595$	mV
V_{IHmin}^5	Input Voltage HIGH	Maximum input voltage HIGH	$V_{CC}-1145$		$V_{CC}-800$	$V_{CC}-1145$		$V_{CC}-800$	mV
V_{ILmax}^5	Input Voltage LOW	Maximum input voltage LOW	$V_{CC}-1950$		$V_{CC}-1475$	$V_{CC}-1950$		$V_{CC}-1475$	mV
I_{L}^2	Input LOW Current	$V_{IN} = V_{ILmin}$			-0.5			-0.5	μA
I_{H}^2	Input HIGH Current	$V_{IN} = V_{IHmax}$			30			30	μA

TTL INPUT/OUTPUT DC CHARACTERISTICS⁷

SYMBOL	PARAMETER	TEST DC CONDITIONS	COMM 0°/+70°C			MIL -55°/+125°C			UNIT
			MIN	TYP ⁴	MAX	MIN	TYP ⁴	MAX	
V _{IH} ⁵	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			2.0			V
V _{IL} ⁵	Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8			0.8	V
V _{IK}	Input clamp diode voltage	V _{CC} = Min, I _{IN} = -18 mA		-0.8	-1.2		-0.8	-1.2	V
V _{OH}	Output HIGH voltage	V _{CC} = Min, I _{OH} = -1 mA	2.7	3.4		2.4	3.4		V
V _{OL}	Output LOW voltage	V _{CC} = Min	I _{OL} = 4 mA		0.4			0.4	V
			I _{OL} = 20 mA		0.5			0.5	V
I _{OZH}	Output "off" current HIGH (3-state)	V _{CC} = Max, V _{OUT} = 2.4 V	-50		50	-50		50	μA
I _{OZL}	Output "off" current LOW (3-state)	V _{CC} = Max, V _{OUT} = 0.4 V	-50		50	-50		50	μA
I _{IH}	Input HIGH current	V _{CC} = Max, V _{IN} = 2.7 V			50			50	μA
I _I	Input HIGH current at Max	V _{CC} = Max, V _{IN} = 5.5 V			1.0			1.0	mA
I _{IL} ⁶	Input LOW current	V _{CC} = Max, V _{IN} = 0.5 V			-0.4			-0.4	mA
I _{OS}	Output short circuit current	V _{CC} = Max, V _{OUT} = 0.5 V	-25		-100	-25		-100	mA

¹Data measured with V_{EE} = -5.2 ± .1V (or V_{CC} = 5.0 ± .1V for +5V ref. ECL 10K) assuming a +50°C rise between ambient (T_a) and junction temperature (T_j) for -55°C, 0°C, +25°C and +70°C, and a +25°C rise for +125°C. Specifications will vary based upon T_j. See AMCC Packaging and Design Guides concerning V_{OH} and V_{OL} adjustments associated with T_j for packages and operating conditions.

²Per fan-in.

³Data measured at thermal equilibrium, with maximum T_j not to exceed recommended limits. See AMCC Packaging Guide to compute T_j for specific package and operating conditions. For +5V ref. ECL 100K, V_{OH} and V_{OL} specifications will vary based upon power supply. See AMCC Design Guide for adjustment factors.

⁴Typical limits are at 25°C, V_{CC} = 5.0V.

⁵These input levels provide zero noise immunity and should only be tested in a static, noise-free environment. Use extreme care in defining input levels for dynamic testing. Many outputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using V_{IL} ≤ 0.4V and V_{IH} ≥ 2.4V for dynamic TTL testing and V_{ILMIN} and V_{IHMAX} for ECL testing.

⁶For standard speed options only.

⁷See figures 4-9.

⁸See figures 10-12.

FEATURES

- On-chip high frequency phase-locked loop
- Up to 1.25 GHz capability
- Edge jitter as low as 50 ps (pk-pk)
- 900 and 3000 gates of customizable digital logic
- Utilizes proven Q20000* Series macro library
- 100 ps equivalent gate delays
- Low power (.5–1.0 mW/gate)
- 10K, 10KH, 100K ECL, PECL and mixed ECL/TTL capability
- Speed/power programmable logic and I/O
- Operation over commercial and military ranges
- Up to 95% utilization of digital logic
- Full logic simulation modeling support of PLL functions

Figure 1

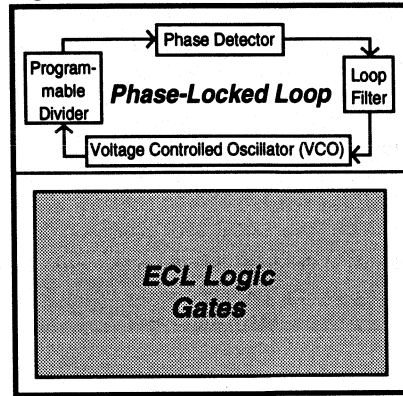


Table 1. Performance Summary

Parameter	Value
Phase-Locked Loop	
Operating Frequency	125 MHz–1.25 GHz
Edge Jitter (pk–pk)	50–100 ps
Residual BER	10E–12
Acquisition Time (typical)	1.0 μs
Digital	
Typical Gate Delay	100–250 ps
Maximum Toggle Frequency	1.25 GHz
Maximum TTL Input Frequency	100 MHz
Maximum TTL Output Frequency	60 MHz
Maximum ECL Input Frequency	1.25 GHz
Maximum ECL Output Frequency	1.25 GHz

Table 2. Product Summary

	Q20P010		Q20P025	
Equivalent Gates				
Full Adder Method	928		3120	
Flip-flop Method	637		2142	
Internal Logic Cells	177		595	
I/O Pins				
Package	68	100	100	132
	LDCC	LDCC	LDCC	LDCC
PLL Related				
Loop Filter	0	0	0	0
Signals	12	12	12	12
Powers & Grounds	8	8	8	8
Digital				
Signals	23	34	45	51
Powers & Grounds	20	20	22	22
AC Monitor & Thermal Diode				
	4	4	4	4
Maximum Total Power (W)				
	1.5–3		2–3	
Availability				
	Now		Now	

APPLICATIONS

- High speed datacom
- Video shift registers
- High performance telecom
- Frequency synthesis
- Timing generation circuits
- Self-timed systems

DESCRIPTION

The AMCC Q20P010 and Q20P025 PLL logic arrays offer gate densities of 900 and 3000 equivalent gates with a high frequency phase-locked loop on-chip. Combining a PLL with user-definable Q20000 series arrays, the Q20P010 and Q20P025 are tailored for high speed serial communication, video, and clock generation applications.

Clock synthesis and clock recovery macros are available for the on-chip phase-locked loop. Speed options ranging from 125 MHz to 1.25 GHz are available. Complete simulation models, implementing all CSU/CRU functions, are available for digital logic simulation on Mentor and Valid workstations as well as the LASAR simulator. Lock detect, local and link loopback features are also selectable options.

For the digital logic portion of the array, an extensive library of SSI and MSI macros is available as part of AMCC's MacroMatrix™ design kit. Latches, parallel-to-serial converters, encode/decode functions, high speed shift registers, bit error rate computation and divide-down counters can easily be assembled to operate in conjunction with the phase-locked loop to meet specific application needs.

*This device specification is an addendum to the Q20000 Series device specification.

DIGITAL LOGIC

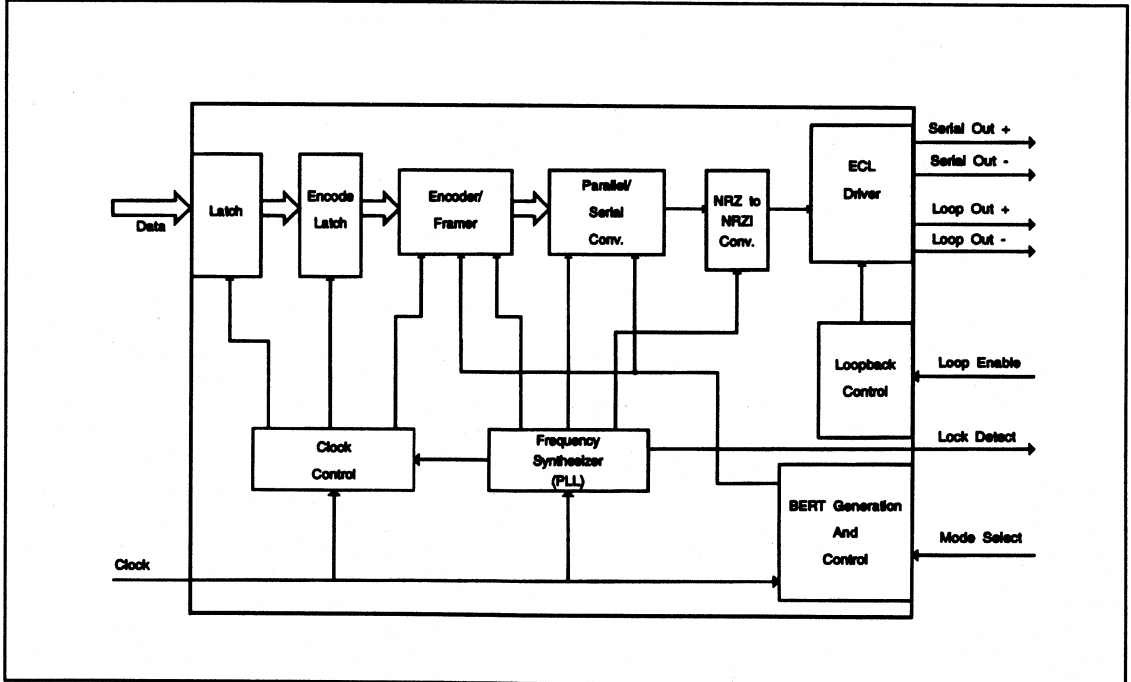
The Q20000 Series is the industry's first ECL logic array family to utilize a channelless architecture called **Sea-of-Cells™**. The Sea-of-Cells organization eliminates the dedicated routing channels between cells thereby doubling the core density. Utilization is maintained at greater than 95% due to three layer metal interconnect and AMCC's state-of-the-art place and route system. A full complement of SSI and MSI macros is offered with low power, standard and high speed options.

To minimize noise injection from the core logic into the PLL section of the device, all core logic must be operated synchronously with the PLL.

PHASE-LOCKED LOOP MACROS

A selection of clock synthesis and clock recovery macros are available for the on-chip phase-locked loop. PLL center frequencies of 1000, 1062, and 1244 MHz are available with user selectable divide ratios of 1, 2, 4, and 8. This results in speed options of 125, 133, 155, 250, 266, 311, 500, 531, 622, 1000, 1062, and 1244 MHz that are available to operate synchronously with the logic in the digital portion of the array. Additional frequency options can be created to meet specific design requirements. AMCC defined loop filter components for each frequency option have been established for applications with divide ratios up to 64, transition densities of 30%–70%, and run lengths up to 64-bit times. Lock detect, local and link loopback features are also available options.

Figure 2. Representative Transmitter Block Diagram



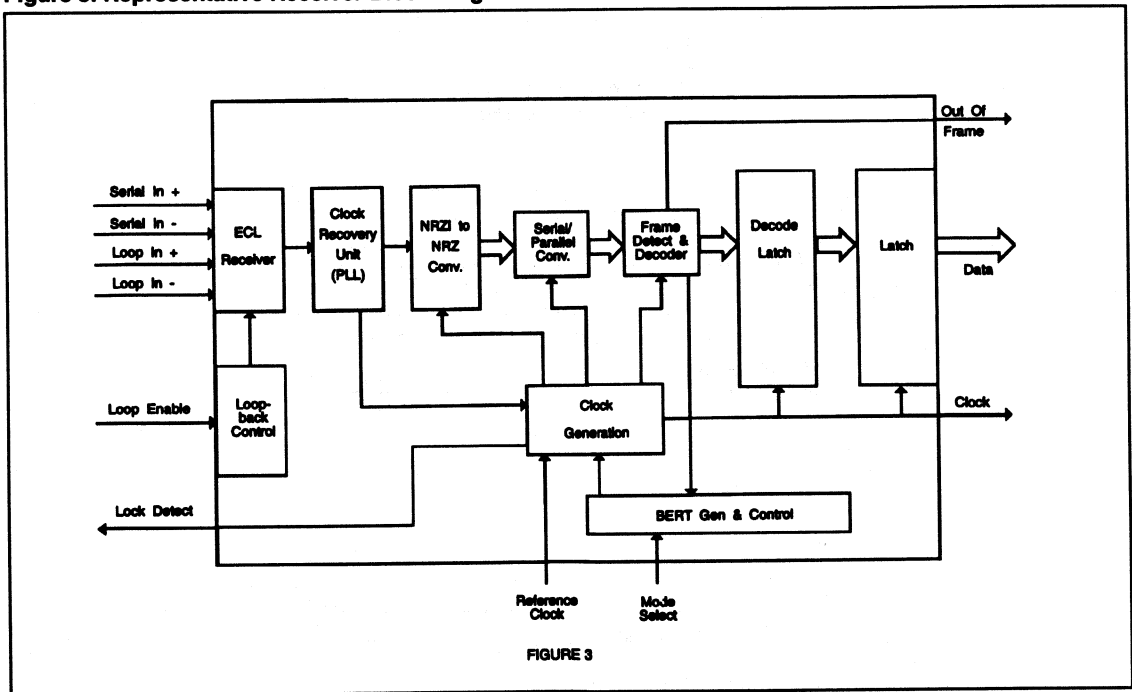
ENCODING/DECODING

High speed datacom and telecom applications frequently require a standard encoding scheme to ensure favorable bit stream characteristics and inter-operability. AMCC initially offers an encoder/decoder scheme implemented using standard macro library components. Popular in datacom applications, IBM's 8B/10B encoding scheme offers DC-balance and short run lengths in an efficiently architected implementation. The 8B/10B macros are available under a licensing and nondisclosure agreement. Other preferred encoding and decoding schemes can easily be designed using the digital portion of the Q20P010 and Q20P025.

FLEXIBLE I/O STRUCTURE

The Q20P010 and Q20P025 array I/O cells are configurable to provide a flexible range of interface options. The I/O cells are designed to interface with standard (-5.2V or 4.5V) and positive reference (+5V) ECL 10KH and ECL 100K or TTL thresholds. The mixed ECL/TTL capabilities allow interface to both technologies on a single chip without the use of external translators. For dual power supply devices, the I/O is also capable of a Darlington-type ECL output which provides significant improvement in drive capability, toggle frequency, and power dissipation over standard ECL outputs. For TTL signals, a special low-noise, low-power controlled edge rate, single cell bidirectional I/O macro is available for use in Q20P010 and Q20P025 circuits.

Figure 3. Representative Receiver Block Diagram

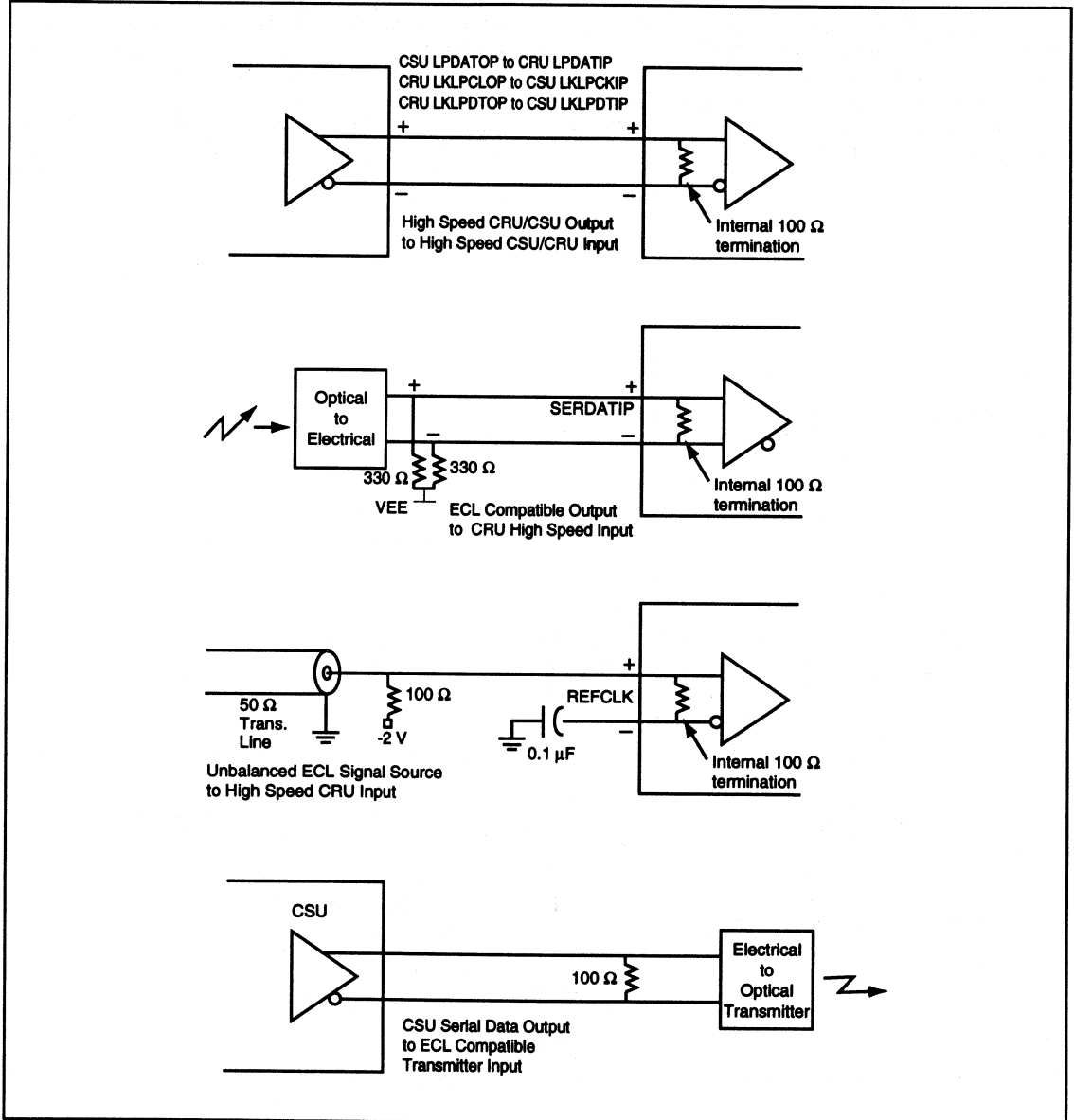


HIGH SPEED I/O CONNECTIONS

The high speed ECL compatible differential inputs in both the CRU and CSU macros have a built in 100Ω termination resistor across the differential pair, eliminating terminating components in loopback and data

paths and ensuring low jitter interfaces. Figure 4 shows some examples of high speed CSU/CRU input and output connections.

Figure 4. High Speed Input and Output Applications



PHASE-LOCKED LOOP

The basic phase-locked loop components are shown in the PLL block diagram (Figure 5). The loop consists of a phase detector, which compares the phase difference between the VCO and the reference input, a loop filter, which converts the phase detector output into a smooth DC voltage, and the VCO, which generates a frequency based on its input voltage.

Metal pattern implementations on AMCC-provided PLL building blocks differ for clock synthesis and clock recovery. This is due to the differences in reference inputs to the phase detector. In the case of the clock synthesis PLL, the reference input is a very stable crystal-based source. For clock recovery from a serial data stream the reference input has varying transition density; i.e., different run lengths of 1's and 0's with short term frequency variations.

The loop filter generates a control voltage for the VCO input based on the output of the phase detector. Different sets of loop filter components must be specified for both the clock synthesis and clock re-

covery applications. Appropriate filter components will be required for different encoding schemes, acquisition time requirements and system noise environments. AMCC provides on-chip selected sets of resistors and capacitors appropriate for specific system conditions.

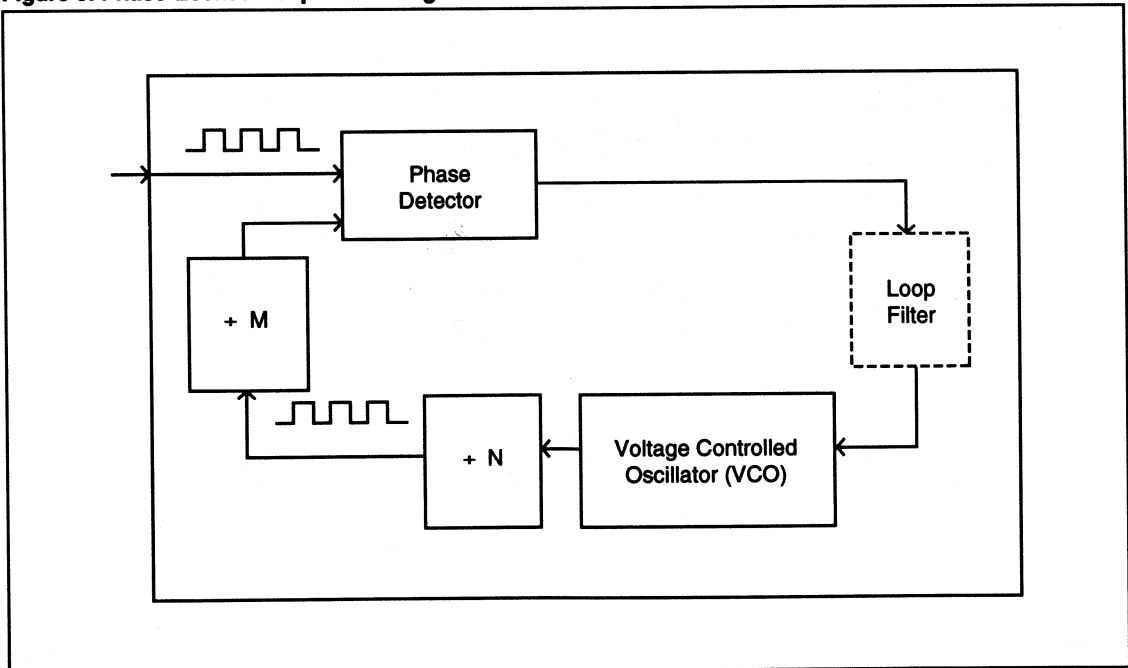
SPECIAL FEATURES

Lock Detect

For CRU macros, lock detect indicates the phase state of the PLL relative to the incoming data stream. Control pins from the core logic area permit lock detect to be indicated after 512, 1024, 2048, or 4096 bit times depending upon loop filter parameters. On CRU macros, if the serial data inputs have an instantaneous phase jump, the CRU will not indicate out-of-lock state, but will recover correct phase alignment within the pre-loaded bit times.

For the CSU macro, lock detect indicates the phase state of the PLL relative to the incoming reference clock.

Figure 5. Phase-Locked Loop Block Diagram



LOOPBACK MODE

Local Loopback

For datacom or telecom applications, local and link loopback is supported. Local loopback requires both a transmit chip and a receive chip. When enabled, serial encoded data from the transmit chip is sent to the receive chip where the clock is extracted and the data decoded. The parallel data is then sent to the subsystem for verification. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium, and allows system diagnostics.

Link Loopback

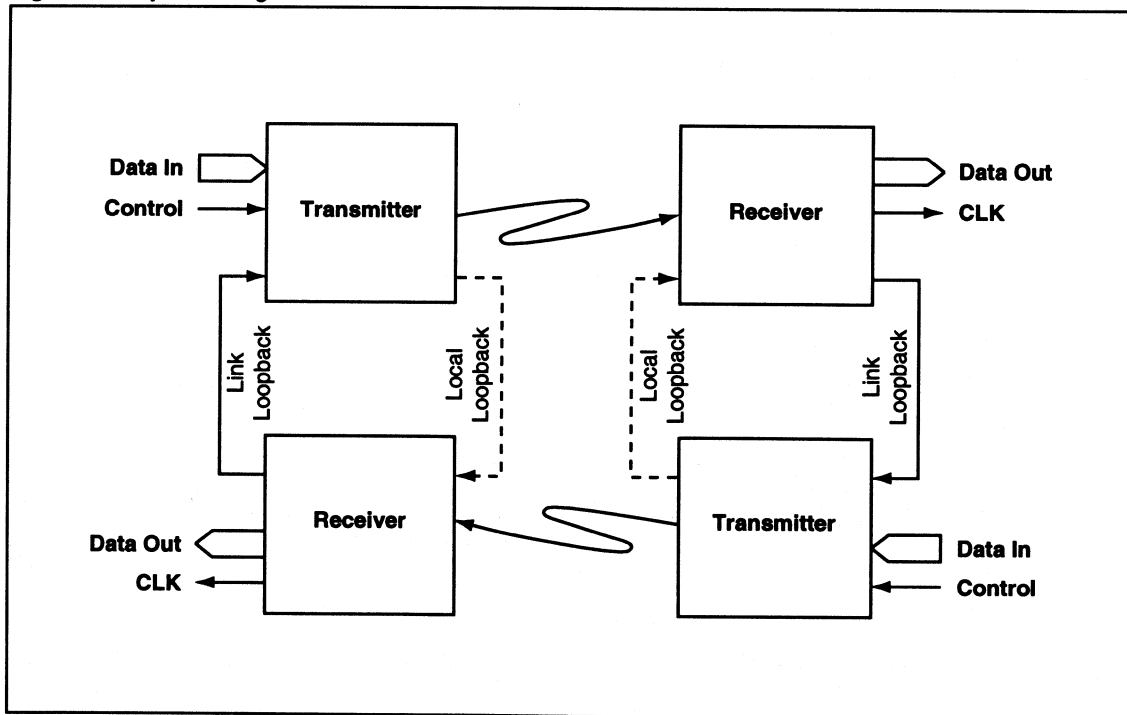
Link loopback provides a means for link testing. When link loopback mode is enabled, the transmitter accepts serial clock and data from the receiver chip.

The serial data is relocked using the link loopback clock to minimize the data distortion and then transmitted via the serial data output pins. Link loopback can also be used to implement a repeater function, with clock jitter and data distortion determining the number of repeaters allowed.

TEST/BYPASS MODE

Clock recovery and clock synthesis macros have testability input pins to aid in functional testing or PLL clock bypass tests. "Test Clock Enable" places the macros into test mode. An externally generated clock can then be input via the reference clock inputs. The PLL clock bypass path is capable of operating at 1.25 GHz to allow at speed testing of the chip functions or for applications in which a user selectable external clock signal needs to be supported.

Figure 6. Loopback Diagram



Clock Synthesis Macros

The clock synthesis PLL will generate a high frequency clock in phase with the input reference. A typical frequency multiplication factor is 20, with extension as high as 64. Critical parameters for the clock synthesis PLL are jitter and accuracy. AMCC loop filter components are set to optimize the loop for minimum phase jitter and maximum accuracy, with less emphasis on acquisition time. Loop filter parameters can be varied by AMCC on a custom basis.

Specifications

Input Reference Frequency — The input reference frequency can be a selected divide ratio of the synthesized clock frequency. The maximum divide ratio is 64.

Reference Clock Jitter — The reference clock needs to be generated from a stable source such as a crystal oscillator. The allowable rms jitter cannot exceed .04% of the reference clock pulse width.

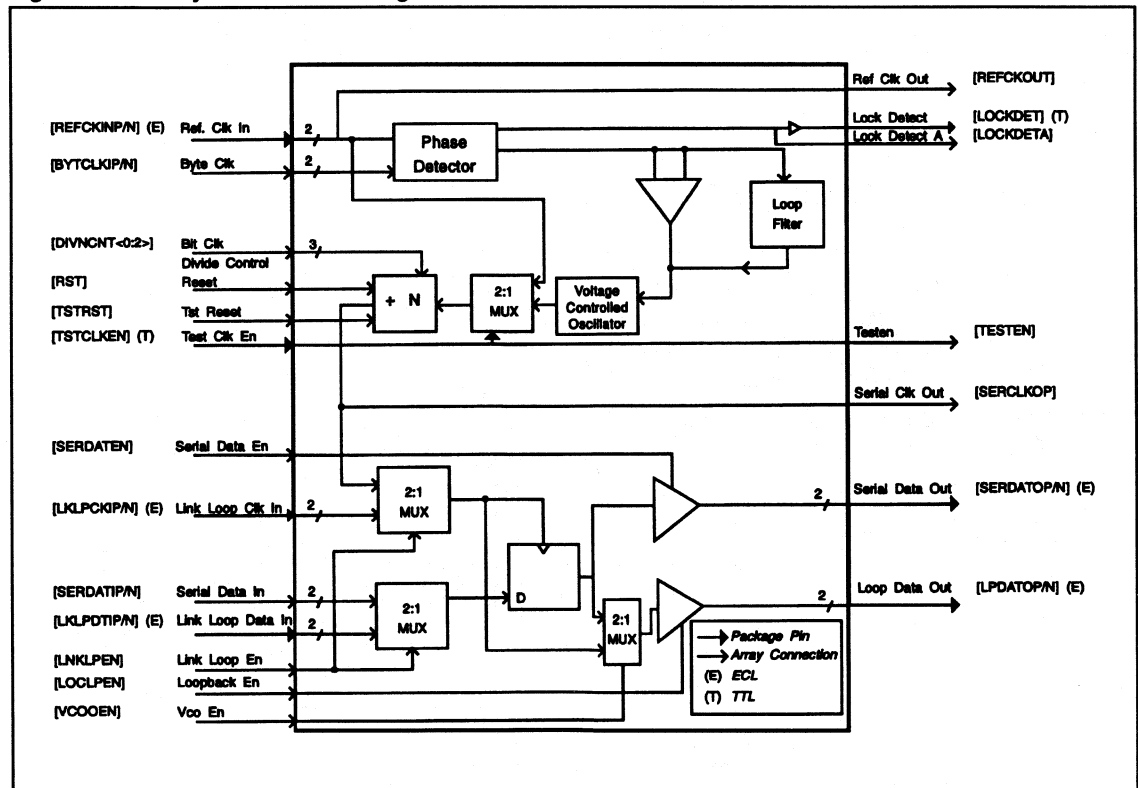
Input Reference Stability — The reference clock stability should be less than 100 ppm.

Acquisition Time — The loop acquisition time will depend on the loop filter parameters. (1.0 μ s to 250 μ s values are typical)

Edge jitter — The output edge jitter will depend on the loop filter parameters. (50 to 100 ps pk-pk values are typical)

Supply Voltage Sensitivity — Power supply noise rejection will be between 40 and 60 dB depending on the noise spectrum.

Figure 7. Clock Synthesis Macro Diagram



Clock Recovery Macros

The clock recovery PLL will generate a clock which is at the same frequency and 180 degrees out of phase with the serial data input. This generates clock and data outputs from the incoming serial bit stream which feeds the subsequent parallel conversion. An external clock reference is used to reduce initial acquisition time and to provide stability in the absence of serial data. The filter parameters are set to optimize the loop for the anticipated serial data input characteristics. These include: maximum run length and transition density of 1's or 0's, and the jitter associated with the fiber optic link. Loop filter parameters can be varied on a custom basis by AMCC.

Specifications

Input Reference Frequency — The input reference frequency can be a selected divide ratio of the VCO clock frequency. The maximum divide ratio is 64.

Reference Clock Jitter — The reference clock needs to be generated from a stable clock source such as a crystal oscillator. For maximum performance rms jitter should not exceed .04% of the reference clock pulse width.

Input Reference Stability — The reference clock stability should be less than 100 ppm.

Acquisition Time — The loop acquisition time will depend on the loop filter parameters. (1.0 μ s to 250 μ s values are typical)

Edge Jitter — The edge jitter will depend on the loop filter parameters and the serial data input specifications. (50 ps to 100 ps pk-pk values are typical)

Supply Voltage Sensitivity — Power supply noise rejection will be between 40 and 60 dB depending on the noise spectrum.

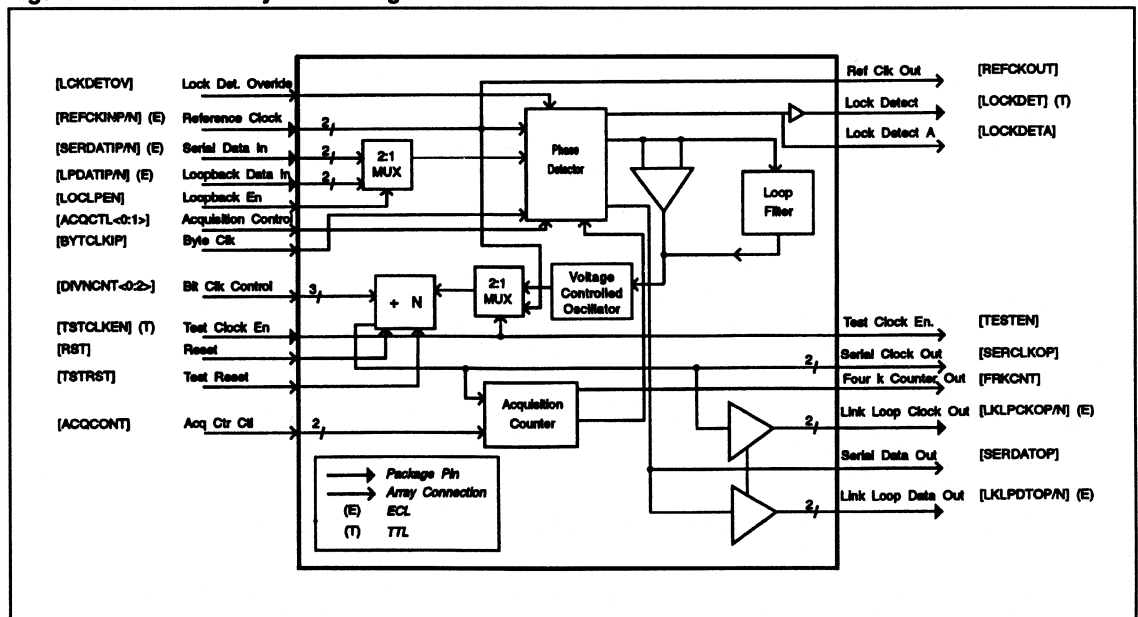
Data Rate — The possible serial data rates from which a clock can be recovered will be grouped around the VCO center frequency and integer divide ratios of 1, 2, 4, and 8.

Allowed Data Jitter — The allowed input data jitter will be a function of the acquisition time, the loop filter parameters, the data rate and the allowed bit error rate. The jitter specification includes duty cycle distortion, random jitter and data dependent jitter.

Pull In Range — The pull in range of the VCO is $\pm 6\%$.

Bit Error Rate — Bit error rates of 10^{-12} or lower are achievable.

Figure 8. Clock Recovery Macro Diagram



ELECTRICAL CHARACTERISTICS
Q20P010/Q20P025
**Table 3. TTL Controlled Edge Rate BiDirectional I/O Macro
AC Electrical Characteristics (Dual Supply +5V/-5.2V or -4.5V)**

SYMBOL	PARAMETER	Test Conditions	COM 0°C to 70°C		MIL -55° to +125°C		UNIT
			MIN	MAX	MIN	MAX	
TOPD←	TTL Output Propagation Delay, Falling Edge	No Load	2.741	4.278	2.598	4.469	ns
		15pF	3.596	6.138	3.033	6.689	
TOPD→	TTL Output Propagation Delay, Rising Edge	No Load	4.174	6.942	3.652	7.226	ns
		15 pF	4.489	7.647	3.922	8.066	
TIPD++	TTL Input Propagation Delay, Rising Edge	No Load	247	755	177	1085	ps
TIPD←	TTL Input Propagation Delay, Falling Edge	No Load	40	260	8	323	ps
TPLZ	Output Disable Time from Low Level	refer to the Q20000 Data Sheet	2.164	3.685	1.718	3.910	ns
TPHZ	Output Disable Time from High Level	refer to the Q20000 Data Sheet	2.741	4.032	2.655	4.091	ns
TPZH	Output Enable Time to High Level	refer to the Q20000 Data Sheet	2.265	5.235	1.818	5.979	ns
TPZL	Output Enable Time to Low Level	refer to the Q20000 Data Sheet	5.166	8.745	4.805	11.284	ns

Table 4. High Speed ECL Output, AC Electrical Characteristics

SYMBOL	PARAMETER	Test Conditions	COM 0°C to 70°C		MIL -55° to +125°C		UNIT
			MIN	MAX	MIN	MAX	
TPD←	ECL Output Delay, Falling Edge	No Load	203	382	176	399	ps
		15pF	443	922	386	1059	
TPD→	ECL Output Delay, Rising Edge	No Load	256	439	228	466	ps
		15pF	556	1009	483	1261	
Fout	ECL Output Frequency			1.25		1.25	GHz

Minimum and maximum specifications account for temperature, voltage, and process variations over the given operating range. For complete specifications, refer to the Q20000 Device Specification and Q20000 Array Series Design Manual.

PACKAGING

The Q20P010 and Q20P025 PLL arrays are available in surface mount technology offering loop filter elements mounted on the package. All packages have been custom designed by AMCC to offer controlled impedance on high speed signals and minimal digital noise injection to the PLL area. For complete details consult the AMCC Packaging Guide.

Package Availability & Thermal Characteristics θjc in °C/W		
Package Type	Q20P010	Q20P025
68 LDCC	6.0	—
100 LDCC	6.5	5.0
132 LDCC	—	5.0

Figure 9. 68 Lead Hermetic Ceramic Flatpack

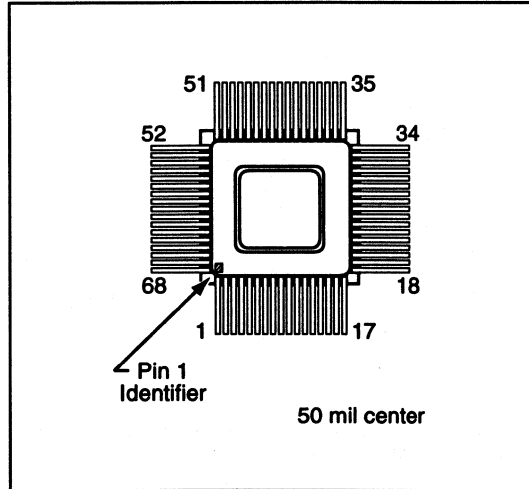


Figure 10. 100 Lead Hermetic Ceramic Leaded Chip Carrier

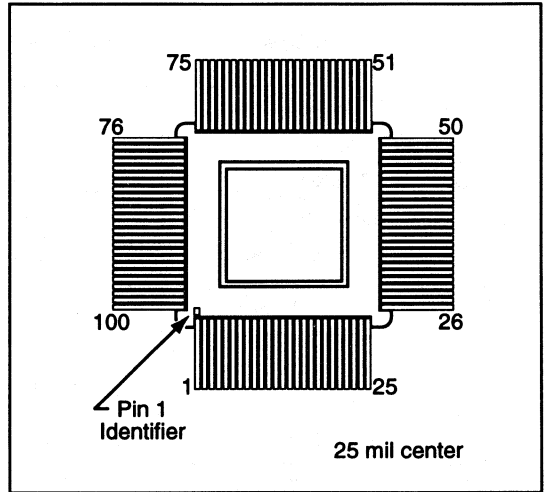
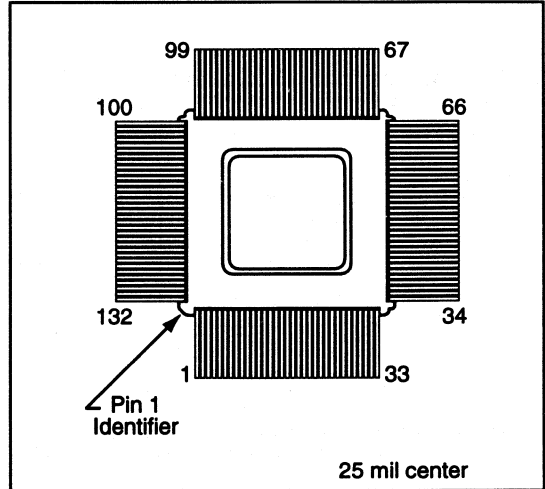


Figure 11. 132 Lead Hermetic Ceramic Leaded Chip Carrier



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